

UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION

In the Matter of

RAMBUS INCORPORATED,

a corporation.

Docket No. 9302

COMPLAINT COUNSEL'S
PROPOSED
FINDINGS OF FACT,
CONCLUSIONS OF LAW
AND ORDER

Volume I

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**COMPLAINT COUNSEL’S
PROPOSED
FINDINGS OF FACT,
CONCLUSIONS OF LAW
AND ORDER**

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Volume I

Introductory Matter

1. Pursuant to Rule 3.46(d) of the Commission's Rules, 16 C.F.R. § 3.46(d), Complaint Counsel state their intention to file stipulated witness and exhibit indices conforming to the requirements of Rule 3.46(b) and (c) of the Commission's Rules.

2. These Proposed Findings of Fact use the following forms of citation:

- Testimony from the trial transcript in this case is cited by witness last name and transcript page: (Crisp, Tr. 2927-28). Citations to testimony of Gordon Kelley and John Kelly include the first initial to avoid confusion.
- Exhibits admitted in evidence in this case are cited by exhibit number and page: (CX0711 at 59) or (CX0545 at 5-9).
- Testimony from depositions or prior proceedings is cited by the exhibit number and the page, followed by a parenthetical with witness name and short description of the transcript: (CX2089 at 41-43 (Meyer, Infineon Trial Tr.)). Page references refer to the internal numbering of the transcript, not the exhibit numbering.

- In camera materials are designated using braces and bold type, with reference to the in camera status in italics in the citation, as specified in Paragraph II of the Order on Post Trial Briefs, July 10, 2003.
- The Answer of Respondent Rambus Incorporated to the Complaint herein, filed July 29, 2002, is cited by page and paragraph as follows: (Rambus Answer at 41, ¶ 101).
- The Parties' First Set of Stipulations, filed April 23, 2003, and The Parties' Second Set of Stipulations, Filed July 25, 2003, are cited by stipulation number, as follows, respectively: (First Stipulations, No. 22) or (Second Stipulations, No 3).
- References to the Rambus privilege log in this case are to the version dated March 14, 2003, included as Tab 9 to the Motion *In Limine* Regarding Rambus's Patent Prosecution Efforts after June 1996 and Neil Steinberg's Opinions Regarding the Scope of Rambus's Prior Patent Applications, filed March 26, 2003, and are cited as follows: (Steinberg Motion *In Limine*, Attachment 9, Rambus Privilege Log Entries). Rambus continued to provide Complaint Counsel with other revised versions of its privilege log through this week, which have not been filed in the record of the case. On September 4, 2003, Rambus confirmed that its document production was complete and that the most recent version of its revised privilege log was final.
- These Complaint Counsel's Proposed Findings of Fact are cited by paragraph, as follows: (CCFF 507) or (CCFF 743-45).

3. There have been filed with the Administrative Law Judge designations of prior deposition and other testimony which the parties have sought to have included in the record in this case. (The Parties' Designated Deposition Testimony (Second Corrected Version, filed August 25, 2003)). While some designated testimony has previously been admitted into the record and read or played at the trial herein, as of the time these Proposed Findings were prepared there remained a number of testimony designations that had not yet been ruled upon. Because Complaint Counsel believe that these designations contain admissible material and reliable evidence relevant to matters at issue in this case, we have cited appropriate portions of this designated testimony in these Proposed Findings. In the event that portions of this designated testimony are not admitted to the record, we request that any citations to such non-admitted matter in these Proposed Findings be disregarded.

The witnesses and transcript exhibits from which testimony designations had been made but not ruled upon, as of the time these Proposed Findings were prepared, are as follows:

Crisp: CX2052, CX2053, CX2069, CX2082, CX2092, CX2093, CX2086,
CX2087, CX2094, CX2104

Davidow: CX2067, CX2083, CX3132, CX2109

Farmwald: CX2064, CX2065, CX3131, CX2096, CX2097, CX2106

Harmon: CX2070

Horowitz: CX2062, CX2063, CX2100, CX2101, CX2116

Mooring: CX2054, CX2056, CX2055, CX2066, CX2079, CX2081,
CX2098, CX2105, CX2112

Tate: CX2060, CX2061, CX2072, CX2073, CX2074, CX2084, CX2088,
CX2099, CX2111

Ware: CX2103, CX2115

4. Paragraphs 4 - 9 are unused.

I. The DRAM Industry.

A. What is a DRAM?

10. DRAM stands for “Dynamic Random Access Memory.” (Rhoden, Tr. 266-67). DRAM is a type of electronic memory. (Rhoden, Tr. 266). DRAM is “dynamic” because it needs to be refreshed every fraction of a second. (Rhoden, Tr.266-267 (“dynamic is something that is a temporary storage.”)).

11. The primary use for DRAM is in computer systems. (Rhoden, Tr. 267 (“Probably the largest percentage of DRAM winds up in computer systems.”); Gross, Tr. 2272-2273 (About 95% of Hewlett Packard purchases of memory are used in computers, including servers, the remaining 5% are used in printers, cameras and camera accessories).

12. DRAMs are also used in a wide range of other products. (Sussman, Tr. 1362 (“Q. What applications or end products would use these DRAMs? A. Basically everything that needed to temporarily store data, a very wide range of products. It could be from today's MP3 music to the supercomputer that NASA would have.”)). These products include servers (Kellogg, Tr. 4993; Tabrizi, Tr. 9126-9127;), workstations (G. Kelley, Tr. 2376-2377; Krashinsky, Tr. 2770-2771; Farmwald, Tr. 8206-8207; Tabrizi, Tr. 9126-9127), printers (Kellogg, Tr. 4986-4987; Krashinsky, Tr. 2770-2771; Gross, Tr. 2272-2273), PDA's (Krashinsky, Tr. 2770-2771) and cameras (Gross, Tr. 2272-2273).

13. In a computer system, DRAM is the area where transactions and information is stored and processed, stored and retrieved while the computer is in operation. (Rhoden, Tr. 267-68).

14. Typically, multiple DRAM chips are placed on a memory module, which is a small printed circuit board (Rhoden, Tr. 272-73; *see, e.g.*, DX0001). The module containing the DRAM chips connects to a motherboard. (Rhoden, Tr. 269, 273).

15. The central processing unit (“CPU” or “microprocessor”) is the “brains” of the computer. The CPU processes and makes decisions based on the information that it receives from memory devices, including the DRAM chips. (Rhoden, Tr. 271-72). The CPU is located on the motherboard. (Rhoden, Tr. 275-76; *see, e.g.*, DX0003).

16. A chipset or controller is a group of computer chips that connect the various components of the motherboard, including the DRAMs and the central processing unit. (Rhoden, Tr. 275 (chipset “defines a grouping of chips that actually are the traffic cops for the motherboard. They connect . . . the memory, the CPU, all of the different I/O devices.”)). The chipset communicates with the DRAM by sending signals for the clock, control, address, and data commands that travel along buses between the chipset and the DRAM. (Rhoden, Tr. 277-

79).

17. A DRAM is made up of a number of cells. (Rhoden, Tr. 359). Information is stored in the cell capacitor as either a high or low voltage. (Rhoden, Tr. 359). The cells of the DRAM are divided into an array via a series of rows and columns with the cells located at the intersections of those rows and columns. (Rhoden, Tr. 359-60). Access to the cell capacitor is made by activating a transistor, which transfers the voltage in the capacitor to a column or bit line. (Rhoden, Tr. 359-60).

18. In the early 1990s, the typical DRAM contained 16 million cells, or 16 “megabits”. (Rhoden, Tr. 360-61).

19. The row address strobe (“RAS”) accompanies the row address information, which supplies the information necessary to identify the row within the DRAM that is required to respond to a particular request from the controller. (Rhoden, Tr. 365).

20. The column address strobe (“CAS”) accompanies the column address information, which supplies the information necessary to identify the column within the DRAM that is required to respond to a particular request from the controller. (Rhoden, Tr. 368).

21. Information is sent to or from the DRAM cells in response to requests made by the chipset. The chipset provides row and column addresses that determine where the information can be found or should be stored. (Rhoden, Tr. 361-63). A sense amplifier senses whether the voltage in the cell capacitor is low or high. The sense amplifier, in turn, is connected to the data output “bus” lines. (Rhoden, Tr. 366).

22. There are different types of DRAM, including asynchronous and synchronous. The term “asynchronous” refers to a DRAM device that operates without reference to a free running clock. Instead, the controller sends instructions to the memory and waits for a response for a period of time that is not synchronized. (Rhoden, Tr. 368; Jacob, Tr. 5394)

23. The term “synchronous” refers to a DRAM device that is synchronous with a free running clock. (Rhoden, Tr. 370-372; Sussman, Tr. 1359).

24. A free running clock operates continuously in contrast to other clock-type signals that only operate intermittently. (Rhoden, Tr. 368).

B. DRAMs Must be Compatible and Interoperable with Other Components.

25. DRAM chips are not sold individually to consumers. Instead, they are included in other products that are then sold to consumers. Examples of products that incorporate DRAM include personal computers, memory modules, graphics cards, printers, servers, and

telecommunications switches. The customers for the DRAM manufacturers are those firms that include DRAMs in their products. (Rhoden, Tr. 298; McAfee, Tr. 7183, *see also* DX0132). For example, SDRAM is used by HP in its printers, servers, and in some of its notebook computers. (Gross, Tr. 2275). DDR SDRAM is approximately 80% of the DRAM that HP buys, and it is used in desktop computers, notebook computers and servers. (Gross, Tr. 2274-76)

26. A DRAM alone is not useful; it needs to communicate with many other components in the computer. (Macri, Tr. 4589 (“It needs to talk to other things, and there's a vast array of, you know, system types, from like a personal computer to a digital television, they all use the DRAM a bit differently.”); Peisl, Tr. 4402-03 (“Memory is interfacing with a number of components on the motherboard . . . [including] the controller. . . modules . . . BIOS”)).

27. In order for DRAM to have any value, it must be compatible with the other components in the products that include the DRAM. (Peisl, Tr. 4410 (“Interoperability between that the DRAM works flawlessly together with all the components in the system. It's not only one chip that the DRAM is interfacing with but all the other components on the motherboard, the position on the motherboard, the particular layout on the motherboard, other components on the modules, for instance, like registers. You have to make sure that your part is fully compliant with all the specifications of the other chips. This is why everybody is working towards the JEDEC specification. That's the common denominator.”); CX1075 at 1 (“A phone or computer that is almost compatible is one that doesn't work. If people build parts 99% compatible, the systems companies won't buy them.”); Heye, Tr. 3655-65, *see*, DX0030; Jacob, Tr. 5562-66, *see also* DX0105)).

28. It is important to DRAM customers such as PC-OEMs that the DRAM that they buy is interoperable with the other components of their systems. (Peisl, Tr. 4409 (“And the second issue is the interoperability. They of course wanted to make sure that our parts work together with all the other components in the system.”); CCF 27 and 114)

C. How DRAMs are Made.

1. Establishing a DRAM “Fab.”

29. DRAMs are manufactured in plants commonly called “fabs.” (Becker, Tr. 1101)

30. Billions of dollars are required to create factories and designs necessary to produce DRAMs (Rhoden, Tr. 297 (“there's a great deal of investment, billions of dollars, that go into the creation of factories and designs that are necessary to produce DRAM. . .”) ; Shirley, Tr. 4161 (“when we bring a new production process to Micron, that's a very expensive process, the act of buying this new tooling for the production plant.”)).

31. The Infineon fab in Richmond, Virginia has so far cost approximately \$1.5 billion.

About \$350 million of that amount was for the buildings and the building infrastructure, office furniture, computer systems and facilities systems. The balance, about \$1.2 billion, was for the actual processing equipment used to manufacture the DRAM chips and modules. (Becker, Tr. 1108).

32. From groundbreaking to production of a qualified chip, it can take two years to build a new fab. (Becker, Tr. 1106-07).

33. Manufacturers generally require 20-25 identical mask sets to achieve full-ramp production of a DRAM. (Becker, Tr. 1123). A full mask set costs approximately \$1 million. (Becker, Tr. 1122-23).

34. Manufacturers frequently are forced to purchase multiple iterations of a mask set as defects are identified and redesigns occur. (Becker, Tr. 1150-51 (“Typically we’ll do at least one all layer redesign, so we’ll buy 22 layers, run those, we will find issues, and we will have to do a redesign of all 22 layers. We will order those 22 layers again with correction. And then typically we will have to. . . redesign maybe four or five of those layers two or three or four times after that to finetune the performance.”)).

2. The DRAM Manufacturing Process.

35. The starting point in the manufacturing process is a bare silicon wafer. (Becker, Tr. 1116-1117).

36. During the course of the manufacturing process, successive layers are built up on the silicon wafer. (*See generally* Becker, Tr. 1116-32 (describing the process on how a bare wafer becomes a processed layer containing hundreds of chips.)). DRAMs require as many as 22 distinct layers. (Becker, Tr. 1131). Each layer requires a series of manufacturing steps. (Becker, Tr. 1131-1132). Processing the wafer takes about 400 manufacturing steps. (Becker, Tr. 1131)

37. The manufacturing process is non-linear, meaning that a wafer will re-enter different processing area of the fab a number of times. (Becker, Tr. 1118).

38. A processed wafer contains hundreds of individual DRAM chips. (Becker, Tr. 1117).

39. The processed wafer is electrically tested in order to find the good chips. (Becker, Tr. 1132-1133)

40. After testing, the wafer is cut into individual DRAMs. (Becker, Tr. 1132-1134)

41. The individual chips are then bonded to a metal lattice like structure called a lead

frame and are covered with a black hard plastic mold compound. (Becker, Tr. 1132-1134)

42. After packaging, the good chips are built into components and tested again. (Becker, Tr. 1132-1134).

43. The testing and packaging process takes approximately two weeks. (Becker, Tr. 1136).

44. The tested components may also be assembled onto circuit boards to create modules and are further tested. (Becker, Tr. 1135) This process takes approximately 1 ½ weeks. (Becker, Tr. 1136; *see generally* Becker, Tr. 1132-36 (describing the process on how the chips are built into components and connected to modules)).

45. The Infineon plant in Richmond produces approximately 3.5 million DRAM chips per week. (Becker, Tr. 1139).

3. Development of a New DRAM, From Specification to Full Production.

46. The development of the DRAM proceeds along a number of “phases” and milestones. Those are the design phase, the layout phase, the simulation phase, the verification phase, “tape out,” initial silicon, the validation phase, internal qualification phase and the production phase. (Shirley, Tr. 4141-42; Reczek 4306-4341; *see* DX0044).

47. Concurrently with the development of the DRAM itself, industry participants dedicate substantial resources to ensuring that the future DRAM products will be available on the same schedule as the other components that make up PCs, servers and workstations. (Gross, Tr. 2278 (“We frequently meet with the technical teams as well as the executive teams with each of our largest partners to exchange projections into the future of the types of technology that we’re going to be needing in our computers, as well as the types of technologies and the mix in volumes that the suppliers plan to manufacture. And we endeavor to work toward a very close alignment of those technology roadmaps.”); Peisl, Tr. 4447; Heye, Tr. 3636-3637; MacWilliams, Tr. 4799-4800).

48. In the design phase, the DRAM designers implement the DRAM specification as a set of circuit designs or schematics. (Shirley, Tr. 4142-43).

49. In the layout phase, the layout designers take the circuit designs created in the first step and create a representation of the circuit designs. (Shirley, Tr. 4143).

50. In the simulation phase, the design engineers simulate the designs in order to verify that the chips will perform as intended before they are first manufactured. (Shirley, Tr. 4144).

51. The verification phase involves ensuring that the schematics created in the design phase are in fact represented by the work done in the layout phase. (Shirley, Tr. 4144-45; Reczek, Tr. 4309).

52. Tape out involves the process of transferring the DRAM layout onto masks that will be used in the fabrication of the DRAM. (Shirley, Tr. 4145). The collection of individual masks necessary fabricate a DRAM design comprises a mask set. (Shirley, Tr. 4147).

53. A mask contains an image that is transferred to the wafer through a process of using light to expose the wafer to the image pattern in the mask and using gasses to etch the resulting pattern into the wafer. (Becker, Tr. 1122-24).

54. At some DRAM manufacturers, including Micron, the physical creation of masks is done by specialized firms that provide the service to the DRAM manufacturers. (Shirley, Tr. 4145-46). Other DRAM manufacturers, including Infineon, produce their own masks. (Reczek, Tr. 4312).

55. For a new design, it generally takes between 6 and 18 months from the beginning of the design phase for a DRAM to be taped out. (Shirley, Tr. 4149; Reczek, Tr. 4342-45; *see* DX0045).

56. The mask set, once it is received, is used to create the first physical manifestation of the DRAM chips on wafers. Those wafers are referred to as “initial silicon.” (Shirley, Tr. 4147).

57. Initial silicon is then tested in the validation and internal qualification phases to ensure that the DRAM on the wafers operate the way they were intended (the validation phase) and that the DRAM on the wafers operate appropriately in the expected environments (the qualification phase). (Shirley, Tr. 4148-49).

58. It can take between 4 and 9 months for a DRAM design to proceed from tape-out through the internal qualification phase. The length of the period depends on the number and types of problems that are found during the test phases. (Shirley, Tr. 4149).

59. Once internal qualification has been completed, it takes another 6 to 9 months to begin high volume production. (Shirley, Tr. 4150-51).

60. Once the internal qualification is completed, “customer samples” of the new DRAM are sent to customers to allow them to test the DRAM. At the same time, additional mask sets are ordered to get ready for high volume production of the new DRAM. (Shirley, Tr. 4149-50).

61. Manufacturers must be in frequent contact with customers to provide technical support for the varied products of the customer in which the DRAMs will be installed. (Peisl, Tr.

4400-02). Manufacturers may send their own engineers to work in the facilities owned by the customers for the purpose of assisting in the validation of the customer samples. (Peisl, Tr. 4399).

62. Manufacturers and customers must test the DRAM extensively. (Peisl, Tr. 4404 (test “all possible configurations, with all the controller chips that were available, all the major motherboard configurations . . . we couldn’t predict where a weakness would occur, so we had to know all the different influences.”)).

63. Once the DRAM is approved for purchase by the customer, DRAM manufacturers “ramp up” production of new DRAMs from low levels of production or no production. (Becker, Tr. 1144-45).

64. Ramping up a new DRAM at a DRAM fab requires a substantial amount of time. (Becker, Tr. 1158-60; Reczek, Tr. 4340-41 (it “takes somewhere in between four to six quarters, which is one to one and a half years, until you have fully converted all your production facilities to run the new -- the new part.”)).

65. From the time a manufacturer receives a completed specification, it can take more than two years to complete a new DRAM for production. (Peisl, Tr. 4373).

4. DRAM Design Modifications - Shrinks, Density Changes and Changes in Type.

66. There are three principal types of changes that are made by DRAM manufacturers: shrinks, changes in density, and changes in DRAM type. (Reczek, Tr. 4304; *see* DX0045).

67. A shrink involves taking an existing DRAM chip and re-designing it so that it can be used on a more advanced process that will allow the size of the chip to shrink. A shrink reduces costs by allowing more DRAMs to appear on each wafer, spreading the costs of producing that wafer over a larger number of chips. (Becker, Tr. 1155-57; *see*, DX0007 at 18 (“probably the biggest thing we do to influence or decrease our costs on a regular basis is we shrink the technology, and the reason that works so well is that we’re able to produce the same part with the same function,... but we can produce it on a smaller chip.... So if you have a smaller chip, you can fit more of those chips on a wafer, your cost per chip is greatly reduced...”).

68. A shrink typically takes approximately 18 months. (Reczek, Tr. 4343; *see* DX0045).

69. Changes in density involve increasing the number of DRAM cells on a particular DRAM design, keeping the same interface elements. (Becker, Tr. 1141). DRAM manufacturers make different DRAM densities depending on the demand from DRAM customers. (*see*, Becker, Tr. 1153-54 (“[I]t was our belief or desire that the next density would be the 256-megabit

SDRAM, so we went from 64 – production of the 64 to developing the 256... but it turned out ... in reality, our customer base really wanted to purchase 128-megabit density. So, we then had to go back and do the work on the 128-megabit SDRAM density....”)).

70. A change in density can take two years or more, depending on the difficulty of the transition. (CX0415 at 5; Reczek, Tr. 4341-4346; *see also* DX0045).

71. Changes to DRAM type involves making changes to the interface of the DRAM as well as making other changes required to accommodate changes in DRAM standards. (Reczek, Tr. 4304, 4310-11 (“So, for example, different types of DRAMs, the switch from an EDO part to a synchronous part or maybe from a synchronous part to a double data rate part, so this would refer to a change in type of the DRAM.”)).

72. A DRAM manufacturer’s first step in manufacturing a new DRAM is to develop a DRAM specification. (Shirley, Tr. 4137; Peisl, Tr. 4373-4374). A DRAM specification is a set of functional and operational guidelines that describe what a DRAM should do under certain circumstances if it's given certain commands or if it's given certain parameters. (Shirley, Tr. 4137-38; Peisl, Tr. 4388-4389). These DRAM specifications are then used by the DRAM designers to design the DRAM. (Shirley, Tr. 4137).

73. Manufacturer’s DRAM specifications are developed from JEDEC standards as well as from inputs from DRAM customers. (Shirley, Tr. 4138-40; Peisl, Tr. 4373-4374; Landgraf, Tr. 1685; *see, e.g.*, CX2410 at 1 (“All inputs are compatible with the JEDEC Standard for SSTL_2”)).

74. The transition from one type of DRAM to another can take much longer than two years depending on how difficult the transition is. For example, when Infineon began its transition from SDRAM to DDR SDRAM, it had to go through three major redesigns before it was able to produce a device that showed acceptable customer performance. That required that Infineon had to repeat a number of steps to finally implement the design change. (Reczek, Tr. 4350-51; CX2107 (Oh, Dep.) at 55-56 (a change in DRAM type is a “very, very long procedure. It normally takes about three years.”); Reczek, Tr. 4350-51 (transition from SDRAM to DDR SDRAM required three major redesigns).

75. A DRAM manufacturer normally does not attempt to do two different types of changes at the same time. (Reczek, Tr. 4305-4306). For example, when a DRAM manufacturer does a shrink, it does a shrink on a product that already exists so that there are fewer changes to track. (Becker, Tr. 1157-58 (“[F]or instance, when we went from .24 [micron] to .20 [micron], we did that with the same 64-meg SDRAM. So, we did all of our product learning at 0.24 [micron], we had to do all of our process and technology learning at 0.2 [micron], but we did it with a product we already knew.”); CX2108 (Oh, Dep.) at 254 (when doing a shrink, “You don’t change anything” on the inside of the DRAM, “It has nothing to do with the circuit. No circuit

change at all.”), 257 (Hyundai’s practice was not to modify its design at the time it did a shrink)).

76. A DRAM manufacturer would not attempt to make a change to a DRAM type at the same time it was doing a shrink or a change in density because multiple changes makes it difficult to determine what is going wrong if the DRAM has a defect. (Reczek 4304-4305 (“So, in the case you take two steps at one time, so this might lead to very big problems, and for example, if something is not working, you don’t know whether the technology is not working or the design is not working. So, its very difficult to figure out what’s really going on, what’s really going wrong there.”)).

77. On occasion, manufacturers undertake a so-called “revision” design at the time of a shrink or a change in density. A revision design involves taking an existing design and changing certain circuitry in that design. A revision design usually occurs only when a DRAM manufacturer has found something fundamentally wrong with a DRAM design project that has already made it to silicon. (Shirley, Tr. 4168; CX2108 (Oh, Dep.) at 257 (“We normally don’t [redesign some of the internal circuitry at the time of a shrink] unless . . . [the part] has a big problem, if it does not work, then we do, but normally we don’t do that.”)).

D. DRAM Industry Market Structure.

78. The DRAM industry is cyclical, and is characterized by sharp fluctuations in price. (Appleton, Tr. 6277-78 (“It’s probably one of the most volatile businesses that exists today . . . the selling price of the product dramatically changing over time. You can have as much as an 80 or 90 percent drop in selling price in as short a period of time as 18 to 24 months.”) and 6281 (“Q. Do you regard the DRAM business as a cyclical business in any way? A. Yes, well, it's very cyclical. When you consider that Micron's revenues can go up 3X and then drop by 80 percent from one year to the next, and when you talk about the supply that comes online in relatively large chunks, if you will, then it creates a very cyclical business”); Heye, Tr. 3641 (“The DRAM industry is very cyclical”)).

79. The DRAM industry has been marked by consolidation. (Appleton, Tr. 6259) In the early to mid 1980's, there were approximately 20-25 DRAM manufacturers. (Appleton, Tr. 6259) Today, there are only 5-6 major DRAM manufacturers left, along with 2-3 much smaller manufacturers in Taiwan. (Appleton, Tr. 6276-6277)

80. Approximate shares of sales of DRAMs in 2001 were: Samsung: 27%; Micron:19%; Hynix: 14.5%; Infineon: 9.7%; Elpida:8.5%; Toshiba: 6.4%. (CX2464 at 1)

81. The consolidation is due to uncompetitive manufacturers leaving the industry. (Appleton, Tr. 6277 (“[I]t's – it's been a very competitive business over time. Those companies that weren't able to focus on cost and reduction of cost simply weren't able to remain competitive, and the more competitive companies are the ones that have been able to remain, and the other

ones have exited the business.”)

82. In 1994, Micron was coming out of what had been a downturn in 1991 and 1992. (Appleton, Tr. 6288)

83. From 1998 through 2002, Micron made losses in each year except 2000. (Appleton, Tr. 6282-6284 and 6286-6287; *see* DX114). By mid way through 2003, Micron had made losses of approximately \$1 billion. (Appleton, Tr. 6284)

84. Typically, only one type of DRAM tends to dominate the market at any one time. As each generation of DRAM is succeeded by a new one, the volume of sales of the older generation slowly drops off, and is replaced by sales of the new generation. (See McAfee, Tr. 11216-11217).

85. Thus, in the mid 1990's, the dominant form of DRAM was asynchronous. In 1995, fast page mode (FPM) accounted for 87.2% and extended data out (EDO) 9.9% of DRAM revenue share. (Rapp, Tr. 10248)

86. By the late 1990's, however, synchronous DRAMs (SDRAMs) had supplanted asynchronous as the dominant form of memory sold in the market. In 1998, SDRAMs accounted for approximately 60.8% of DRAM revenue share; EDO accounted for about 27.6%, FPM accounted for about 8.8%, RDRAM accounted for 1.6% and others accounted for about 1.3%. (Rapp, Tr. 10249).

87. In 2001, SDRAMs accounted for about 69.7%, RDRAM accounted for 12.5%; EDO accounted for 7.7%, DDR SDRAM accounted for 5.3%, FPM accounted for 4% and others accounted for 0.8%. (Rapp, Tr. 10249).

88. In January 2001, according to Rambus CEO Tate, DDR SDRAM accounted for 10 percent of the market, SDRAM accounted for 80 percent of the market, and RDRAM accounted for between 5 and 10 percent of the market. (CX2061 at 45-46 (Tate, Dep.)).

89. In January 2001, according to Rambus CEO Tate, all systems shipping in the PC desktop and lap top market are using one of: Rambus DRAM, SDRAM, or DDR SDRAM for main memory. (CX2061 at 51-52 (Tate, Dep.)).

90. Over time, the bus speeds with which DRAMs have been able to operate has increased. In 1988 DRAM bus speeds were around 10 MHz. (Horowitz, Tr. 8081) The 2002 Infineon product information guide, in comparison, lists DDR SDRAMs running as high as 333 Mhz and SDRAMs running as high as 166 Mhz. (CX2466 at 5-7; *see* Becker, Tr. 1142)

91. Over time, the capacity of memory has increased substantially. (CX2853 at 37-41; CX2225 at 251-252) For example, from the mid-1990's to 2001 Infineon went from producing

64 Mb SDRAMs to 512 Mb DRAMs. (Peisl, Tr. 4384-4385; Becker, Tr. 1168-1173; Reczek, Tr. 4298-4300) Currently, companies are in the process of designing 1 Gb DRAMs. (Soderman, Tr. 9426)

92. Over time, the process technology, or size of the circuits and traces on each DRAM, has decreased. For example, Micron has decreased its process technology from .20 to .11 microns. (Appleton, Tr. 6294).

E. DRAMs are Commodities.

93. DRAMs are regarded in the industry as commodity products. (Appleton, Tr. 6280 (“Q. Have you ever heard the DRAM business referred to as a commodity business? A. Sure. Q. And do you agree with that characterization? A. Ah, I do in many ways”); Bechtelsheim, Tr. 5756 (“the nature of the memory market is that there's a number of suppliers which are fiercely competing for the memory business and the cost or prices for memories in the market behave very much like a commodity-type market.”); Gross, Tr. 2307 (“among the components that we purchase for computers, it is the most commodity-like, it is the most influenced by the global supply and demand variables.”); Heye, Tr. 3636 (“every memory in itself is a commodity.”) and 3641); CX2107 at 30, Oh, Dep. Tr. 136 (“DRAM is – is a commodity in – in this electronic market, and they are – the DRAM manufacturers are producing standard products, so anybody who – can come and make the standard products.”); Becker, Tr. 1138 (“[T]he DRAMs that we build in the manufacturing factory or the Richmond facility are considered commodity parts.”); Polzin, Tr. 3960 (“We needed to make sure that whatever memory we chose in our systems for our microprocessors was a commodity and met the performance requirements at the lowest possible cost.”).

94. Business decisions of the DRAM manufacturers are driven by the fact that DRAMs are commodity products. (Becker, Tr. 1138-39 and 1154-55; CX2107 (Oh, Dep.) at 136, 159 (importance of cost); Horowitz, Tr. 8516-17 (choice of design)).

F. DRAM Manufacturers are Driven to Reduce Costs.

95. Cost in the DRAM industry is measured on a cost-per-bit basis. (Appleton, Tr. 6278-79 (“And so the cost to produce that individual bit is the way that we measure through time ... either cost reductions or how competitive we are.”)).

96. On a per-bit basis, DRAM prices have dropped by about 30 percent per year for at least the last 25 years. (Becker, Tr. 1160 (“That's the -- that's the historical ASP or average selling price curve that we get for our memory, and that's been for the last 25, almost 30 years.”)).

97. As a result of the fact that DRAM prices have dropped by 30 percent per year, DRAM manufacturers have historically reduced costs per bit by about 30 percent per year as

well. (Becker, Tr. 1155 (“within our industry, over the last 25 years or so. . . our industry has had to reduce its cost per bit or cost per piece of memory by about 30 percent per year just to remain competitive.”); Appleton, Tr. 6279 (“Micron’s been able to average over the last 20 years reducing our costs every year, compounded, approximately 25 to 30 percent annually.”)).

98. DRAM manufacturers must strive to reduce costs by about 30 percent per year in order to remain competitive. (Appleton, Tr. 6279 (“the most predominant factor in being successful in the DRAM business has been a company’s ability to continue to lower its cost per bit, and that’s why we focus so much on it.”); Becker, Tr. 1155 (“fact that we can’t control the selling price but can only control the cost, that means we have to do a very good job of controlling those costs. We have to be very aggressive to keep those costs down.”) and 1160-1161 (If Infineon does not reduce costs by 30 percent per year, “[m]y costs are significantly higher than my competitors, and I slowly go out of business.”); Bechtelsheim, Tr. 5761 (“It was well understood that the memory market was a very cost-competitive market”) and 5975 (“I would claim that memory prices are very competitive and there is in fact fierce competition in the market where virtually no manufacturer is returning a reasonable profit on their fab investment.”); Heye, Tr. 3636 (“they’re constantly cost reducing memory technology.”); McAfee, Tr. 7200-02, 7206-07).

99. DRAM manufacturers are extremely concerned about reducing their costs because their customers demand low cost products. (CX1708 at 2 (Richard Crisp writing “Compaq (Dave Wooten) like the others, stressed that price was the major concern for all of their systems. They didn’t particularly seem to care if the SDRAMs had 1 or two banks so long as they didn’t cost any more than conventional DRAMs. . . . Sun echoed the concerns about low cost. They really hammered on that point.”); CX1030 at 2 (“Mr. Choi said that when he met with Compaq, Compaq (server group) said that they will not use Rambus because of the royalty for the chip set.”); CX2383 (“[S]ince we are very cost conscious we are willing to drop features that add too much cost or complexity”); CX0711 at 34 (Richard Crisp writing “[T]hey want cheap, cheap, cheap”); JX0027 at 13 (“The Committee noted they wanted highest performance and lowest price SDRAM.”); CX2777 (“[T]he age old rule for DRAMs still apply. Customers will take as much performance as we can give them for absolutely no added cost over the previous technology. They will not pay extra for increased DRAM performance.”)).

100. DRAM manufacturers also are extremely concerned about reducing cost because producing at low cost is a critical factor to a DRAM manufacturer’s success in the marketplace. (Appleton, Tr. at 6277 (“Those companies that weren’t able to focus on cost and reduction of cost simply weren’t able to remain competitive, and the more competitive companies are the ones that have been able to remain, and the other ones have exited the business.”) and 6279 (“the most predominant factor in being successful in the DRAM business has been a company’s ability to continue to lower its cost per bit”); CX2107 at 136 (Oh, Dep.) (“ . . . the competition is very severe, and, as a result, the margin, the profit margin, is very, very small, so we have to be really concerned on the cost.”)).

101. The pressure to reduce costs creates incentives for DRAM manufacturers run their fabs continuously. (Becker, Tr. 1136 (“We try to operate our factory seven days a week, 24 hours a day, 365 days a year”), 1139 (“What we can control and what we can influence is what it costs us to manufacture those chips, and the lower our manufacturing costs, especially compared to our competitors, the better off we are, and one of the ways we do that is we leverage that \$1 and a half billion investment is by running it constantly. If it's sitting there not producing anything, then it's costing me money, and I'm getting no return on it.”); Appleton, Tr. 6254 (“we ran 24 hours, seven days a week beginning in 1983 shortly after I started with the company.”)).

102. Because of the complexity of shutting down and restarting a fab, shutting down for a single day can cause a loss of productivity equal to 2.5 days. (Becker, Tr. 1137-38).

103. One of the major ways that DRAM manufacturers are able to reduce cost is by performing shrinks on DRAMs already in production. (Becker, Tr. 1156 (“probably the biggest thing we do to influence or to decrease our costs on a regular basis is we shrink the technology, and the reason that that works so well is we're able to produce the same part with the same function . . . but we can produce it on a smaller chip, because we're using a smaller technology, and the wafer size doesn't change for us.”)).

104. Shrinks reduce costs by allowing manufacturers to achieve economies of scale by producing a higher volume of DRAMs per silicon wafer. (Williams, Tr. 872 (“Q. And it's been your experience that there are economies of scale which are realized in the manufacture of integrated circuits, correct? A. Correct. Q. The higher the volume, generally the cheaper the cost of manufacture? A. Correct.”); Peisl, Tr. 1156 (“So, if you have a smaller chip, you can fit more of those chips on a wafer, and if you get more of those chips on a wafer, your cost per chip is greatly reduced.”)).

105. The current high volume DRAM products are the first to experience cost reduction efforts by the DRAM manufacturers. (CX2544 at 1 (“Toggle happen[s] when volume hits... the memory vendors migrate the highest volume memory to the new processes first, therefore giving cost advantage.”); MacWilliams, Tr. 4837-4838 (“What it means is the transition of volume from one standard to the next. So what we're referring to is the fact that the DRAM vendors, for operating reasons, typically will shrink their highest-volume parts first, and therefore those parts have an advantage because they get the process technologies, the best cost structures first, it's in their economic interest to do so.”)).

106. Because current-generation commodity DRAMs are generally the highest volume DRAMs in production, current-generation DRAMs often have the lowest prices to DRAM customers. (Gross, Tr. 2306 (“[I]ndustry standard products are most often produced in the highest volume in the industry, and those efficiencies in manufacturing and the level of competition in that production enables the best cost per bit.”)).

107. The pressure to reduce costs also drives the DRAM industry to avoid paying royalties whenever possible. CX0711 at 13 (“Terry Walther of Micron . . . Said they are very nervous about doing a deal. Don’t like license type business he says.”), 35 (“Our proposition should be attractive there if we do not scare them away with extremely high license/royalty terms.”), 61 (“Farhad . . . says their #1 issue with the Rambus business proposal is the royalty rate. They do not want to be straddled [sic] with 3% royalties.”); CX0913 at 1 (“[IBM] asked lots of suspicious questions on our IP, patent pooling, and biz model. . . . He assured me that they are seriously considering Rambus. But the IP thing is a real dilemma.”); CX1030 at 2 (“Mr. Choi said that when he met with Compaq, Compaq (server group) said that they will not use Rambus because of the royalty for the chip set.”); CX0838 at 1 (“I think that Samsung is on a path to do anything they can to get out of paying us royalties”); Heye, Tr. 3731 (“The second concern [about Rambus’s patent claims] was a possible cost disadvantage we might incur in the infrastructure due to the incremental royalty fees”); Appleton, Tr. 6299 (“when I became CEO in 1994, we were paying approximately 10 percent of our revenues in royalties, and we knew that going forward that that just wasn’t going to work for the DRAM business model, it just wasn’t possible to do that, and as a result, we focused on developing our own know-how, if you will, developing our own intellectual property, and we already talked about capturing that intellectual property so that we could reduce those royalty rates.”); CX2107 at 158 (Oh, Dep.) (“[A royalty] will add additional cost to the manufacturing cost, so we are very much concerned.”)).

108. DRAM manufacturers were particularly concerned to avoid royalties on high-volume, commodity DRAMs. (CX2107 at 159 (Oh, Dep.) ([C]ost is “very, very important” on high volume commodity parts); CX2250 at 2 (“License is ok for niche, but not for main memory.”); Lee, Tr. 7047 (“He had made a statement on the order that having a license fee for some small-volume product would be reasonable, but it didn’t make sense for a very high-volume product of that magnitude for main memory.”); *id.* at 7047-48 (“the 2 percent [royalty demand] was larger than anything we’d ever heard of for an interface technology and certainly the largest thing we ever heard of for some sort of fee we’d have to pay to produce main memory.”); CX0676 (“[Samsung] will think that 2% is high for a commodity (memories).”))

109. Concerns about royalties on high-volume commodity DRAMs have caused the industry to prefer royalty-free open standards whenever possible. (CX2107 at 137 (Oh, Dep.) (open architecture was important to Hyundai “[b]ecause it means that it is adopted by JEDEC, and thus it requires no royalty or no fees at all.”); CX2294 at 15 (“Strong Points . . . Open architecture without royalties or fees”); CX0676 (“[Samsung] will think that 2% is high for a commodity (memories)”); CX2726 at 7 “Why DDR Is Cost Effective No Royalties”)

110. Even with respect to DRAM architectures that were not regarded as high-volume commodity products (including RDRAM before it received Intel’s endorsement), DRAM manufacturers sought to negotiate royalties down as far as possible. (CX0733 (Tate e-mail: “Big stumbling block is royalties – they [Samsung] want numbers in 1% or less range.”); CX0711 at 61-62 (Crisp e-mail: Hyundai “didn’t care that much about the first xxx million units: their worry

was what if the product was wildly successful: how can they minimize the upside risk? SO he liked the idea of a pre-set schedule of declining royalties.”; “So my suggestion is a . . . 2.5% DRAM royalty declining to 1.25% after 50 million cum units ship.”).

111. When the DRAM industry is unable to avoid royalties completely, they have sought to negotiate royalties down as far as possible. CX0961 at 1 (“I had requested a 1:1 with pat g[elsinger of Intel] as a result of his request . . . to lower our rdram royalties to <0.5%”); CX0974 at 1 (“On royalty reduction we tried several trial discussion with major dram partners and NONE were willing to trade royalty reductions for CHANGES IN BEHAVIOR: all said give me lower royalty and I’ll be more motivated.”); Appleton, Tr. 6300 (Micron has “gone through negotiations, future negotiations as we developed our own property, and as a result of that, our royalties today are very insignificant. Essentially they have gone from 10 percent of the company to an insignificant percentage of the company.”).

G. Strong Forces Drive Standardization in the DRAM Industry.

112. Standards are essential in the DRAM industry. (CX2634 at 3 (article by former Rambus expert states: “Deviation from the herd is not tolerated by the marketplace. Not since the 1970s have individual DRAM vendors had the power to innovate architecturally.”) CX1284 at 28 (Rambus’s co-founder Mike Farmwald once stated, “There is real value in having a world DRAM standard.”)).

113. Standardization benefits the DRAM industry generally by ensuring quality and reliability. (J. Kelly, Tr. 1791 (“to the extent that companies are following JEDEC standards, there is a consistency in terms of quality and reliability”); Prince, Tr. 9016-17 (“when something comes for formal standardization, it has the review of peers throughout the industry. Everyone gets a chance to review it and make comment, and if there are good and bad features, they can be modified. And what ultimately comes out for the users in the industry is the most adequate device that the industry collectively can prepare.”)).

114. Standards in the DRAM industry ensure that the DRAM devices are compatible with other components. (Peisl, Tr. at 4410 (“Interoperability... [means] the DRAM works flawlessly together with all the components in the system. It’s not only one chip that the DRAM is interfacing with but all the other components on the motherboard, the position on the motherboard, the particular layout on the motherboard, other components on the modules, for instance, like registers. You have to make sure your part is fully compliant with all the specifications of the other chips. That is why everybody is working towards the JEDEC specification.”) and 4382 (Standards are “of utmost importance...not only for...a DRAM designer on one side, but it’s very important...for the chip designers at Intel, AMD and other companies who design the chips that communicate with our DRAMs as well, and it enables essentially the whole industry to develop products that work together in more or less a predefined manner.”); Heye, Tr. 3715 (“AMD spends a lot of time -- AMD works collaboratively with the

memory vendors through JEDEC to ensure that the memory standards going forward can be implemented both by the chipset vendors and the memory vendors.”)).

115. Standards in the DRAM industry ensure that the entire industry, including manufacturers of systems and compatible components, settles on one solution, thus allowing firms to make long-term investments the success of which depend on long-term investments made by others. (Macri, Tr. 4620-21 (Discussing CX1315, he states “[U]sually in the DRAM world, there is only one choice. You know, it’s not a matter of what; it’s a matter of when. So, users, they can plan their transition based on their own -- you know, their own internal decision-making process, plan their transition to meet their own business needs. The suppliers, they know making the investment up front is going to be realized, because they know the users will eventually move over. It may not all be at once, but over a period of time, they can count on the market slowly building up. In this particular case [when both DDR SDRAM and RDRAM could have become the dominant standard], there were two choices, and it was very unclear which way the world would go.”); Heye, Tr. 3678 (“from the time you start thinking about a chipset to implementing it, especially when it’s brand new like the one for AMD, it’s about two years prior to shipping.”); Bechtelsheim, Tr. 5796-5797 (“[O]ur design cycle was typically one to two years for a new product, so we would need to know at the beginning of that design cycle which exact memory technology we could use at the time the product would be manufactured.”)).

1. Benefits to DRAM Purchasers.

116. Customers require standardized DRAM because standards ensure that parts purchased from various manufacturers are perfect substitutes, thereby ensuring customers of multiple sources of supply. (CX1075 (“everyone wants multiple-sourced DRAMs, so to make DELL happy, you need multiple suppliers of DRAMs, modules, connectors, and clock chips”); CX1354 at 5 (“DRAM Industry: commodity business, Customers want multiple sourced, compatible DRAMs.”); Peisl, Tr. 4408-10 (“JEDEC essentially ensured that it had multiple sources because everybody in the industry, every major DRAM company or every DRAM company and every controller company designed towards the agreed-upon JEDEC standard.”); Polzin, Tr. 3973 (“JEDEC allows manufacturers to all design to a common standard and basically enables the commodity marketplace. Everybody is designing compatible parts at the lowest possible cost competing on manufacturing cost.”); Sussman, Tr. 1324 (“we have no choice, we must standardize the part so it will fit within the consumer’s application”) and 1327-28 (“if the part is standardized, [customers] can buy it from multiple sources, they have options, and in that there are multiple sources . . . So, often the customers will be very hesitant to design a part into their system that is not standardized. They want more than one vendor to be able to provide it to them.”); G. Kelley, Tr. 2387-88 (DRAM “must be available for many suppliers, and it must be interchangeable from those suppliers”); Becker, Tr. at 1152-1153 (“Our customers, customers like Dell, IBM, Compaq, they’re interested in buying DRAM models or components from...[Infineon’s] parts or Samsung’s parts or Micron’s part and use them interchangeably, and

through the standards process, they get that benefit.”); Rhoden, Tr. 296 (“Essentially what they're asking for is they want interchangeability where they can get it from multiple places, get the same thing from multiple places. It gives them a great deal of advantage in the market.”) and 298-299 (“Q. Why do the customers want standardization? A. Well, they -- frankly, they like to have a broad customer supply base so they can pit one supplier against the other and get the lowest possible price”); Williams, Tr. 763 (“Their customers are mainly computer customers who require that they are able to buy products from multiple sources and that these products interoperate, and JEDEC is the body that sets those standards by which there are interoperability and everybody has, in essence, the same part based upon the JEDEC standard”) and 823 (“customers were very concerned, like they always are, to ensure that you've got multiple sources and that they're not locked into a proprietary product where then you can charge whatever you want. They want to make sure that there's a plentiful supply and that . . . they can get it from everybody.”); Williams, Tr. 763 (“for Micron, they make memory products that are used in the industry. Their customers are mainly computer customers who require that they are able to buy products from multiple sources”); Gross, Tr. 2305 (“[G]enerally industry standard material is made in the highest volumes, which enables the most competitive costs and price.”) and 2306-2307 (“all of the DRAM manufacturers would strive to meet those standards and produce product that aligned with those standards.”), 2307 (HP procures DRAM from all of the largest DRAM manufacturers in the world.); Lee, Tr. 6859 (“[I]n our business, we have to have perfectly substitutable products from other suppliers, so there needs to be multiple sources of the same part.”); Polzin, Tr. 3943-44 (“It was crucial that we had a common standard that would allow interoperability”); Bechtelsheim, Tr. 5789 (“the primary concern was that JEDEC was in fact able to develop a standard that was suitable for manufacturing of identical parts by all the memory manufacturers”), 5863-64; Farmwald, Tr. 8296 (“[Interchangeability is] very important to the DRAM customers”); Heye, Tr. 3641 (“because the volume of memory is so great, Apple thought it was very, very important to have multiple suppliers”); Goodman, Tr. 6013 (“we try and avoid a single-source scenario”).

117. Customers benefit from the presence of multiple DRAM suppliers because competition between the suppliers ensures customers will receive lower prices for DRAM. (Bechtelsheim, Tr. 5762 (“it was well-understood that in a competitive market where multiple manufacturers make essentially the same type of component that the cost to us as a customer would be significantly superior and there would be a lot more cost pressure on the manufacturers themselves to optimize the manufacturing of their components.”); Polzin, Tr. 3973 (“JEDEC allows manufacturers to all design to a common standard and basically enables the commodity marketplace. Everybody is designing compatible parts at the lowest possible cost competing on manufacturing cost.”); Peisl, Tr. 4409 (A very simple economic law says: The more suppliers you have, the lower you can drive the cost.”); Gross, Tr. 2307-2308 (“When you have several sources, they, of course, will compete for business, which generally produces a lower price.”); Rhoden, Tr. 298-99 (customers “like to have a broad customer supply base so they can pit one supplier against the other and get the lowest possible price.”); G. Kelley, Tr. 2388); J. Kelly, Tr. 1791 (“any company wishing to comply can and can develop product to the standards, and that

tends to mean more sources of supply”; this means “more competition in the manufacture of product,” which “tends over time to drive the price down”).

118. Customers benefit from the presence of multiple DRAM suppliers because having multiple sources reduces the risk of losing supply. (Gross, Tr. 2308 (“[A]ny change to our business or the DRAM supplier’s manufacturing would impact directly the other partner, and that’s,... a fairly unacceptable risk, since its not a necessary risk to take.”); Landgraf, Tr. 1692-93 (“We also had assurance of supply going forward. . .many of HP’s products are supported for a five to seven, maybe ten-year product life cycle, and in some cases that exceeds the manufacturing cycle for some suppliers . . .by having a standard, we would have a greater chance of having continuity of supply for any time in production or even in support life.”); Rhoden, Tr. 298-99 (“they also have the capability that if one supplier disappears or whatever, they still have a continuous supply. So, standardization is something that they. . . basically demand.”); Heye, Tr.3641 (“availability is very, very important and when you have a commodity like memory, you know if you don’t get the memory, you can’t chip your Mac...you’re out of business. And because the volume of memory is so great, Apple thought it was very, very important to have multiple suppliers.”)).

2. Benefits to DRAM Suppliers.

119. Standardization in the DRAM industry benefits suppliers by providing a high degree of assurance that there will be a demand for product and by allowing suppliers to leverage their design costs over a number of designs. (Rhoden, Tr. 296-298 (“there’s a great deal of investment, billions of dollars, that go into the creation of factories and designs that are necessary to produce DRAM, and the supplier gets a large demand, because working with the customer inside an area like JEDEC, because you’re working together with your customers and with the supply base, and when everyone agrees, then they have essentially an automatic market . . . they have basically a presold customer base just by complying and working with the standard.”); Appleton, Tr. 6275 (“ . . . when the whole world can design to a standard, then it has a benefit . . . to those of us that manufacture, because we all then cumulatively put resources towards bringing that product to market and it’s more cost-effective because we’re able to know what’s going to be consumed in the marketplace in aggregate”); Macri Tr. 4596 (Discussing CX0378 at 1 he states “[O]ur goal was to create a broad enough standard to be used by as many people as possible in the world, so it made sense that if that was our goal, we would have as many people attend the meeting from as many different, you know, applications of DRAMs as well as builders of DRAMs, everything surrounding DRAM, so that the final standard would have, you know, the consensus of the world, so that it would become widely adopted and used throughout the world.”) and 4620-21 (Discussing CX2315, he states “[U]sually in the DRAM world, there is only one choice. You know, it’s not a matter of what; it’s a matter of when. So, users, they can plan their transition based on their own -- you know, their own internal decision-making process, plan their transition to meet their own business needs. The suppliers, they know making the investment up front is going to be realized, because they know the users will eventually move

over. It may not all be at once, but over a period of time, they can count on the market slowly building up. In this particular case, there were two choices, and it was very unclear which way the world would go.”); Rhoden, Tr. 298).

120. One way that standardization in the DRAM industry helps to assure a demand for new DRAM standards is by having an open standard setting process that involves all interested firms. (Macri Tr. 4596 (Discussing CX0378 at 1 he states “[O]ur goal was to create a broad enough standard to be used by as many people as possible in the world, so it made sense that if that was our goal, we would have as many people attend the meeting from as many different, you know, applications of DRAMs as well as builders of DRAMs, everything surrounding DRAM, so that the final standard would have, you know, the consensus of the world, so that it would become widely adopted and used throughout the world.”)).

121. Standardization benefits suppliers by allowing them to save resources on development. (Appleton, Tr. 6304 (standardized products benefit manufacturers because “we can look at all of that in a cumulation and save on resources . . . that would otherwise be required to come up with a device”)).

H. A Variety of Factors Affect the Selection of Technology to be Included in DRAM Industry Standards.

1. Timeliness.

122. Standard setting at JEDEC is time-consuming. (Peisl, Tr. 4453 (“JEDEC is traditionally a very slowly moving consortium, and there's a reason for that, because there's so many companies involved, it's basically the whole industry that produces parts for the PC and the laptop and the server business, so to try to reach consensus at JEDEC, based on my experience, have been incredibly hard and tough.”); Macri, Tr. 4607-608 (“The design process is long.”)).

123. Industry participants consider time to market an important factor in developing standards. (Bechtelsheim, Tr. 5797 (“for example, if the synchronous DRAM did not have a completed spec, we would chose the previous memory technology. . . we would not be able to take advantage of the performance characteristics of the next-generation synchronous DRAM”) and 5803 (“Sun itself did not have a strong view of what exact features the part should have as long as it would meet the cost, complexity and timely completion of the standard.”); Rhoden, Tr. 299-300 (“You can't really wait until after you develop something and then decide to standardize it. You have to move in real time at the time that technology is being developed to create the standards. . . there is an urgency in the development of standards, because if you delay and if you wait too long, then sooner or later someone else will replace and do the job for you.”); Heye Tr. 3747 (“anything that impacts time to market . . . would put us at a competitive disadvantage”); Macri, Tr. 4600 (“Time to market is extremely critical in this world”); CX0302 at 3 (“Delay is NOT a viable market option.”); JX0027 at 12 (“Concern about JEDEC taking too long to

produce a standard was mentioned as a reason not to pursue a standard within it.”)).

124. The potential impact on time to market is a factor that influences the decisions of JEDEC members regarding what technologies to include in a standard. (CX2383 (“We are willing to make compromises if necessary to reach a quick resolution on a standard”); Bechtelsheim, Tr. 5794-95; Lee, Tr. 6635 (Although it preferred the SDRAM-Lite device, Micron “agreed in the interests of schedule to just go ahead and accept the full-feature proposal.”) and 6683 (“Our preference was still not to have [strokes], but our action was to -- to go along with the committee in general with this compromise, because there was -- because of these differences of opinion, it was causing some delay in the standardization process.”)).

2. Cost.

125. The potential cost of manufacturing and implementing a prospective technology is a factor that influences the decisions of whether a particular technology is included in a standard. Industry participants often are willing to forego performance advantages in exchange for lower cost products. (CX1708 at 2 (Richard Crisp writing “[Compaq] didn’t particularly seem to care if the SDRAMs had 1 or two banks so long as they didn’t cost any more than conventional DRAMs.”); CX2383 (“Since we are very cost conscious we are willing to drop features that add too much cost or complexity”); CX0711 at 34 (Richard Crisp writing “They want cheap, cheap, cheap”); JX0027 at 13 (“The Committee noted they wanted highest performance and lowest price SDRAM.”); CX2777 (“[T]he age old rule for DRAMs still apply. Customers will take as much performance as we can give them for absolutely no added cost over the previous technology. They will not pay extra for increased DRAM performance.”)).

126. In order for a new memory technology to achieve high volume, it must be price competitive with the previous technology already in high volume. (MacWilliams, Tr. 4805 (“[W]e were concerned that with any new memory technology, for it to achieve high volume we need to be price competitive with the previous technology that was already in high volume.”); CX2370 at 2 (“Must be within 5%”); CX0034 at 4 (“Dallas Task Group Conclusions Mr. Kelley summarized the presentations of 7.2 and 7.3 and presented some of the consensus views of the Dallas meeting: 1) To be cost effective sync DRAM must cost no more than 5% over conventional DRAMs for many applications”); CX0711 at 1 (Richard Crisp writes: “Desi added that if the SDRAM doesn’t cost less than 5% more than standard DRAM they will not be used.”); Tabrizi, Tr. 9082 - 83 (“For any product, if it doesn't become a low cost to manufacture, it never becomes reality. The issue is cost, cost, cost.”)).

127. Changes in the DRAM industry tend to be incremental or evolutionary in nature, with only a handful of changes from standard to standard. (Rhoden, Tr. 408 (“[W]ithin JEDEC, we follow the process of evolutionary progress. So, there's some thousand things that go into the making of a particular DRAM, and we tend to change just a few, maybe a handful, maybe -- sometimes two or three, sometimes four or five, but that's the typical process, is we just evolve

one to the next, to the next, with as little changes as possible, because it's much easier to bring the whole industry along when you make minor changes.”); Sussman, Tr., 1362 (“The customer base does not really want to jump ahead to something new and different.”).

128. Evolutionary, as opposed to revolutionary, changes serve to minimize cost, and to ease the introduction of new DRAM standards. Bechtelsheim Tr., 5835 (“Because if it's not broken, we don't fix it. In other words, unless there's an overarching reason to make a change, people tend to do the same as they did previously....Well, it takes time to verify, validate, prove new memory components at the system level, which is quite extensive. So yes, there's a significant cost in qualifying new types of memories.”); Appleton Tr., 6297 (“Sure, Micron's preference, of course, is to go evolutionary, because it's more stable for us, it's less costly for us, and we can more easily plan for it.... Well, customers in general would prefer to have an evolutionary process as well. It -- the changes don't just affect us, they affect the people we are selling the product to, and when you start talking about reliability of the device, reliability of the technology platform, reliability of the supply, it's also a much easier transition for them.”); Peisl, Tr. 4378 (“JEDEC wanted to do an evolutionary step going from SDR to DDR, evolutionary in order to keep the costs down in the industry because it affected much more than the DRAM design, . . .”).

3. Need.

129. A technology might not be standardized if the technology's performance improvements are ahead of their time from the standpoint of what customers demand. For example, JEDEC began considering a form of dual-edged clocking in the early 1990s but did not adopt it until the DDR standard because the industry did not require the additional performance that dual-edged clocking could provide. (Rhoden, Tr. 462-63 (“[W]e talked about dual edge clocking, and at the time . . . we actually decided to postpone implementation of that until a later date. . . Many of those wound up in DDR ultimately. . . We said, well, since we don't need it at this time, perhaps we don't need to expend the effort.”); Kelley, Tr. 2515 (“[W]e decided as a group that we could meet the requirements of the high-performance systems for the next-generation DRAM without needing a double-edged clock for that doubling of the performance and that we would reconsider the double-edged feature in the next generation.”); CX0742 at 4 (“The implication here is that customers are willing to leave performance on the table in exchange for having lower cost systems.”)).

4. Uncertainty.

130. At the time that the technologies are selected for incorporation into a standard, not all of the facts are known. Industry participants must make decisions on what technologies to include in the standard based on predictions with respect to the likely future performance, implementation difficulties and manufacturing costs. (Wagner, Tr. 3841 (“The decision was made to support both SDR SDRAM and DDR SDRAM so that if DDR didn't show up, we still

had a fallback plan and could still ship our product on the market”); MacWilliams, Tr. 4884 (“Because server design cycles are longer than desktop, [OEM’s] were going to make some decisions in terms of what they were going to build for a much longer time frame.”); Gross, Tr. 2296 (chose DDR because it “appeared to us to be the next mainstream high volume memory technology.”).

131. The predictions of industry participants are not always correct. For example, when Intel first evaluated DDR SDRAM in 1996 it did not appear to Intel employees that it would work. (MacWilliams, Tr. 4881 (“so when we looked at it back in the 1996 time frame, it didn't look like it would work ...”). Even in 1999, when Intel began to consider using DDR for use in servers, it was believed at Intel that DDR could not be used in main memory for personal computer systems. (MacWilliams, Tr. 4881-82). However, by September of 2001, Intel was working to deliver robust DDR platforms for all Intel architecture CPUs. (RX-1761 at 16).

132. Paragraphs 132 - 199 are unused.

II. JEDEC Is An Industry Organization for Developing Consensus-Based Standards.

A. The Founding and History of JEDEC.

200. The formal name of JEDEC is the “JEDEC Solid State Technology Association.” (J. Kelly, Tr. 1750-51).

201. JEDEC was founded in 1958 and originally named the “Joint Electron Device Engineering Council.” (CX0302 at 10; *see also* J. Kelly, Tr. 1773-74 (“JEDEC has been active within an EIA organization under the name JEDEC since approximately 1958, and under other names with slightly different functions for a number of years prior to that, probably dating back to the 1940s.”)).

202. Between 1991 and 1996, JEDEC was an entity within the Electronic Industries Association Engineering Department. (J. Kelly, Tr. 2075). EIA is alliance of organizations engaged in the electronics industry in the United States. (J. Kelly, Tr. 1750 (“EIA is a broad-based association that represents the electronics industry in the United States, and it engages in a variety of different activities in support of that industry.”); CX0302 at 28).

203. In 1998, EIA changed its name to the Electronic Industries Alliance. (CX0302 at 11). In 1998, JEDEC became a separate division of EIA. (CX0302 at 11).

204. In 1999, JEDEC became independently incorporated. (CX0302 at 11). Both EIA and JEDEC are headquartered in Arlington, Virginia. (J. Kelly, Tr. 1751).

B. The Purpose of JEDEC.

205. JEDEC develops standards for semiconductors and solid state products. (J. Kelly, Tr. 1751 (“JEDEC is focused on standard-setting in support of the industry sector that it represents, which is semiconductors and solid state products.”)).

206. The purpose of JEDEC is to create consensus-based standards. (CX2767 at 1 (“JEDEC exists because of an industry need for standardization.”); CX0035 at 14-15 (“The work we do on the JC-42.3 DRAM committee continues to approach a design by committee.”); Becker, Tr. 1152 (JEDEC “tries to build a consensus across the industry to produce a specification or an industry standard [to which] everybody manufactures and conforms their products.”); J. Kelly, Tr. 1784 (“In every instance, our standards have to be based upon a consensus of the formulating committee and a consensus of the board . . . formerly the JEDEC Council, indicating that they agree with the content of the . . . standard”); Landgraf, Tr. 1685 (“JEDEC is a standardization body that . . . brings together memory -- or electronic component manufacturers as well as customers using those devices to formulate common standards that can be used by manufacturers and be understood by the users.”); Polzin, Tr. 3946-47 (“JEDEC was

the natural forum and process for resolving the numerous differences.”); Lee, Tr. 6682-84 (discussing differing views on using DLL in DDR SDRAM)).

207. JEDEC standards ensure uniformity and reliability in products. (CX0419 (“uniform terms and definitions, common packages [and] interchangeability of logic [and] memory” to the industry); J. Kelly, Tr. 1791; Bechtelsheim, Tr. 5781 (“Well, the purpose was to develop standards that could be used by all memory manufacturers to manufacture devices that had the same functionality and thus could be used as a multivendor, multistandard device from multiple manufacturers.”); Polzin, Tr. 3972 (JEDEC “defines standards that multiple manufacturers can design to have interoperable parts.”); Calvin, Tr. 994 (“the expectation is when you buy something in the industry and you plug it into your system, that it's supposed to work. And so that's the purpose of the standardization body to get agreement across the industry members in terms of what the aspects of that standard are going to be.”)).

208. JEDEC standards are procompetitive because they lower costs and ensure broader participation in the market. (CX0419 (“What JEDEC standards mean to the industry is lower price and wider supply, consistent quality and reliability, uniform terms and definitions, common packages, interchangeability of logic, memory, etc.”); J. Kelly, Tr. 1790-91 (“Because it is an open standard, any company wishing to comply can and can develop product to the standards, and that tends to mean more sources of supply, and because there’s more competition in the manufacture of the product, it tends over time to drive the price down for the benefit of the supply chain as well as OEMs and end user and in many cases consumers.”); Polzin Tr. 3973 (“JEDEC allows manufacturers to all design to a common standard and basically enables the commodity marketplace. Everybody is designing compatible parts at the lowest possible cost competing on manufacturing cost.”)).

C. How JEDEC Is Organized.

1. Membership.

209. A company becomes a member of both JEDEC and EIA by completing and submitting one application and paying dues. (CX0601 (Rambus application); J. Kelly, Tr. 1801 (“one becomes a member of JEDEC by filling out a membership application and paying dues.”); 1801-02 (Since at least 1990, when one becomes a member of JEDEC, one automatically becomes a member of EIA.); Rhoden, Tr. 294-95 (“Companies become a member of JEDEC by paying dues.”); CX0208 at 7 (“Eligible organizations can become members of JEDEC by joining the EIA Solid State Products Division or by joining JEDEC directly,” and paying annual dues.)).

210. During the 1990s, JEDEC had approximately 250 member companies who sent approximately 1800 individuals to participate in approximately 50 committees. (J. Kelly, Tr. 1774-75).

211. JEDEC membership is open to broad array of companies and individuals. (CX0208 at 6 (“[a]ny company, organization, or individual doing business in the United States that itself or through a related entity manufactures electronic equipment or electronics-related products, or provides electronics or electronics-related services, shall be eligible for membership” in JEDEC.); CX0203A at 4 (members can include “any and all companies having a relevant commercial interest within the respective jurisdiction of the committees.”)).

212. JEDEC members represent a broad cross-section of the semiconductor supply chain. (CX0302 at 8 (members include chipset companies like Ali and VIA, microprocessor companies like AMD and Intel, packaging companies like Amkor, computer memory module companies like Celestica, memory suppliers like Elpida, Hynix, Samsung, Micron and Infineon, OEM companies like HP and IBM, networking companies like Lucent and cell phone companies like Motorola.); JX0028 at 1-3 (list of members attending and not attending); Rhoden, Tr. 293.).

213. JEDEC’s membership includes companies from around the world. (Rhoden, Tr. 294 (noting companies from Korea, Germany, Taiwan and Japan companies.); CX0302 at 8.).

214. Membership entitles companies to attend meetings, receive minutes, vote, and receive copies of standards and other publications. (J. Kelly, Tr. 1805-06 (JEDEC “members can attend any meeting. They can receive meeting notices. They receive copies of minutes of meetings. They have an opportunity to vote on a one-company/one-vote basis. They have the right to . . . receive copies obviously of standards and other publications that are distributed generally by JEDEC to members”)).

215. During the early and mid-1990's, JEDEC minutes were regularly circulated to all members. (Crisp, Tr. 3139 (“Q. Now, Mr. Crisp, JEDEC regularly circulated minutes from the meetings. Isn't that right? A. I think that's correct.”)).

216. Attendance by non-members is limited to one meeting. (J. Kelly, Tr. 1805-06).

217. A member can withdraw from JEDEC either by letter or by not paying dues for an extended period of time. (J. Kelly, Tr. 1808 (“A company can withdraw from JEDEC by either submitting a letter indicating their wish, their desire to withdraw, or by not paying their annual dues.”), 1808-09 (“we do not drop member companies for nonpayment of dues until around September 1, and the reason for that is that the nonpayment of dues is equivocal . . . , and it's not at all unusual for member companies to be six months late in paying their dues. We don't ever drop them without knowing to a reasonable degree of certainty that they don't intend to pay their dues.”)).

218. Members who are late paying their dues still are entitled to attend meetings, vote, and receive minutes. (J. Kelly, Tr. 1809-10).

2. Management.

219. Prior to 2000, the JEDEC Council was the governing body of JEDEC. (J. Kelly, Tr. 1768). Today, the JEDEC board of directors is the governing body of JEDEC. (J. Kelly, Tr. 1770).

220. The JEDEC board of directors consists of approximately 22-27 people. (Rhoden, Tr. 287). The members of the JEDEC board of directors are representatives of the DRAM industry, from electronics and semiconductors companies. (Rhoden, Tr. 287).

221. The chairman of the board of directors is elected by JEDEC members. (Rhoden, Tr. 286). The JEDEC chairman is not compensated by JEDEC. (Rhoden, Tr. 287-88). The JEDEC chairman is responsible for “the business aspect of JEDEC, trying to make sure that we [JEDEC] have office space, staff, relationships with other organizations, and to make sure that we take care of the business aspects of the corporation itself.” (Rhoden, Tr. 286-87).

222. Desi Rhoden is the current Chairman of the JEDEC board of directors. (Rhoden, Tr. 283).

223. The president of JEDEC is responsible for supervising the JEDEC staff, managing the JEDEC budget, and implementing the policy directives of the JEDEC board of directors. (J. Kelly, Tr. 1754). Prior to 2000, the JEDEC president did not have any supervisory responsibilities for JEDEC staff. (J. Kelly, Tr. 1754-55).

224. John Kelly is the president of JEDEC. (J. Kelly, Tr. 1750-51).

225. The EIA general counsel is “the legal counsel for all of the operating units within EIA, including JEDEC.” (J. Kelly, Tr. 1754).

226. The EIA general counsel is the person responsible for interpreting EIA rules and the JEDEC rules, including the JEDEC patent policy. (J. Kelly, Tr. 1813-14 (“a number of questions do arise from time to time about the patent policy of EIA and JEDEC, because that is part of -- and a very important part -- of the ground rules for the engineering function.”), 1939 (“Q: . . . when either the staff or the committee leadership have interpreted EIA or JEDEC rules differently than you, whose interpretation controls? A: Mine does.”); Sussman, Tr. 1348 (“Q. If a participant at JEDEC had raised any questions, who would you refer that person to for more precise answers on the patent policy? A. JEDEC legal counsel. None of us are lawyers.”)). Cf. (J. Kelly, Tr. 2057-58 (Rambus never contacted EIA Legal Counsel concerning questions of interpreting the patent policy)).

227. John Kelly has been the General Counsel of EIA since 1990. (J. Kelly, Tr. 1754).

228. Today, JEDEC employs a staff of ten persons to facilitate the meetings of JEDEC committees. (J. Kelly, Tr. 1792-93). During the early to mid-1990s, the size of JEDEC's staff was "considerably" smaller than the current size. (J. Kelly, Tr. 1795).

229. JEDEC's current budget totals \$2.2 million, approximately half of which covers salaries. (J. Kelly, Tr. 1800).

3. Committees and Subcommittees.

230. JEDEC is organized into committees and subcommittees. (Landgraf, Tr. 1687 ("below the council are a series of committees which [the council] approve to exist")). Each committee or subcommittee has a chairman. (J. Kelly, Tr. 1794 ("The members of each committee and subcommittee elect from their membership a chairman and a vice-chairman.")).

231. The JC-42 committee is concerned with developing standards for the memory products. (Williams, Tr. 765-66 (The JC-42.3 membership consists of "[a]lmost all of the DRAM memory companies, SRAM memory companies, logic companies, customers of memory, as well as interconnect companies, such as socket manufacturers," and testing companies.); Rhoden, Tr. 288 (JC 42 is the committee responsible for developing standards relating to memory devices.)).

232. The JC-42 chairman is responsible for coordinating all the activities in the JC-42 committee and subcommittees, including the scheduling of meetings. (Rhoden, Tr. 288).

233. The JC-42 committee had several subcommittees focusing on particular specialized subject matters. (J. Kelly, Tr. 1769; Rhoden, Tr. 285 (JC-42 included subcommittees devoted to DRAM (42.3), SRAM (42.2), memory modules (42.5), flash memory and other types of programmable devices)).

234. JEDEC's JC-42.3 committee develops the predominant standards relating to dynamic random memory ("DRAM") products. (Peisl, Tr. 4381 (JEDEC subcommittee JC 42.3 "standardizes the DRAM interfaces and the packages of DRAM generations."); Rhoden, Tr. 283-84 ("JEDEC is the place where industry standards are set for the DRAM" industry.); Krashinsky, Tr. 2773 (JEDEC sets memory standards for the industry); (CX2107 at 23 (Oh FTC Dep) ("JEDEC is the committee which standardize all the standard products in the market."); MacWilliams, Tr. 4910-11 (Intel PC100 specification included programmable CAS latency and programmable burst length because features were already in the JEDEC specification.)).

235. In late 1991, approximately 40-50 companies were represented on the JC-42.3 committee. (Rhoden, Tr. 340-41; JX0010 at 1-2 (minutes listing approximately 42 companies as members of JC-42.3)).

236. The JC-42 committee and its related subcommittees typically meet at least four times per year. (Rhoden, Tr. 340 (“there are four regular meetings, once a quarter, and depending upon the workload for the committee, the amount of work that we have to do, we often times hold special committee meetings in between meetings, and so somewhere between four and eight. In times of high activity, we will have eight meetings per year and almost always have five.”)).

237. Minutes of JC-42 committee and its subcommittees are prepared by, Ken McGhee, a staff person. (Rhoden, Tr. 327).

238. The minutes of JC-42 and its subcommittees record the key decisions that are made during the standard development process, including motions and votes. (Rhoden, Tr. 327-28).

D. How JEDEC Standards Are Made.

239. The standard development process begins with discussions among the participants at a JEDEC meeting concerning subjects that members may feel should be considered for standards. (Rhoden, Tr. 406-07).

240. Typically, standardization at JEDEC involves a series of presentations. (CX0302 at 23; Williams, Tr. 772-73 (“[I]n order to get a point or feature to ballot, it required a first showing, which would happen at one meeting. You would then go to a second showing at the second meeting. You could then at the end of the second showing request that the item or the ballot -- the item be sent to ballot. The ballots would be issued. They would count the ballots at the third showing.”); Rhoden, Tr. 406-07 (“Our procedure that we follow inside of the JC-42 committee is we typically have a first presentation, then followed by -- after some review, follow that by a second presentation.”)).

241. Standardization proposals typically receive an item number after the first presentation. (Calvin, Tr. 1025).

242. A presentation might generate other proposals to solve the same problem. (Rhoden, Tr. 406-07 (“When someone has an idea that they'd like to bring into the committee, they will bring in a presentation, and then we will make presentations, and based on the presentations . . . the committee may generate other discussions and may also generate the development of other presentations for that matter.”); CX0711 at 2 (Crisp of Rambus discussing corrupting SynchGDram proposals: “Desi made a comment at the end of the meeting that was in effect request for some of the folks to withdraw their proposals. He reminded folks that there are a lot of variants being proposed; VRAM, SGRAM, frame buffers on a chip, etc.”)).

243. JEDEC entertains a number of proposals by members when working toward a standard for a new device. (Rhoden, Tr. 415 (“[W]hen we're working on a particular device or

whatever, there will be proposals that are made that come from usually a number of different companies. Sometimes multiple proposals or multiple ideas, if you will, come from a particular company, but more often than not, it comes from a variety of companies. So, you will have several different proposals that will be made inside JEDEC as to what path we should take for the next improvement cycle, if you will, of what we're working on”).

244. JEDEC members decide which of these ideas to pursue. (Rhoden, Tr. 415-416 (“Well, the differences of opinion are something that people have to investigate to see if particular -- if the particular proposals are viable or if they -- it usually winds up being that engineers themselves come up with the ideas, so they're almost always reasonable ideas, and it's just a question of then deciding which path they're going to take.”)).

245. In some cases, discussions of possible features generate a survey ballot that requests the members to give their views concerning different solutions. (JX0028 at 6 (“SDRAM Feature Survey Ballot”); Rhoden, Tr. 481 (“everything that shows up in a survey ballot is either from a presentation or from an earlier discussion that takes place in JEDEC.”), 516 (survey ballot is “a collection of all of the topics that we had been discussing for some time, usually within JEDEC, and at some point we would need to make decisions, basically get a sense of the committee to see what path we would take moving forward.”); Calvin, Tr. 1032 (“I also remember discussion before the survey was actually issued. Because this was an attempt to get a cross section from all the members. . . this survey was a result of trying to capture the top most things that were necessary for SDRAM to continue to evolve. This had been discussed at numerous meetings before, and many inputs were coming in”)).

246. Survey ballots are official JEDEC work. (Landgraf Tr. 1716 (“in a JEDEC committee, there's a lot of official work that is documented, and survey ballots are considered to be official work.”); Sussman, Tr. 1419 (“Q: Does the patent policy apply to a survey ballot based on your experience at JEDEC? A. And I've already answered that basically yes, as soon as possible in the discussion, we'd like to know.”)).

247. Following the conclusion of the second or subsequent presentations, the committee decides if it wants to create a ballot to vote on the substance of a proposed standard. (Rhoden, Tr. 406-07 (after the second presentation “we would decide if we want to have a ballot or not have a ballot.”)).

248. JEDEC participants often had significant differences of opinion concerning the development of a standard. These differences of opinion drove heated debates concerning the merits of the various solutions to the technical challenges facing the JEDEC participants. (E.g., CX0711 at 14 (Regarding various proposals for SDRAM modules Crisp writes: “This was argued quite a lot . . . There was much wrangling etc and the conclusion is that they will all huddle once again to work out the details”), 33 (Regarding an HSTL ballot Crisp writes: “Another example of the flailing at JEDEC . Approximately three and a half hours was spent

arguing about the resolution of the “No” ballots. The companies voting no are adamant about their objections and it appears there is basically an impasse”), 47 (Regarding a various pinout proposals Crisp writes: “The same issues came up as well as the usual pin naming and ‘why don’t you move pin xxx to yyy location.’ Usually someone out in the audience seems to have some overwhelming reason why a particular pin should be in a particular position. Many times it really does not matter, but sometimes it does. *But always there are strong opinions!*”) (emphasis added); CX0680 at 1 (Billy Garrett email from the September 1992 JC-42.3 meeting "This is not to say that there are not active, heated discussions on features and functionality. There areNEC tried to introduce a second showing . . . but even the request for balloting was turned down due to several technical objections."), 2 ("Precharge and Autoprecharge were not resolved. Lots of disagreement on the effects on banks, and how autoprecharge will be done."); Rhoden, Tr. 434-35 (“if you give ten engineers a problem, you’ll probably get 12 or 14 solutions, and the same is true inside the discussions inside the committee. People were proposing a number of other approaches to the same type of thing.”); Sussman, Tr.1380 (“I had a lot of arguing to do to get the degree of programmable features into the part.”)).

249. From time to time, ballots failed or was put on hold in the JEDEC committees because the committees did not reach a consensus. (JX0012 at 6 (“There was some discussion on the package size, but no consensus was gained. The ballot failed.”), 12 (“ATT moved to put the ballot on hold until the two sided high pin count package issue was resolved. . . . Motion passed”); JX0019 at 10 (“In conclusion, NEC wanted to table the ballot. Fujitsu made motion to send it to Council. Motion failed for lack of a second. Hitachi moved to take it off hold and send this ballot back to Committee. Apple seconded. The vote was unanimous.”); JX0026 at 5 (“Motion to send to Council by Cypress, Xerox seconded. The vote was 5 yes, 8 no. Motion failed. The ballot was put on hold.”)).

250. Ballots also may be put on hold for other reasons, including unresolved patent concerns. (G. Kelley, Tr. 2464-66 (“Because patent issues are almost terminal for a ballot to pass. If a patent issue comes up, unless it's able to be resolved at the meeting, it will -- the ballot will be put on hold or it will fail.”)).

251. On other occasions, after long debate, ballots passed because they represented compromises that satisfied a majority, but not all, of the members. (JX0026 at 6 (“Micron: Vss and Vdd pins at the end of the package are not that useful. Vddq and Vssq can be organized better around the Dqs. . . . Committee responded to Micron that this has been discussed for over a year. There are advantages and disadvantages of both implementations and this satisfies most.”)).

252. If it preferred, a committee could pass items individually but place the individual items on hold until an entire list of related items that were needed to define a single standard was complete, and once that group of ballots was complete and passed, then together the committee could motion them to go to council for publication. (G. Kelley, Tr. 2554 (discussing the process

for standardizing SDRAM); see also, e.g., JX0010 at 8-9 (V-PACK ballot failed due to patent concerns)).

253. After a JEDEC committee approves a standard, the proposed standard is sent by a ballot to the JEDEC board of directors, which then has to again by a consensus approve the ballot in order for the proposal to become a JEDEC the standard. (J. Kelly, Tr. 1785 (“Once the committee approves a standard . . .the proposed standard is sent by a ballot to the board of JEDEC, which then has to again by a consensus approve the ballot to adopt the standard.”); Rhoden, Tr. 406-07 (“if the ballot were to pass [the committee], then we would move that ballot perhaps on to the final review process, which would be a procedural review to make sure that due process was followed at -- at that time it was the JEDEC Council, now it's the JEDEC board of directors.”)).

254. JEDEC’s consensus-based process means that the board of directors will consider any committee votes that were cast in opposition to the proposed standard. (J. Kelly, Tr. 1786 (“[t]he board will always discuss the fact that there are negative votes, particularly if there are unresolved negative votes.”)).

255. JEDEC’s consensus based process often requires years in order to adopt a new standard or change an existing standard. (CX0302 at 22 (“Complete process may take 2-3 years”); Polzin, Tr. 3977 (“JEDEC is open to any and all parties, so any and all parties have an opinion and can contribute or delay, or everybody has a vote, so it's not always the most straightforward thing to get a technical specification through. It's sometimes long, laborious, and you have to argue your points endlessly, probably much like Congress down the road, but it's successful and it works.”); Peisl, Tr. 4453 (“JEDEC is traditionally a very slowly moving consortium, and there's a reason for that, because there's so many companies involved, it's basically the whole industry that produces parts for the PC and the laptop and the server business, so to try to reach consensus at JEDEC, based on my experience, have been incredibly hard and tough. In the last decade, essentially there were only two standards that emerged for SDR and DDR”)).

256. During the standard development process, JEDEC prohibits members from public discussion of committee deliberations. (G. Kelley, Tr. 2519 (“We specified that members were only to talk about JEDEC work within their companies.”); CX0035 at 16)).

257. During the 1990s, JEDEC standards became more detailed. (CX0035 at 14-15 (“The work progressing on Synchronous DRAMs. . . is pushing our JC-42 scope- ‘. . . development of technical information and standards pertaining to pinouts, operational characteristics, test parameters, characterization and registration formats. . . If we do not do this, then we cannot create common parts that are plug compatible at 100Mhz operation and above. . . So, in addition to the design framework, we now are filling-in the details with timing diagrams that will impact, in a greater way, the chip design.”); G. Kelley, Tr. 2390 (“the level of technical

issues that we were dealing with [in 1992] on my DRAM pass-through was much greater than we had handled historically.”)).

E. Why Companies Belong to JEDEC.

258. Formal standardization in the DRAM industry benefits the entire industry by ensuring quality and reliability in the products. (Prince, Tr. 9016-17 (“when something comes for formal standardization, it has the review of peers throughout the industry. Everyone gets a chance to review it and make comment, and if there are good and bad features, they can be modified. And what ultimately comes out for the users in the industry is the most adequate device that the industry collectively can prepare.”)).

259. JEDEC is the most important standard-setting organization for DRAMs. (CX0035 at 14-15 (“This JEDEC standardization process creates the structure from which all DRAM designs begin. . . JEDEC is the fulcrum for DRAM standards in Asia, the Americas and Europe”); CX0419 (As of May 2000, “75% of the top 250 semiconductor manufacturers [were JEDEC] members, representing 80% of semiconductor sales. An estimated 90% of semiconductor standards in use are JEDEC standards.”); Rhoden, Tr. 283-84 (“JEDEC is the place where industry standards are set for the DRAM” industry); Prince, Tr. 9016 (“JEDEC is the primary standardization body for RAMs.”), 9021–22 (recalling only one RAM standard that was not formally standardized in either JEDEC or IEEE); Sussman, Tr. 1364; CX2773 at 9 (JEDEC standards are included in Micron’s internal “Designer’s Toolbox.” web application.); CX2334 at 25 (“Pros” of DDR include fact that it is an open standard); CX2297 at 79 (“DDR SDRAM . . . Strong Points. . . JEDEC standardization in 1997.”); CX0302 at 7 (JEDEC is the “World Leading technology standards association.”), 16 (“Global JEDEC standards usage has skyrocketed.”), 17 (“If you are not [at JEDEC], your competition may be deciding your future.”); Peisl, Tr. 4384 (“JEDEC's standards were the only source for our own specifications, meaning that . . . Infineon chip specifications were entirely directed towards the -- 100 percent compatibility towards the JEDEC specifications.”), 4386 (“If we wouldn't have produced a chip that would not comply to the JEDEC specification, it would have not been able to work at the PC, at the server, at the laptop platforms at HP, IBM and all our other customers because of noncompliance issues, nontechnical issues, and we essentially would not have been able to sell anything”); (CX2080 at 194 (Karp, Micron Dep.) (“JEDEC’s a bunch of competitors. They are not people that particularly like each other. *They are there because they have to be there* because it’s part of – it’s part of the business.”)).

260. JEDEC standards are very valuable to manufacturers. (CX0707 at 1 (Geoff Tate writes: “JEDEC is a bid deal to them [Samsung] because it [JEDEC] represents the big users.”); Peisl, Tr. 4384 (“JEDEC's standards were the only source for our own specifications, meaning that . . . Infineon chip specifications were entirely directed towards the -- 100 percent compatibility towards the JEDEC specifications.”), 4386 (“If we wouldn't have produced a chip that would not comply to the JEDEC specification, it would have not been able to work at the

PC, at the server, at the laptop platforms at HP, IBM and all our other customers because of noncompliance issues, nontechnical issues, and we essentially would not have been able to sell anything”); Bechtelsheim, Tr. 5790 (monitored JEDEC’s progress on SDRAM standard because “it was a prerequisite for, in my mind, for the memory manufacturers to actually produce and manufacture these JEDEC-compatible parts.”); Williams, Tr. 763 (Micron’s customers “require that they are able to buy products from multiple sources and that these products interoperate, and JEDEC is the body that sets those standards.”); (CX2107 at 23 (Oh, FTC Dep) (“JEDEC is the committee which standardize all the standard products in the market.”)).

261. JEDEC standards are valuable to customers because customers require competitive, effective devices with a competitive and reliable supply. (Landgraf, Tr. 1692-93 (“the utility of a [JEDEC] standard . . . is that from HP's perspective, we were a large user of memories, and we wanted to use the most competitive and most effective devices available, and we wanted them available from a number of suppliers. . . . So, we have a wide supply. We also have a competitive supply that -- the more suppliers you have, the better your selection is for -- and more competitive supply base you have. We also had assurance of supply going forward. HP -- many of HP's products are supported for a five to seven, maybe ten-year product life cycle, and in some cases that exceeds the manufacturing cycle for some suppliers, and so we -- by having a standard, we would have a greater chance of having continuity of supply for any time in production or even in support life.”); G. Kelley, Tr. 2387-88 (“The DRAM is the largest single semiconductor used in [IBM], and the DRAM is probably the one that we spent more money on than any other. One of the realities of the DRAM, because of its proliferation, is that it must be low cost. To be low cost, it must be available for many suppliers, and it must be interchangeable from those suppliers, which means I can plug a component out from one supplier and plug the component in from another and they work equally well.”); Heye, Tr. 3635-36 (“Q: Do you have an understanding as to why Apple chose to send a representative to the JEDEC memory committee? A: Yes. . . .in the early nineties, Apple was the largest consumer of semiconductors in the world outside of IBM. . . . So, when you're in that kind of volume in the '90s, you have got to ride the commodity curve. And by that I mean you have to ensure that your products, that is commodity parts, are using the parts that are the highest available lowest cost parts. . . . And so we had a person whose job was not only to be a member of JEDEC, but he would go literally around the world, I think at least twice a year, and talk to every memory vendor to understand the memory roadmaps.”), 3716-17 (“AMD's use of open standards is absolutely critical for success in the marketplace.”); Wagner, Tr. 3829 (“[nVidia] originally got involved with JEDEC, partially on request from memory vendors. We had -- we were making requests of them for certain features that JEDEC was trying to eliminate, they encouraged us to participate in JEDEC to ensure that those features didn't get dropped from the standards. So, we got involved at that point.”); Peisl, Tr. 4409-10 (understood from discussion with customers concerning JEDEC standards that customers “were looking essentially for two major features . . . multisourcing [and] . . . interoperability.”)).

262. JEDEC standards are valuable to third-party enablers. (Calvin, Tr. 999-1000

(“because of the standardization effort there, obviously anything that [Intel] wanted to use or make use of in the future, we wanted to be able to influence the direction, as well as to be able to understand what we would be getting as the part involved. So, [Intel] had a strong interest in knowing and being part of that development activity.”); Polzin, Tr. 3973 (“AMD views the JEDEC standards process as crucial to its business. JEDEC allows manufacturers to all design to a common standard and basically enables the commodity marketplace. Everybody is designing compatible parts at the lowest possible cost competing on manufacturing cost.”)).

263. Customers insist on buying only JEDEC-compliant parts. (Peisl, Tr. 4409 (“The customers wanted to ensure that their systems, their platforms and servers, laptops and desktops, were sold at the best price and the best delivery situation, so they were looking essentially for two major features. One was the multisourcing, which JEDEC is ensuring. Because of the specified interface, they make sure that you have several DRAM vendors and several other vendors because they're all working towards the same interface. And the second issue is the interoperability. They of course wanted to make sure that our parts work together with all the other components in the system.”); Becker, Tr. 1152-53 (“Q: Do you have an understanding as to why it is you only manufacture JEDEC-compliant products, DRAMs? A. My understanding is that that's all our customers are willing to buy. We talked about the DRAMs I manufacture as being a commodity product. Our customers, customers like Dell, IBM, Compaq, they're interested in buying DRAM modules or components from [Infineon], but not just [Infineon]. They want to be able to buy [Infineon] parts or Samsung's parts or Micron's part and use them interchangeably, and through the standards process, they get that benefit.”); Sussman, Tr. 1363 (“Q. Have you ever had any customer indicate to you that they would only accept a JEDEC-compliant part for a particular application? A. I think we have had some military programs that they were insisting in their documents that they needed to be JEDEC standard.”); Bechtelsheim, Tr. 5790 (monitored JEDEC’s progress on SDRAM standard because “it was a prerequisite for, in my mind, for the memory manufacturers to actually produce and manufacture these JEDEC-compatible parts.”); (CX2054 at 47-48 (Mooring, Infineon Dep.) (DRAM customers like Hewlett-Packard, Apple, and Sun told Rambus “we only use memories approved by JEDEC.”); CX2079 at 117-18 (Mooring, Micron Dep.) (DRAM customers like Sun, Hewlett-Packard, Apple, and Compaq told Rambus “we don’t use non-JEDEC standard memories”), 118 (“in the DRAM business, the only standard is JEDEC.”)).

F. Members of the Industry Understand the Importance of JEDEC.

264. Even Rambus recognized the importance of JEDEC. In 1996, shortly after it withdrew from JEDEC, Rambus considered initiating a standards-related organization that it would control called “REDEC.” (CX0902 at 1 (“We’d be responsive and open to their inputs, but it would be us making the real decisions”), 2 (“Get them away from Jedec and participating in our ‘JEDEC.’”); CX0903 at 1 (“This is about pacification of our partners, pure and simple.”)).

265. Although Rambus wanted to give the group the veneer of an open standards

organization, Rambus fully intended to continue charging royalties for intellectual property generated by REDEC. (CX0902 at 1-2 (“My belief is that the name should NOT contain Rambus, and should contain the words ‘open standard’ . . . First, we want royalties on what we do. . . All IP is shared. We get royalties.”); CX0903 at 1-2 (“what should our answer to JEDEC be? First of all it would be beneficial if it were designed to give our partners a forum that they can participate in that makes them feel that they are as much in control of their own destiny as they currently are with JEDEC. I am not sure from a practical perspective how we could effect that and still remain in an ownership position with out patent rights. . . .Open standards seem at odds with our business model.”)).

266. Intel’s PC-100/133 specifications adopted the JEDEC SDRAM standard and added parametric details. (Peisl, Tr. 4411 (“Intel’s PC100 and PC133 specification essentially described some additives or addendums to the synchronous DRAM spec and it was JEDEC specification and it was later on added into the JEDEC specifications,” and no inconsistency between the JEDEC standard and the Intel specification); Shirley, Tr. 4139-40 (“The Intel PC-100 specification added what I would call as a low level of detail about additional speed grades and additional current requirements that they saw as important to their use of our memory products.”); MacWilliams, Tr. 4887 (“when [Intel] did the PC100 application, we made sure it was backwards compatible with the 66 megahertz”), 4906-07 (“PC100 was the effort by Intel to try and make the 100 megahertz SDRAM that met a spec referred to as PC100.”)).

267. DRAMs produced in compliance with JEDEC standards have dominated the DRAM industry for the past decade. (CX0419 (As of May 2000, “75% of the top 250 semiconductor manufacturers [were JEDEC] members, representing 80% of semiconductor sales. An estimated 90% of semiconductor standards in use are JEDEC standards.”); CX0302 at 16 (“Global JEDEC standards usage has skyrocketed.”), 17 (“If you are not [at JEDEC], your competition may be deciding your future.”); Peisl, Tr. 4384 (“JEDEC’s standards were the only source for our own specifications, meaning that . . . Infineon chip specifications were entirely directed towards the -- 100 percent compatibility towards the JEDEC specifications.”), 4386 (“If we wouldn’t have produced a chip that would not comply to the JEDEC specification, it would have not been able to work at the PC, at the server, at the laptop platforms at HP, IBM and all our other customers because of noncompliance issues, nontechnical issues, and we essentially would not have been able to sell anything”); *see* DX0141; DX0219).

268. Paragraphs 268 to 299 are unused.

III. JEDEC's Purpose and Rules Are Designed to Develop Open Standards, Free of Hidden Intellectual Property Rights.

A. JEDEC Is Devoted to Open Standards.

300. The goal of JEDEC is to develop open standards. (CX2957 at 2 (Declaration of Joel Karp) (“My understanding of the EIA patent policy is that standards promulgated by standard-setting groups are ‘open’ standards”); CX0419 (“JEDEC standards are open (in terms of IP licensing)”); CX0449 at 2 (“JEDEC’s core business is the development of open standards.”); CX3089 at 13-14 (“one of the goals of setting open standards is to prevent a single entity from stifling competition”); Appleton, Tr. 6328 (JEDEC’s “purpose is to develop an open standard [to which] companies and customers would have access . . . in order to develop their products”); Bechtelsheim, Tr. 5781-2, 5785 (“stated goal is to develop open industry standards”); Calvin, Tr. 995-96; Rhoden, Tr. 301, 536 (“the fundamental premise inside JEDEC is open standardization); J. Kelly, Tr. 1776-78 (“those [open standards] are the only kinds of standards that JEDEC generates”), 1782, 1787; Sussman, Tr. 1325; Williams, Tr. 761 (JEDEC creates “open standard[s] that everybody can use”)).

301. Open standards are free from hidden or restrictive intellectual property rights. (CX0903 at 2 (Richard Crisp writes: “The job of JEDEC is to create standards which steer clear of patents which must be used to be in compliance with the standard whenever possible.”); CX0449 at 2 (“Open standards by definition are free of restrictive intellectual property (or ‘IP’) rights”); (CX2059 at 90 (Karp, Infineon Dep.) (“open is distinguished from something that’s proprietary”); J. Kelly, Tr. 1777, 1898-99 (“EIA does not endorse a standard that contains hidden IP”); G. Kelley, Tr. 2393-96 (“first requirement was to avoid patents”); Kellogg, Tr. 5041-42; Rhoden, Tr. 536, 637; Tabrizi, Tr. 9118).

302. Open standards uphold the antitrust laws by ensuring that standards are free of discrimination and do not lead to monopolization. (CX0202 at 6 (basic rules prohibit activity that could violate the antitrust laws); CX0204 at 5 (EIA programs “shall not be proposed for or indirectly result in. . . restricting competition, giving a competitive advantage to any manufacturer, excluding competitors from the market. . .”); CX0302 at 9; J. Kelly, Tr. 1781-82 (open standards are not used to enhance market power); Rhoden, Tr. 302-03)). *See also* CX0711 at 16 (Richard Crisp email from JEDEC meeting stating “The meeting opened with a lot of controversy regarding Patents. . . Micron says the policy exists due to anti-trust concerns. That if a group of companies wanted to keep out competition they could agree amongst themselves to standardize something that is patented and not license those that they do not want to compete with.”)).

303. Open standards lower costs by avoiding patents and royalties. (G. Kelley, Tr. 2396 (“first requirement was to avoid patents”); Lee, Tr. 6595-96 (“There was also a policy . . .to try to avoid the use of patents, when possible, in defining a standard”); Peisl, Tr. 4476; CX2107 at 136-

38, 158-60 (open standards important for cost-effectiveness) (Oh, Dep.); CX2297 at 79 (DDR DRAM strong points: “Open architecture without royalties or fees.”). *See also* CX0013 at 30 (“Problems in Intellectual Property - Some participants may look for commercial advantage. Late disclosure close to market interaction. Failure to indicate a patent is filed, pending or awarded . . . - Some participants might vote differently or develop different but equivalent standards if royalties were identified in the beginning as an objective.”); CX0711 at 44 (Richard Crisp noting that Micron cited patents as reason for its “No” vote.); Heye, Tr. 3731 (“The second concern was a possible cost disadvantage we might incur in the infrastructure due to the incremental royalty fees”).

304. Open standards help ensure the use of the standard. (G. Kelley, Tr. 2398-99 (failure to disclose could block standard); Landgraf, Tr. 1694 (“worst thing to have” is a system you cannot produce because of infringement.)). *See also* CX0711 at 16 (Richard Crisp email from JEDEC meeting stating “The meeting opened with a lot of controversy regarding Patents. . . Micron says the policy exists due to anti-trust concerns. That if a group of companies wanted to keep out competition they could agree amongst themselves to standardize something that is patented and not license those that they do not want to compete with.”), at 187 (Richard Crisp writes: “SSTL passed 30/0 and was sent to council. However Hitachi stated that they had a patent relating to it. This created a big ruckus. The major thrust of the criticism of Hitachi was that they waited until the ballots had been passed before mentioning that they had a patent”).

B. JEDEC Operates Pursuant to Rules Which Govern Its Standard-Setting Activities.

305. Between 1991 and 1996, JEDEC was a part of EIA. (J. Kelly, Tr. 2075).

306. During the time when JEDEC was a part of EIA, the standard setting activities of JEDEC and other parts of EIA were governed by the written rules of the EIA as well as their own specific manuals and rules. (J. Kelly, Tr. 1824).

307. EIA’s basic rules relating to standard setting activities are found in the EIA Legal Guides, as well as in EP-3, EP-7. (CX0202 at 6; CX0203A at 20, CX0204 at 5, JX0054 at 8-9; J. Kelly, Tr. 1824-25).

308. The rules of JEDEC are provided in the EIA Legal Guides, EIA Manuals, and the JEDEC Manual of Organization and Procedure. (CX0202; CX0204; CX0203A; JX0054; CX0205; CX0205A; CX0208; J. Kelly, Tr. 1824-25 (citing EP-3, EP-7 and EIA Legal Guides)).

309. EIA rules and JEDEC rules concerning disclosure and licensing of patents are consistent. (J. Kelly, Tr. 1915-16 (“I’m not aware of any conflicts between the JEDEC rules and the EIA rules”), 1919-20 (“I think that those terms were used interchangeably, EIA patent policy and JEDEC patent policy.”)).

C. JEDEC Participants Must Act in Good Faith.

310. From 1991 to 1996, and continuing through today, EIA Basic Rule 1 required EIA/JEDEC participants to act in good faith. (CX0202 at 6 (Basic Rule 1); CX0204 at 5; CX0449 at 4; J. Kelly, Tr. 1840-41 (“[T]his provision is designed to prevent companies from acting in bad faith in connection with standard-setting activities”), 2053-55 (“all participants are under a duty under the EIA Legal Guides to act in good faith”; “clearly there are no intended loopholes”); CX2058 at 431 (Meyer 12/14/00 Dep.) (expected that JEDEC members, including Rambus, would act in good faith); Rhoden, Tr. 306-07; Sussman, Tr. 1330-32; Crisp, Tr. 2946-47; McGrath, Tr. 9272).

311. Good faith imposes a duty on participants in EIA and JEDEC activities to familiarize themselves with and abide by the letter and the spirit of the patent policy. (CX0449 at 4; J. Kelly Tr. 2053-54 (“the patent policy is supposed to be complied with not just in terms of its written letter but also in terms of the spirit of the patent policy”)).

312. Good faith requires fair treatment of other participants, trust, and honesty. (CX0449 at 4 (rules are “designed to promote openness, good faith, and fair dealing in the development of standards.”); J. Kelly, Tr. 1841 (“[C]ompanies need to participate in the process openly and honestly and fairly and in good faith and not in bad faith, because bad faith undermines the confidence of everyone in the process.”); G. Kelley, Tr. 2397 (“my mind translated [good faith] to fair treatment for all members”); Rhoden, Tr. 305-06 (“The term “good faith” as used in [the Legal Guides] is that the people. . . are coming under the premise that they're going to . . . work toward the benefit of the end user of the industry itself, and operating in good faith means that you would expect other people to do the same thing.”); Sussman, Tr. 1330 (“Good faith, we're all competitors, we're all about ready to dice each other in the marketplace, but seeing we're talking about or about to talk on intellectual property, I trust you to do something, and I expect that same set of trust back.”)).

313. Bad faith undermines the standard-setting process. (J. Kelly, Tr. 1841-42 (“bad faith undermines confidence of everyone in the process”), 1846-48 (discussing example of bad faith by deliberately shielding representative from patent information); 2134-35 & 2167-68 (discussing example of bad faith by trying to stall standardization process); G. Kelley, Tr. 2523-24 (planting a press story concerning dissension in JEDEC is bad faith and “undermines the JEDEC process.”)).

314. EIA and JEDEC must rely on the good faith of participants in the process to surface patent issues. (J. Kelly, Tr. 1836-37 (EIA relies on “the participants in the process to surface patent issues to our attention, and when those are surfaced, then we identify them in the standard, but if we don't know, we're not in a position to go out and find out either through the U.S. PTO or otherwise what intellectual property may be there.”)).

D. JEDEC Standard Setting Is Not to be Conducted in a Manner That Would Result in Anticompetitive Effects.

315. Between 1991 and 1996, and continuing through today, Basic Rule 5 required that EIA/JEDEC activities “not be proposed for or indirectly result in . . . restricting competition, giving a competitive advantage to any manufacturer, [or] excluding competitors from the market.” (CX0202 at 6; CX0204 at 5; J. Kelly, Tr. 1842-44, 1848-49 (discussing example of bad faith that could lead to patent royalties on television sets); CX0711 at 16 (Richard Crisp email from JEDEC meeting stating “The meeting opened with a lot of controversy regarding Patents. . . Micron says the policy exists due to anti-trust concerns. That if a group of companies wanted to keep out competition they could agree amongst themselves to standardize something that is patented and not license those that they do not want to compete with.”); CX1958 at 12 (“Two possible theories of non-enforcement [of patents]:. . . 2) Antitrust?”), 21 (discussing monopolization in context of standard-setting activities)).

E. JEDEC Participants Must Comply With Patent Disclosure and Licensing Assurance Rules Intended to Ensure Open Standards.

1. The Patent Rules Are Intended to Foster Free Use of JEDEC Open Standards.

316. Between 1991 and 1996, and continuing through today, JEDEC has ensured that its standards were open through the JEDEC patent policy. (CX0449 at 2; J. Kelly, Tr. 1908 (“If there’s no disclosure, then there’s no opportunity to request the assurances”); G. Kelley, Tr. 2398-99 (prevent IP from “blocking” standards), 2475 (discussing letter to Texas Instruments concerning Quad CAS issue (CX2384) and the need to prevent development of mediocre standards); Landgraf, Tr. 1694 (“the purpose of the patent policy is to disclose and make sure that standards do not have any conflicts down the road with their potential use.”); Lee, Tr. 6598 (“the general goal [of the patent disclosure policy] was to develop a standard that was free from encumbrance from patents, and so the purpose to disclose it was to be able to allow the committee to avoid the use of patents and incorporating them in the standard.”)).

317. Early disclosure provided JEDEC participants with the opportunity to choose a different, but equivalent path for the standard. (CX0903 at 2 (Richard Crisp writes: “The job of JEDEC is to create standards which steer clear of patents which must be used to be in compliance with the standard whenever possible.”); CX0711 at 187 (Richard Crisp writes: “SSTL passed 30/0 and was sent to council. However Hitachi stated that they had a patent relating to it. This created a big ruckus. The major thrust of the criticism of Hitachi was that they waited until the ballots had been passed before mentioning that they had a patent”); CX0013 at 30 (“Problems in Intellectual Property - Some participants may look for commercial advantage. Late disclosure close to market interaction. Failure to indicate a patent is filed, pending or awarded . . . - Some participants might vote differently or develop different but

equivalent standards if royalties were identified in the beginning as an objective.”); CX0711 at 44 (Richard Crisp noting that Micron cited patents as reason for its “No” vote.); CX3005 at 1 (“We [Toshiba] understand from Micron and Cyrix there is also concern on the infringement of Intel’s burst patent . . . a pin was dedicated to burst mode, making it selectable, *to side step the patent issue.*”) (emphasis added); CX0083 at 5-6 (two ballots were put on hold pending resolution of status of patent owned by Sun Microsystems.); Sussman, Tr. 1343 (“The earlier that we have the information that something may have some IP on it, the better it turns out to be, so we don’t waste time talking of this rather than an alternate.”); Landgraf, Tr. 1693-94 (“The policy, as I understood it, was that if you as a member of JEDEC knew of a patent or application for a patent that would potentially be impacting the standard or proposed standard, you were to disclose it to the committee for -- for consideration so the committee could decide to either modify the standard proposal. . . so that it did not infringe with the application or the patent.”)).

2. JEDEC Participants Must Disclose Patents or Pending Patents That Might Be Involved In The JEDEC Work.

318. The JEDEC patent policy contains two distinct parts. First, all participants in the process are subject to a mandatory duty to disclose intellectual property that might be involved in the work of the committee. Second, the chairperson of the meeting has a duty to ensure that no known patented or patentable material is included in a JEDEC standard unless the committee has received advance, written assurance from the owner of the intellectual property to that the owner will license the intellectual property for free or on reasonable and non-discriminatory terms. (CX0208 at 19; CX0208A at 19 (copy of 21-I Manual produced by Rambus); CX2076 at 80-81 (Brown Infineon Dep.) (“any members who are aware of any patent position or potential patent positions on the material should and are obligated to reveal that to the committee at that time.”); CX2191 at 8 (JEDEC policy is to not standardize patented items without fair licensing; all participants are requested to reveal patents)).

319. The JEDEC patent disclosure policy is that:

“The Chairperson of any JEDEC committee, subcommittee, or working group must call to the attention of all those present the requirements contained in EIA Legal Guidelines, and call attention to the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or *pending patents*, that might be involved in the work they are undertaking.”

(CX0208 at 19; CX0208A at 19) (emphasis added); (J. Kelly, Tr. 1837-38 (The EIA/JEDEC patent policy “requires an early disclosure of intellectual property; that is, patents or patent applications that are or may be related to the work of a standard-setting committee. And then once the disclosure -- the early disclosure is made, if the patent owner is willing to give reasonable assurances that I alluded to earlier, that is, reasonable and nondiscriminatory licensing

terms or without charge.”); Rhoden, Tr. 307 (“The JEDEC patent policy is essentially if you have IP, IP that may relate to any of the discussions that are going on inside JEDEC, that you are required to disclose that IP to the people who are participating.”); Lee, Tr. 6595-96 (“[T]here was a requirement to disclose patents or patent applications in progress to the committee if the work that they were doing may relate or if the patent may relate to the work the committee was doing.”); Sussman, Tr. 1333 (“Q. What is your understanding of the JEDEC patent policy that was in effect from the 1991 to '96 time period? A. Basically, if you have IP, you are to inform the group of that IP.”); Landgraf, Tr. 1693-94 (“The policy, as I understood it, was that if you as a member of JEDEC knew of a patent or application for a patent that would potentially be impacting the standard or proposed standard, you were to disclose it to the committee. . . so the committee could decide to either modify the standard proposal. . .so that it did not infringe with the application or the patent, or the committee would then ask . . . the owner of the patent . . . whether they would comply with the JEDEC policy, which had to do with granting licenses either freely to all applicant requesters or offer the patent on reasonable terms and conditions. In a nutshell, that was the policy.”), 1702 (“when I first joined JEDEC, [the manual containing the patent policy] was at Revision I, and subsequent it was revised to Revision J, but Manual 21-I is the standards and policies.”); Williams, Tr. 771 (“if somebody had a patent or pending patent based upon the work that was being discussed at JEDEC, that there needed to be disclosure of sufficient information so that the council or the committee could determine whether or not what was being discussed was actually implied in the patent.”), 790 (“I don't know exactly what the JEP stands for, but it is a manual that guides the policies of JEDEC, how the JEDEC ought to operate.”); CX2076 at 80-81 (Brown Infineon Dep.) (“whenever material comes up in the committee for discussion and for voting, any members who are aware of any patent position or potential patent positions on the material should and are obligated to reveal that to the committee at that time.”); Calvin, Tr. 1004 (“anyone who was aware of patent - - patented items, that could affect policy, had an obligation to bring that awareness to the group.”)).

320. The JEDEC patent disclosure rule applied not only to issued patents, but also to patent applications and anything in the patent process. (CX0208 at 19; CX0208A at 19; JX0014 at 25; CX0306 at 1; CX0042A at 7 (Townsend memo produced by Rambus referring participants to “existing rules of EIA governing *patentable matters*) (emphasis added); CX2957 at 2 (Declaration of Joel Karp) (“contrary to industry practice and understanding for an *intellectual property* owner to remain silent during the standard-setting process – and then after a standard has been adopted and implemented – later attempt to assert that its *intellectual property* covers the standard”) (emphasis added); CX2059 at 150-51 (Karp, Infineon Dep.) (verifying veracity of declaration); Calvin, Tr. 1006-07 (clear about fact that patent applications were required to be disclosed); Kellogg, Tr. 5024; J. Kelly, Tr. 1869-70; 1886-88 (term “patent” included patent applications), 1893-94, 1896-97 (“The industry probably moves even more quickly, particularly in high technology industries like the ones that EIA works with, and frequently patent applications move at a measured pace through the patent application policy to the issuance of final patents. So, if the work of the committee was held up, in effect, by the condition that only issued patents needed to be disclosed, then the standard development process could reach a very

late stage or, in fact, already be concluded by the time a patent finally issued and there was disclosure that the patent was required to comply with the work by the committee on the standard under development, and that would produce exactly the same kind of anti-competitive result that we're trying to prevent by the disclosure.”); G. Kelley, Tr. 2406-07 (“patent” as used by Mr. Townsend meant “an issued patent that was available from the patent office, patent applications that were being worked on with the patent office, and items that were probably going to become patents.”), 2689 (“I would have thought that that new member would understand that it included patent applications from the beginning because we were dealing with patent applications from that new member's beginning and was clearly an issue at my meetings.”); Landgraf, Tr. 1695-96 (“As soon as a member knew that they had -- either they had a patent of their own or applications or even a third party's patent or application, if you knew that and it was touching on some element of the standard or proposed standard, you were supposed to disclose that to the committee so that the committee has the earliest possible time to make changes or to have patent policy compliance.”); Lee, Tr. 6595-96 (“the patent policy had a few aspects to it. First of all, there was a requirement to disclose patents or patent applications in progress to the committee if the work that they were doing may relate or if the patent may relate to the work the committee was doing. There was also a policy, as I understand, to -- to try to avoid the use of patents, when possible, in defining a standard.”); CX2057 at 211-12 (Meyer 12/13/00 Dep.) (understood that “patents” included patent applications); Rhoden, Tr. 307, 317-21 (“patent” has always been applied to anything in the patent process), 336 (“patentable” includes whether or not a patent has been applied for), 618-19, 626-27; Sussman, Tr. 1333-34 (“issued patents, patent applications . . . if you were about to apply for a patent”), 1342 (understood in 1981 or 1982 that patent policy required disclosure of patent applications); Williams, Tr. 771 (“patent or pending patent”), 909-11); CX2076 at 80-81 (Brown Infineon Dep.) (“Issued patents and pending patent material”); McGrath, Tr. 9272-73 (“JUDGE McGUIRE: But also this obligation to act in good faith, did that incorporate the idea of disclosing patent applications as they were being developed? THE WITNESS: Yes, it would.”); (CX2054 at 165 (Mooring, Infineon Dep.)). [note: R objection pending] (“if [Manual of Organization and Procedure 21-I] was the valid document, then there would be requirement to disclose applications.”)).

321. The EIA/JEDEC patent policy did not change during the 1990s. (J. Kelly, Tr. 1920 (since 1990 “sometimes the words have changed, but the substance has not.”)).

322. The EIA Legal Guides prohibit the sharing of future plans at EIA sponsored meetings. (CX0202 at 4). There is no tension between the prohibition on discussing future plans and the requirement to disclose patent applications that might relate to JEDEC standards. (J. Kelly, Tr. 1989 (“I don't see that there's any tension there at all.”). The future plans that are subject to the prohibition in the EIA Legal Guides are discussions of plans that would result in a violation of the antitrust laws. (J. Kelly, Tr. 1989 (“T]he future plans that were referred to in the EIA Legal Guides are discussions that could result in conduct prohibited by the antitrust laws.”)).

3. Disclosure is Mandatory.

323. Membership in JEDEC is voluntary. (J. Kelly, Tr. 1966 (“The entire process is voluntary, and as a voluntary standards development organization, we really don't have the power to impose sanctions against members who don't comply with the policy.”); Rhoden, Tr. 615 (“participation in the committees is always voluntary.”)).

324. Once a member joins JEDEC, however, the obligations that participants assume are mandatory requirements of participation. (CX0208 at 19 (“the obligation of *all participants* to inform the meeting of any knowledge they may have of any patents, or pending patents that might be involved in the work they are undertaking”) (emphasis added); J. Kelly, Tr. 1903-04 (“is it optional on the part of someone with knowledge of a patent or patent application to disclose or not disclose, *the answer is absolutely no, it is not optional*”), 1979 (“any time a participant has knowledge of relevant intellectual property, patent or patent application, that is or may be required to comply with the work underway, then that participant has an absolute duty to disclose it.”); Lee, Tr. 6595-96 (“there was a *requirement* to disclose patents or patent applications in progress to the committee if the work that they were doing may relate or if the patent may relate to the work the committee was doing.”); Rhoden, Tr. 319, 615 (disclosure is an obligation); Sussman, Tr. 1346 (“Q. Again, based on your experience, did you view this patent disclosure policy we have been discussing as a voluntary option or was it a mandatory requirement on JEDEC members? A. *It's required.*”); CX2057 at 200 (Meyer 12/13/00 Dep.) (disclosure is an obligation); CX0711 at 188 (Richard Crisp noting that “So the conclusion I reach here is that we can abide by the patent policy on a case by case basis. . . . As long as we mention that there are potential patent issues when a showing or ballot comes to the floor, the we have not engaged in ‘inequitable behavior. . . . The things we should not do are to not speak up when we know that there is a patent issue.’”)).

4. The Disclosure Obligation Does Not Include A Duty to Conduct a Patent Search.

325. EIA and JEDEC did not require members to conduct patent searches. (J. Kelly, Tr. 1869-70, 1966-67; G. Kelley, Tr. 2457-58 (IBM did not agree to provide a list of patents because IBM was concerned that bringing a list to JEDEC might erroneously be construed as a complete catalog of IBM patents in a particular area); Williams, Tr. 895-96 (discussing IBM's statement); CX2057 at 193 (Meyer 12/13/00 Dep.)). *See also* (RX1712 at 8 (no duty to search under ANSI Guidelines)).

326. From time to time, however, JEDEC participants made requests for other participants to clarify their companies' patent position relating to specific items. In these instances, participants fulfilled their obligations under the patent policy by acting in good faith. For example, at the May 1992 JC-42.3 meeting, patent issues were raised concerning Hitachi's LOC package proposal. Hitachi's representative, Mr. Tabrizi, did not know about the patent, but

promised the committee that he would check on it. (CX0034 at 8). At the July 1992 JC-42.3 meeting, concern about patent coverage was noted relating to a Hitachi presentation. (JX0013 at 13). At the September 1992 JC-42.3 meeting, Hitachi noted that it did not have a patent on the proposal. (CX0042 at 9). Ultimately, JEDEC chose a different path to develop the standard because of the difficulty in reviewing the patent issues on the matter. (JX0015 at 4).

327. Similarly, among the patent matters discussed at the March 1993 Committee meeting was an inquiry made to IBM concerning whether IBM would disclose to the Committee all patents and patent applications held by the company worldwide. (G. Kelley, Tr. 2449-50; JX0015 at 6). Because of the breadth and difficulty of the company-wide search that would be required for such a listing, there was a risk that any such listing would be incomplete and misleading, therefore IBM stated that it would not undertake such a listing. (G. Kelley, Tr. 2450-51).

328. Despite the fact that IBM was under no duty to search its patent portfolio, IBM representatives agreed to inform the JC-42 committee of any relevant patents, patent applications or items in the patent process of which they were aware, and to investigate IBM's position with respect to any patent that other JEDEC participants could describe. (G. Kelley, Tr. 2450-51 ("they were asking me to provide the committee with a list of all issued patents and patent applications, and I was warning the committee that that was not something that I could do. It was just not a possible task for me to know what was going on all over the world for the IBM Corporation. I then went on to promise the committee that I would alert the committee to any information that I had that applied to the JEDEC task at hand and if a question came up, I would get them information on any patent that they could describe to me."); Kellogg, Tr. 5024-26 ("one of the things that [IBM] felt impossible for us to do would be to study/evaluate the entire patent portfolio from IBM"; "I believe Gordon [Kelley] stated at least once and actually followed up. . . that if we were requested to evaluate the possibility of patents and if we were able to do so, we would investigate.")).

329. The issue concerning IBM's position on listing all its patents was raised again at the December 1993 Committee meeting. (JX0018 at 3; G. Kelley, Tr. 2471-73). IBM reiterated its position as stated to the Committee in March 1993 that it was impossible reliably to conduct a search to provide such a company-wide listing, and so would not attempt to do so. (JX0018 at 3; G. Kelley, Tr. 2471-73).

5. All JEDEC Participants Must Disclose.

330. The JEDEC disclosure policy imposed an obligation on "*all participants* to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking." (CX0208 at 19 (emphasis added); CX0202 at 4 ("They [the "General Guides Applicable to All EIA Activities"] are required to be read and followed by all members of the Association and staff, chairmen and members of all committees,

sections, divisions, and other EIA sponsored groups.”); Calvin, Tr. 1005-06 (for presenters “it wasn't a different obligation”); J. Kelly, Tr. 1865, 1969-70 (“All participants in the work of the committee have a shared responsibility to disclose any information of which they have personal knowledge of intellectual property that may relate to the working committee. It's not limited to members, it's not limited to the IP owner. It's across the board.”); Landgraf, Tr. 1700 (“I don't think there was any distinction, whether you were a member presenting ideas for standardization or you're a member just observing the direction the committee is going, because . . .the committee is the collective intelligence of its membership, . . . So, the obligation is not only on the person making a presentation but also on the membership to point out improvements that can be done or issues with the direction that the committee is going. And so the dialogue and feedback is important, and that includes the idea of disclosures of patents and applications.”); Rhoden, Tr. 319-20 (“it's everyone who is a member either in attendance or not in attendance, a guest, a -- whoever is either in the room at the time discussions are held or has access to any of the JEDEC information outside of the meetings themselves.”). *See also* RX1712 at 8 (ANSI Guidelines suggest standards organizations adopt rules to ensure that any participant, not just the patent holder, identifies patents that may be required)).

6. Meaningful Information Must be Disclosed.

331. The JEDEC patent policy required that a participant disclose sufficient information to put the committee on notice as to the nature of the relationship between the proposed standard and the intellectual property that might relate to the proposed standard. (Calvin, Tr. 1010-12 (“tell the subject matter of the patent or patent applications, as the case may be”; “the policy would be to follow up to understand those aspects of claims that might affect the patent, or might affect the development of the standard.”); J. Kelly, Tr. 1870-71 (“[A]s long as enough information is provided to the committee that it understands the nature of the technology and how it applies to the standard, that's enough.”), 1994, 2004 (“the explanation includes identification of the technology and how it relates to the work of committee.”), 2136-37; Rhoden, Tr. 627 (“sufficient technical information would be required to be disclosed, such that the formulating committee can understand what has been claimed”); Sussman, Tr. 1375-76 (“give us the concept and. . . at least enough information to know what you're doing.”); Williams, Tr. 771-72, 774-75 (no requirement to provide copies of patent applications), 793-94 (“you needed to know sufficient information to make an informed decision whether or not it applied. . . You needed to know sufficient information so that you could make a decision”)).

332. Disclosures that did not provide the committee with an understanding of the relevance of the technology to the are insufficient. (J. Kelly, Tr. 2134-35 (discussing Echelon example), 2158-63 (disclosure made to block standard is made in bad faith); Kellogg, Tr. 5060 (“JUDGE McGUIRE: Well, then let me ask a question. Under your understanding of the patent policy, when one discloses a patent, are you saying then that if they haven't also disclosed the implications of the patent, have they I guess adequately then disclosed the patent under the patent policy? THE WITNESS: No. That's kind of my point, and I appreciate the clarification.. .

.Within the context of the patent policy at JEDEC, disclosure of a number I don't believe meets the patent policy. If the number is disclosed not in any context of anything else.”); G. Kelley, Tr. 2578-79 (comment of “no comment” is inadequate.); Sussman, Tr. 1413-14 (Rambus disclosure relating to SyncLink was inadequate because “I do not have enough information to know what you have. All I can do is determine that you have something. . . . you're telling me that you do have something. But I don't know what it is.”)).

7. The Duty to Disclose Is Triggered by the Participant’s Knowledge or Belief of A Relevant Patent or Application.

333. The duty to disclose was triggered by the knowledge or belief of the JEDEC participant. (Calvin, Tr. 1012 (“as you began to realize that the direction the standard was going could be affected by those [patents or patent applications], you would have a similar obligation [to disclose].”); J. Kelly, Tr. 1980-82 (subjective belief or judgement of participant that there is a sufficient relationship between the IP and the standard triggers disclosure obligation); CX2057 at 200 (Meyer 12/13/00 Dep.) (“sufficient knowledge to be aware that there was coverage” triggers obligation to disclose)).

334. A company could not deliberately shield its representative from knowledge of relevant patents. (J. Kelly, Tr. 1983 (such conduct would violate duty of good faith)).

8. The Duty to Disclose Extends to Any Patent or Application That Might Be Involved in JEDEC Work.

335. The EIA/JEDEC patent policy required disclosure of patents and patent applications that “*might be involved*” in the standards under development. (CX0208A at 19 (“obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking”) (emphasis added); G. Kelley, Tr. 2705 (“there were many work items that occurred on the committee that did not become standards. . . My definition says that any claim that might apply to the work of the committee it was required to disclose.”); Landgraf, Tr. 1693-94 (disclose patents or applications “that would *potentially* be impacting the standard or proposed standard.”); Lee, Tr. 6595-96; Rhoden, Tr. 307; Sussman, Tr. 1346 (participants must disclose where there is a “gray” area); CX2057 at 203-04 (Meyer 12/13/00 Dep.) (disclosed patent when “sufficiently close” to work of JEDEC.); Williams, Tr. 909-11 (if “there would be a reasonable possibility that the patent was going to be associated with the work of JEDEC, that you ought to say, hey, I’ve got something I’m patenting here or there’s something that you’re talking about that I’ve got some IP on.”)).

336. In 1994, Texas Instruments sought clarification of the of the EIA/JEDEC patent policy. (CX0353 at 2-5) (March 9, 1994, memo from requesting that the JEDEC Council and Legal Counsel provide guidance to the committee concerning whether the patent policy applied only to patents that must be used to comply with the standard). *Cf.* (J. Kelly, Tr. 2057-58

(Rambus never contacted EIA Legal Counsel concerning questions of interpreting the patent policy)).

337. On March 29, 1994, Mr. Kelly responded that “[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention.” (CX0353 at 1 (underline in original); J. Kelly, Tr. 1941-42). Furthermore, it was not necessary for the committee to make a factual determination that the use of the patented invention is, in fact, required to meet the standard. (CX0353 at 1; J. Kelly, Tr. 1941-42). *See also* (J. Kelly, Tr. 1945 (assurance should come as soon as “it appears that the technology is or may be required to comply with the standard under development.”)).

338. The Federal Circuit erred on the facts when it appeared to say that the only intellectual property that was required to be disclosed was that which, in fact, is required to meet or to comply with the final issued standard. Participants are unable to make an on-the-spot infringement analysis of what the final standard will look like and whether or not the patent or patent application covers the proposed standard. (CX3089 at 18; J. Kelly, Tr. 2064-66 (the majority “appeared to say that the only intellectual property that. . . needed to be disclosed was that which in fact is required to meet or to comply with the final issued standard, and the concern we have there is that it basically requires participants in the process to make an on-the-spot infringement analysis of what the final standard will look like.”); Williams, Tr. 771-72 (“and none of us were lawyers there, so we couldn't determine . . . if it infringed or not. I mean, that wasn't the purpose.”); CX2059 at 201 (Karp, Infineon Dep.) (disclose intellectual property that might be involved in the work; no expectation that participants would conduct an infringement analysis)).

9. The Duty to Disclose Arises As Soon As a Participant Knows of A Relevant Patent or Application.

339. A participant is under a duty to disclose at the very moment the participant knows that his or her own company or anyone else's company has patents or patent applications that might involve the work of JEDEC. (Calvin, Tr. 1012-13 (“as you began to realize that the direction the standard was going could be affected by those [patents or patent applications], you would have a similar obligation [to disclose.]”); J. Kelly, Tr. 1837; 1945 (disclose as soon as “it appears that the technology is or may be required to comply with the standard under development.”), 1983-84 (“if there is any suggestion that the committee's work should move in a certain direction or any information that's presented with that as the intent, then the duty to disclose arises.”); Landgraf, Tr. 1695-96 (“as soon as a member knew that they had -- either they had a patent of their own or applications or even a third party's patent or application, if you knew that and it was touching on some element of the standard or proposed standard, you were supposed to disclose that to the committee”); Rhoden, Tr. 356-57 (“my understanding always was as early as possible. That's the way it has always been stated and the way we have always used it. You are required as soon as you have knowledge of a discussion taking place, a

presentation, discussion, ballot, whatever, as soon as you become aware that a topic is being discussed for which you know that there is IP, you are obligated to disclose.”), 654 (disclose as early as possible); Williams, Tr. 772 (“as soon as you knew that there was a possible patent the could apply to what was being discussed”), 909-11 (as soon as you could if you thought it [a patent or patent application] was going to be applicable)).

340. The duty to disclose was not tied to any procedural formality in the JEDEC process. (CX0208A at 19 (“The Chairperson of any JEDEC committee, subcommittee, or working group must call to the attention of all those present the requirements contained in EIA Legal Guidelines, and call attention to the obligation of all participants to inform the meeting of any knowledge they may have of any patents, or pending patents, that might be involved in the work they are undertaking.”) (emphasis added); J. Kelly, Tr. 1945, 1983-85 (“it's not tied to any procedural formality in the process at all”); Rhoden, Tr. 488-89 (duty triggered by “discussion, presentations, ballots, anything that’s taking place inside the committee.”); Landgraf, Tr. 1716-17 (“in a JEDEC committee, there's a lot of official work that is documented, and survey ballots are considered to be official work.”); Lee, Tr. 6987-88 (“Q. Was it your understanding in April 1997 that the required time of disclosure for intellectual property known to the representative was time of balloting, but it was encouraged earlier? A. No.”); Sussman, Tr. 1343 (“Basically any discussion. The earlier that we have the information that something may have some IP on it, the better it turns out to be, so we don't waste time talking of this rather than an alternate.”)).

341. The disclosure duty is triggered by discussions at task group meetings. (Sussman, Tr. 1386 (“The same rules apply.”); Macri, Tr. 4661 (“At the beginning of every task group meeting, we always say that the full JEDEC rules are in effect, and during discussions with these companies, I said, of course, you would have to abide by the JEDEC rules.”)).

342. Early disclosure promotes efficiency in standards development practices. (J. Kelly, Tr. 1955-56 (“by encouraging early disclosure of patents and obviously in EIA's case also patent applications, we get as much information, as I said before, as early in the process as possible to allow it to move forward expeditiously and efficiently without concern about unknown, undisclosed patents that may impede the work of the committee.”)). *See also* (RX1712 at 6-7 (encouraging early disclosure of patents and patent applications promotes “greater efficiency in standards development practices.”)).

343. A company that deliberately withdraws from JEDEC for the purpose of avoiding its patent disclosure obligations had violated both the patent policy and the duty of good faith. (J. Kelly, Tr. 1907 (“every participant in the process with knowledge of relevant IP has a continuing duty to disclose that IP and relevant technical information.”), 1993 (“the violation [of the patent policy] would occur at that time there was knowledge that triggered the duty to disclose. . . the withdrawal itself, if it was motivated by bad faith, would certainly violate the Legal Guides.”); G. Kelley, Tr. 2758 (“Q: Again, Mr. Kelley, based on your understanding of the disclosure policy between 1991 and 1996, if a company observed a presentation while that company was a member

and then chose to withdraw before the matter came to ballot, would the member's withdrawal relieve it of any obligation to disclose relevant patents or patent applications? A. No.”)).

344. Resigning from JEDEC does not relieve a company of the duty to disclose relevant intellectual property that might relate to JEDEC work conducted while the company was a member. (G. Kelley, Tr. 2758 (“Q: Again, Mr. Kelley, based on your understanding of the disclosure policy between 1991 and 1996, if a company observed a presentation while that company was a member and then chose to withdraw before the matter came to ballot, would the member's withdrawal relieve it of any obligation to disclose relevant patents or patent applications? A. No.”); J. Kelly, Tr. 1907 (“every participant in the process with knowledge of relevant IP has a continuing duty to disclose that IP and relevant technical information.”), 1992-94 (violation of the duty to disclose occurs at the time of the participant’s knowledge, which would be prior to withdrawal; party withdrawing must identify technology and its relationship to the standard.)).

345. The Federal Circuit majority was in error on the facts when it tried to pinpoint an exact moment in time when disclosure might be or was required. (CX3089 at 18; J. Kelly, Tr. 2064-65 (the majority “tried to pinpoint an exact moment in time when disclosure might be/was required, and I believe the majority said that that moment in time was when a formal ballot was presented for a vote in JEDEC, and that. . . is absolutely not the case. The rule is as early as possible in the process and there is no procedural point, identifiable point, at which disclosure is required”)).

10. The Duty to Disclose is Continuing.

346. The EIA/JEDEC patent policy applied with equal force to situations involving: 1) the discovery of patents that may be required for use of a standard subsequent to its adoption, and 2) the initial issuance of a patent after the adoption of a standard. (CX0208 at 29 (“the EIA Patent Policy applies with equal for to situations involving: 1) the discovery of patents that may be required for use of a standard subsequent to its adoption, and 2) the initial issuance of a patent after the adoption of a standard.”); J. Kelly, Tr. 1985 (once a standard has been finalized and adopted, members have a continuing duty to disclose patents or patent applications relevant to the final standards.); Rhoden, Tr. 323 (“the EIA patent policy has applied to patents even after the fact, those granted after the issuance of a standard.”); Sussman, Tr. 1344-45).

11. In Addition to Disclosure, JEDEC Participants Must Comply With Licensing Assurance Requirements.

347. JEDEC rules prohibit it from including patented or patentable material in JEDEC standards without written assurances from the owner of the intellectual property that it will grant licenses for free or on reasonable and non-discriminatory (“RAND”) terms. (CX0203A at 11 (“The committee chairman must have also received a written expression from the patent holder

that he is willing to license applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination.”); CX0208 at 19 (“the committee chairperson must receive the written assurance of the organization holding rights to such patents that a license will be made available without compensation to applicants. . . or that a license will be made available to all applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination”); JX0054 at 9; CX2191 at 8 (“JEDEC has a policy of not making standards on items that have been patented, unless the patent holder agrees to certain restrictions regarding fair royalties and not restricting companies that can be licensed”); Bechtelsheim, Tr. 5897-98 (using patented technology “is okay as long as the patent holder would commit to licensing their required patents under reasonable and nondiscriminatory terms”); J. Kelley, Tr. 1868-69; 1884-86 (the rule is “firm” and JEDEC committees are forbidden to adopt standards with known patents), 1895-96, 1907-08 (“The patent owner is free to give or not to give the written assurances. If the patent owner does not give the written assurances, then the committee can take no further action with respect to the patented technology.”); G. Kelley, Tr. 2393; Landgraf, Tr. 1693-94 (the committee would ask the patent owner “whether they would comply with the JEDEC policy, which had to do with granting licenses either freely to all applicant requesters or offer the patent on reasonable terms and conditions.”); Lee, Tr. 6991 (when patents were identified “the JEDEC member also had a responsibility to agree on reasonable, nondiscriminatory license fees”); Rhoden, Tr. 307-08; Williams, Tr. 793-794 (the intellectual property “needed to be licensed on a reasonable and nondiscriminatory basis”); Grossmeier, Tr. 10951 (“If there were patents declared or disclosed, the committee chair would advise . . . that proposal or that standard could not proceed to the JEDEC Council for approval until a letter was received by the JEDEC office from the patent holder saying that it. . . would comply with the EIA guidelines on accessibility of the patent, with reasonable terms and nondiscriminatory access.”). *See also* (Kellogg, Tr. 5046 (obligated to terminate consideration of Quad CAS once committee became aware of patents; begin considering “work-arounds.”); CX0711 at 171 (Richard Crisp noting that “There are no second showings at this meeting of the SyncLink material . . . Off-line Dave Barnum of Augat. . . said that he thinks that the reason there will not be second showings is that we have cast doubt over the patent issue.”)).

348. RAND licensing helps to ensure open standards. (J. Kelly, Tr. 1895-96 (“licensing assurances are designed to ensure that the process is open and that the end product of the process is open and . . . that the end product of the process, which is a standard or a technical publication, will not include” unlicensed or restrictive IP.”)).

12. The Licensing Assurances Must Be in Writing.

349. Oral statements relating to licensing assurances are not enough to comply with JEDEC/EIA policy. (J. Kelly, Tr. 1880-81 (“We would require in addition a written expression of the company's willingness to license [on reasonable and non-discriminatory terms] signed by a person in a position of authority to bind the company.”), 2004-05 (JEDEC requires “the commitment of the company, not the commitment of the participant, and that of necessity

requires that there be something in writing on company letterhead signed by an official with the authority to bind the company.”)).

350. The wording on the written assurance letter needs to be consistent with the language found in Section 3.4 of EP-7-A, the EIA Style Manual, with no substantial modifications or additions. (JX0054 at 9; J. Kelly, Tr. 1881 (“the wording needs to be in the words that you see in Section 3.4 [of EP-7] with no substantial modifications or additions.”), 1898-99 (the RAND requirement is related to good faith)).

351. EIA general counsel is responsible for determining whether a written assurance complies with EIA policy. (J. Kelly, Tr. 1882 (“Q. And who within EIA determines whether licensing assurance letters satisfy the organization's rules? A. I do.”)).

352. Assurances should come as soon as it appears that the technology is or may be required to comply with the standard. (J. Kelly, Tr. 1945 (“ if it appears that the technology is or may be required to comply with the standard under development, then the assurances should be forthcoming at that point.”); CX0353 at 1 (“[w]ritten assurances must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention.”) (underline in original)).

353. Once written assurances are received, then JEDEC may consider including patented technology in a standard. (J. Kelly, Tr. 1839-40 (“when the best approach to a technological problem is patented technology, then we, of course, will adopt the patented technology as part of the standard. . . provided there is disclosure of the existence of the IP early in the process and provided that we obtain the licensing assurances.”), 1988 (“if the patent is disclosed early and the assurances are given, there is no reason not to move forward with the best technological approach, even if it's patented or subject to a patent application.”)).

13. Assurance Must be Given of Reasonable Royalty Rates.

354. Actual royalty rates are not discussed in JEDEC. (CX2058 at 235-36 (Meyer 12/14/00 Dep.)).

355. EIA and JEDEC do not determine what is a reasonable royalty rate. (CX2089 at 174-75 (Meyer Infineon Tr.) (reasonable “was up to the negotiations”); J. Kelly, Tr 1882-83 (JEDEC does not “have the expertise to be able to determine what's commercially reasonable in the context of any industry, no less semiconductors. . . That expertise resides in the industry. So, that's why in the first instance we leave it to the parties themselves to work out what's reasonable.”)).

356. Determination of a reasonable royalty rate is left to negotiation and market forces or the courts. (CX2089 at 174-75 (Meyer Infineon Tr.); J. Kelly, Tr. 1882-83, 2073-74 (JEDEC and

EIA “don't get into the definition, the further definition of reasonable and nondiscriminatory at all. We leave that to the parties to work out or the courts.”)).

F. JEDEC Informs Participants of the Disclosure and Licensing Obligations.

357. JEDEC informed participants of their obligations under the patent policy through discussions at JEDEC meetings, manuals, minutes, ballots, the JEDEC sign-in sheet, and advice from John Kelly. (Rhoden, Tr. 324) (stating that JEDEC informed participants of the patent policy by: (1) reviewing the patent policy at every committee meeting; (2) making available to everybody the Manual of Organization and Procedure; and (3) reiterated the patent policy on the sign-in sheet). *See also* (CX2057 at 95 (Meyer 12/13/00 Dep.) (Describing various ways of learning about the patent policy)).

1. Meeting Presentations.

358. The chairperson of each JEDEC committee, subcommittee, or working group was required to call to the attention of all those present the requirements contained in the EIA legal guides to inform the meeting on any knowledge they may have of patents or pending patents that might be involved in the work of the meeting. (CX0208 at 19; CX0208A at 19).

359. Jim Townsend of Toshiba was the chairman of the JC-42.3 committee during the relevant time period. He was elected chairman at the December 1991 meeting. (JX0010 at 12 (noting Mr. Townsend's election)).

360. Mr. Townsend ensured that the committee participants were informed of their obligations with respect to the patent policy. (CX2078 at 38-39 (Karp, Micron Dep.) (“I believe it was a personal crusade by Jim Townsend); G. Kelley, Tr. 2399 (“Jim Townsend made it a very big issue that the committee needed to deal with patents and what he called patent applications in the work of the committee so that we could avoid whenever possible.”); Lee, Tr. 6597 (Townsend “was pretty vocal at the beginning of meetings to state the policy and to clarify if any question came up.”); Rhoden, Tr. 325 (“Generally, during that period of time, it would have been Mr. Jim Townsend who would have made those [patent] presentations”); Williams, Tr. 771 (“Q. Between late 1991 through 1993, how did you learn about JEDEC's patent policy? A. Mainly by the presentations that were given at every meeting by Mr. Townsend.”)).

361. Other chairmen also presented the patent policy to their respective committees. (JX0029 at 2 (“Mr. Kelley noted verbally what is the patent policy of EIA/JEDEC.”); Sussman, Tr. 1347-48 (“As a chair, as I opened the meeting, I would mention the JEDEC patent policy, and I would flash a transparency on the screen.”)).

362. The Wang litigation sensitized the JC-42 committee to patent issues. (G. Kelley, Tr. 2401-02 (after *Wang* “Jim had become a general with a flagpole patent, and at every meeting

and every sub-meeting for a week of meetings, Jim emphasized each group's need to make sure that we gave time for disclosure of patents and discussion of patents and resolved any patent issues that could be resolved at the committee meeting for the purposes of meeting the requirements of an open standard.”); Landgraf, Tr. 1698-99 (*Wang* “served to reinforce the seriousness of the policy. At this point, it became crystal clear to me and I think other people that when you're developing standards, the idea is to expand the number of suppliers and the number of potential users for it, and if you are going to participate in an open standard formulation body, you need to disclose everything that is applicable or potentially impacting the standards that you're going to adopt.”); Sussman, Tr. 1353 (Townsend “was very sensitized by the WANG case and started to compile a [patent tracking] list.”); Williams, Tr. 786-87 (Chairman Townsend and the rest of the board wanted to ensure [that *Wang*] never happened again, and so that's why there was so much emphasis placed upon why the policy was where it was and why there was discussion upon it and why it was at length discussed that this was so important, so that the industry was not held hostage again like it was under the WANG case.”)). See also (CX0013 at 4 (noting that Mr. Townsend brought in a lawyer, gave a presentation, and made suggestions as to what could be done to avoid *Wang* problems in the future)).

363. Between May 1991 and September 1995, presentations on the patent policy were given at each meeting of the JC-42.3 subcommittee. (JX0005 at 3-4 (May 1991) (“Toshiba recommended that at each meeting a showing be made to explain what the intellectual property policies are . . . The important thing is disclosure”); Calvin, Tr. 1007-09 (essentially every meeting; gave presentation at each meeting during the week of meetings); G. Kelley, Tr. 2407; Rhoden, Tr. 325, 330; Williams, Tr. 785-86 (early presentation were quite lengthy); CX3136 at 134 (Meyer Infineon Tr.); JX0007 at 3 (September 1991); JX0010 at 11 (December 1991); JX0012 at 5 (February 1992); CX0034 at 3 (May 1992); JX0013 at 4 (July 1992); CX0042 at 3 (September 1992); JX0014 at 3 (December 1992) (noting that a draft of the revisions to the Manual or Organization and Procedure was shown); CX0045A at 2 (December 1992); JX0015 at 4 (March 1993); CX0050A at 2 (March 1993); JX0016 at 5 (May 1993); JX0017 at 3 (September 1993); CX0057A at 2; (September 1993); JX0018 at 3 (December 1993); CX0060A at 2 (December 1993); JX0019 at 4-5 (March 1994); JX0020 at 4 (May 1994); JX0021 at 4 (September 1994); JX0022 at 3 (December 1994); JX0025 at 3 (March 1995); JX0026 at 4 (May 1995); JX0027 at 4 (September 1995)).

364. The patent policy was presented at other JC-42 subcommittee meetings. (CX0018 at 7 (JC-42.5) (“It was suggested that at the beginning of each meeting the patent disclosure requirements be shown. Committee agreed.”); CX0021 at 3 (JC-42.5); CX0030 at 3 (JC-42.5); CX0044 at 3 (JC-42.5); CX0052 at 4 (JC-42.5)).

365. Beginning with the December 1995 meeting, participants discussed the patent policy during the plenary session. (JX0028 at 3 (“Patent Policies. This subject was covered in the Plenary Session in December 4”)).

366. Mr. Townsend cautioned participants to disclose “relevant patent applications.” (RX0356 at 2 (“members are cautioned to disclose their relevant patent applications.”); G. Kelley, Tr. 2406-07 (The JEDEC patent policy as explained by Jim Townsend required members to disclose “an issued patent that was available from the patent office, patent applications that were being worked on with the patent office, and items that were probably going to become patents.”); Rhoden, Tr. 332 (“Mr. Townsend would always make reference that disclosure was required of patent applications.”); Williams, Tr. 788-89; CX3136 at 134 (Meyer Infineon Tr.)).

2. The Patent Tracking List.

367. In addition to his presentations of the patent policy, Mr. Townsend also kept a patent tracking list, which was his compilation of patents and pending patents concerning which he had been made aware of through the course of the work inside JEDEC. (Rhoden, Tr. 325 (Townsend “also distributed copies of. . .his notes about patents that he had been made aware of through the course of the work inside JEDEC. He called that his patent tracking list”); Sussman, Tr. 1355 (JUDGE McGUIRE: Okay, now, whose job was it to transcribe any information on these sheets, these tracking sheets? I mean, who had that responsibility? Jim Townsend? THE WITNESS: Jim Townsend.”); McGrath, Tr. 9247 (“As I recall there were at times things that were listed just as a patent application on his list.”)).

368. The patent tracking list had multiple purposes, including record-keeping, a reminder to other participants of the patent issues that were on, and as an educational tool for those who were newcomers to the committee. (G. Kelley, Tr. 2407-08).

369. The patent tracking list was not a complete list of all patents and patent applications disclosed to the JC-42 committee. (G. Kelley, Tr. 2408 (“I know of instances where patent issues did not make the list.”)). *See, e.g.*, (CX0034 at 7 (Fujitsu LOC package patent application disclosed in May 1992 did not appear on patent tracking list as of December 1995); CX0711 at 169 (Fujitsu SSTL patent application disclosed in September 1995 did not appear on patent tracking list as of December 1995); JX0027 at 7-8 (Stacktek patent disclosed by Hewlett-Packard in September 1995 did not appear on patent tracking list as of December 1995)). *Cf.* (JX0028 at 15-18 (December 1995 patent tracking list)).

370. A memorandum sometimes was shown and circulated with the patent tracking list. The memorandum referred participants to the “existing rules of the EIA governing *patentable* matters” and reminded participants of their obligation to indicate “the intent of your company to patent or not patent the subject matter.” (CX0042A at 7) (emphasis added). *See also* (CX0336; CX0342; CX0347).

371. Although the memorandum apparently was addressed only to participants representing companies with patents already on the patent tracking list, inclusion of the patent tracking list in the minutes assured that every participant was aware of the rules. (CX0042 at 16-

17). Rambus received copies of the patent tracking lists that were included in the minutes. (CX0042A) (original bates numbers indicate that these minutes were produced from Rambus's files)).

372. The patent tracking list, memoranda and other patent policy related documents were included in the package of minutes and attachments. (JX0007 at 21-23; JX0012 at 28-30; CX0034 at 13-21; JX0013 at 14-18; CX0042 at 13-17; CX0042A at 7-9; JX0014 at 21-30; JX0015 at 24-30; JX0016 at 21-29; JX0017 at 12-14; JX0018 at 14-21; JX0019 at 17-30; JX0020 at 15-25; JX0021 at 14-25; JX0022 at 12-20; JX0025 at 18-26; JX0026 at 15-28; JX0027 at 20-27; JX0028 at 12-23; CX0021 at 12-21; CX0030 at 12-20; CX0044 at 8-16; CX0052 at 11-14; CX0079A at 6-10; JX0009 at 13-16; JX0012 at 28-30).

3. New Member Orientation.

373. JEDEC conducted new member orientations that included discussions of the patent policy when the new members had questions. (Rhoden, Tr. 341-42).

374. New members received copies of the JEDEC Manual of Organization and Procedure. (CX0208; Landgraf, Tr. 1702-04).

4. Sign-In Sheets.

375. Participants at each JEDEC meeting were required to record their names on the Meeting Attendance Roster or sign-in sheet. (CX0306; CX3136 at 135 (Meyer Infineon Tr.) (“Q. This [sign-in sheet] is what the members signed whenever they came to a JEDEC meeting, is that right, Mr. Meyer? A. They sign that sheet, yes.”); CX0356).

376. The attendees listed on the front page of each set of minutes was taken from the sign-in sheets. Thus, participants who appear as having attended the meeting necessarily must have signed the sign-in sheet. (Rhoden, Tr. 343 (“the people sign in, and then. . . they are transferred from this sheet then to the printed document, and you see at the head of all of the meeting minutes, the names that appear at the head of the meeting minutes would necessarily have signed a sheet just like this to be transferred to that point.”); Calvin, Tr. 1014-15 (“the policy is that there's a sign-up sheet that is sent around, and you sign in, either as a member, or as an associate. And that's how they track.”)).

377. After the Wang case (see CCF 362, 434), JEDEC also revised the sign-in sheet to further clarify the rule requiring disclosure of patent applications that may relate to JEDEC work. (CX0306 at 1; J. Kelly, Tr. 1934-35 (“the language that I'm referring to is ‘subjects involving patentability or patented items shall conform to the EIA policy’ . . . I think that first appeared on the sign-in sheet in the early 1990s time frame, around the time of the WANG case.”); CX0317 at 2 (March 1991 letter from Jack Kinn to Jim Townsend stating “Finally, subject to concurrence

by our legal counsel, I will have a statement on patents, included on the reverse of the sign-in sheet plus suggest to Council a statement go on the front, requesting the chairmen to read the excerpts at the beginning of every meeting.”)).

378. The sign-in sheet used during at least part of the relevant time period contained a written reminder at the top of the first page that “[s]ubjects involving *patentable* or patented item shall conform to EIA Policy.” (CX0306 at 1) (emphasis added); J. Kelly, Tr. 1934-35 (language appeared around the time of the *Wang* litigation)). Mr. Crisp recalled having seen the sign-in sheet with this language at some point while attending JEDEC meetings. (CX2094 at 439-40 (Crisp, Dep.)).

379. The term “patentable,” as used in the sign-in sheet, referred to anything over which an individual company claimed ownership or anything that they claimed could be patentable. (J. Kelly, Tr. 1935-36 (“patentable” meant patent applications), 1856-57 (sign-in sheet incorporates language from EIA Legal Guides); Rhoden, Tr. 344 (“My understanding is anything that an individual company claimed ownership, anything that they claimed could be patentable, then that references the patentable terminology that you see here.”); Sussman, Tr. 1350-51 (language in sign-in sheet is “all inclusive.”)).

380. The sign-in sheet also referred participants to EIA general counsel concerning any doubtful questions. (CX0306 at 1; J. Kelly, Tr. 1857-58, 1937-38 (receives questions concerning the patent policy approximately once every other month)).

381. EIA general counsel is the official responsible to final interpretation of the patent policy. (J. Kelly, Tr. 1857-58, 1915, 1939 (Mr. Kelly’s interpretation controls)).

5. Meeting Minutes.

382. JEDEC meeting minutes contained discussions of the terms of the patent policy. (CX0045A at 13) (showing proposed revisions of the JEDEC Manual of Organization and Procedure); CX0064A at 2 (discussion of request by Texas Instruments for clarification of the patent policy)).

6. Ballots.

383. JEDEC ballots required that participants who were "aware of patents involving this ballot, please alert the Committee accordingly during your voting response.” (JX0059 at 2).

384. The term “patents” as used in JC-42.3 subcommittee ballots (see, e.g., JX0059 at 2) is not limited to issued patents; it includes all IP for which a patent had been applied for or was about to be applied for, as well as issued patents. (Sussman, Tr. 1391-92).

385. This language was included on every ballot during the time Rambus was a member. (Rhoden, Tr. 355-56 (ballots between 1991 and 1996); Williams, Tr. 812-13 (ballots included this “verbiage” between 1991 and 1993)).

386. A participant was required to disclose patent information at this point in the process if “it had not been disclosed to the committee before” this time. (Rhoden, Tr. 356-57 (ballot did not mark the time that participants were required to disclose)). *See also* Williams, Tr. 812-13 (“This is like a last ditch effort to get a disclosure and to remind people that they have that obligation even when voting”).

7. Manuals.

387. The rules of JEDEC are provided in the EIA Legal Guides, EIA Manuals, and the JEDEC Manual of Organization and Procedure. (CX0202; CX0204; CX0203A; JX0054; CX0205; CX0205A; CX0208; J. Kelly, Tr. 1824-25 (citing EP-3, EP-7 and EIA Legal Guides)).

388. EIA rules and JEDEC rules concerning disclosure and licensing of patents are consistent. (J. Kelly, Tr. 1915-16 (“I’m not aware of any conflicts between the JEDEC rules and the EIA rules”), 1919-20 (“I think that those terms were used interchangeably, EIA patent policy and JEDEC patent policy.”)).

(A). EIA Legal Guides.

389. EIA participants are required to comply with the rules and policies set forth in the EIA Legal Guides. (J. Kelly, Tr. 1829-32 (participants obligated to read and follow EIA Legal Guides)).

390. The Legal Guides were made available to all EIA and JEDEC participants. (J. Kelly, Tr. 1830-31 (“Copies of this document were also available through my office, as well as through the Publications Index.”)).

391. Part I of the EIA Legal Guides includes “general guides applicable to all Electronic Industries Association activities. They are required to be read and followed by all members of the Association and staff, chairmen and members of all committees, sections divisions, and other EIA-sponsored groups.” (CX0202 at 4; CX0204 at 3; J. Kelly, Tr. at 1830).

392. Part II of the EIA Legal Guides “are special guides that relate to engineering standardization programs uniquely.” (CX0202 at 5; CX0204 at 4; J. Kelly, Tr. 1828).

393. Parts I and II of the EIA Legal Guides apply directly to JEDEC activities and the activities of JEDEC Committees. (J. Kelly, Tr. 1829).

394. Part III of the EIA Legal Guides relate to market research activities. Because JEDEC has never engaged in market research activities, Part III of the EIA Legal Guides is not applicable to JEDEC. (J. Kelly, Tr. 1828-29).

395. The Legal Guides set forth the basic rules under which EIA and JEDEC programs must operate, including the duty to act in good faith and the requirement that EIA and JEDEC programs be operated in a manner that does not result in anticompetitive effects. (CX0205 at 5).

(B) EP-3.

396. EP-3 is the EIA Manual for Committee, Subcommittee and Working Group Chairmen and Secretaries. (CX0203A at 1; J. Kelly, Tr. 1859-60 (purpose of EP-3 was to guide chairs on how to conduct meetings)).

397. EP-3 prohibits the inclusion of patented items in EIA/JEDEC standards unless the patent information has been disclosed and the patent owner has agreed to grant licenses on RAND terms. (CX0203A at 11 (“No program of standardization shall refer to a product on which there is a known patent unless all the technical information covered by the patent is known to the [committee]. The committee chairman must have also received a written expression from the patent holder that he is willing to license applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination.”) (also cross-referencing EP-7)).

398. EP-3 was made available to all EIA and JEDEC participants. (J. Kelly, Tr. 1878).

(C) EP-7-A.

399. EP-7 is the Style Manual for Standards and Publications of EIA, TIA, and JEDEC. (JX0054 at 1).

400. EP-7 requires JEDEC members to avoid patented items or process unless disclosure has been made and the owner of the intellectual property agrees to RAND licensing. (JX0054 at 9 (“Avoid requirements in EIA standards that call for the exclusive use of a patented item or process. No program standardization shall refer to a patented item or process unless all the technical information covered by the patent is known to the [committee]. The committee chairman must have also received a written expression from the patent holder that he is willing to license applicants under reasonable terms and conditions that are demonstrably free of any unfair discrimination”)).

401. The term “patent” as used in EP-7 means issued patents as well as patent applications. (J. Kelly, Tr. 1886-88).

402. EP-7 was made available to all EIA and JEDEC participants. (J. Kelly, Tr. 1878).

(D) JEDEC Manual of Organization and Procedure.

403. The JEDEC Manual of Organization and Procedure was directed to all members. (CX0205 (JEP21-H) CX0208 (JEP21-I); J. Kelly, Tr. 1913-14 (purpose of JEP21 was to provide sector-specific guidance to JEDEC engineering committees); 1914-15 (the JEDEC manual was “made available to all new members at the time they became members. It was also made available to committee chairs when they assumed their responsibility as committee chairs. It was also brought to meetings by the staff people who were responsible for the committees and available at the meeting if anyone cared to review the document.”); Sussman, Tr. 1349 (never heard of Manual of Organization and Procedure referred to as “Chairman’s Manual.”); Landgraf, Tr.1702-04 (never heard of Manual or Organization and Procedure referred to as “Chairman’s Manual;” “it was given out by Mr. Townsend to all new members from companies. So, every time a company either joined JEDEC or they changed members, they would get a new copy of this, this document.”); Rhoden, Tr. 313 (“never” heard of Manual of Organization and Procedure referred to as “Chairman’s Manual.”)).

404. The Manual of Organization and Procedure is the manual by which all JEDEC activities are conducted. (Rhoden, Tr. 313 (“This is the manual that is for all of the participants inside JEDEC to operate and for JEDEC committees to operate under.”); Landgraf, Tr.1702 (“Manual 21-I is the standards and policies.”); G. Kelley, Tr. 2385 (“I would control the agenda and make sure that. . . the meeting was run by JEDEC's manual of operation and procedures.”); Williams, Tr. 790 (“I don't know exactly what the JEP stands for, but it is a manual that guides the policies of JEDEC, how the JEDEC ought to operate” including the patent policy)).

(1) JEP21-H.

405. JEDEC Manual of Organization and Procedure 21-H (“JEP21-H”) was the version in effect between 1991 and late 1993. (J. Kelly, Tr. 1913-14 (21-H was in effect in 1990); CX0208 at 1 (published October 1993)).

406. JEP21-H specifically incorporates the EIA Legal Guides. (CX0205 at 14; J. Kelly, Tr. 1916)).

407. JEP21-H noted that EIA Legal Counsel was authorized to advise the committees concerning interpretation of the Legal Guides. (CX0205 at 14 (“EIA Legal Counsel can advise the Counsel and Committees from time to time concerning interpretation of Legal Guides”); J. Kelly, Tr. 1916-17)).

(2) JEP21-I.

408. Beginning as early as January 1992, JEDEC began considering making revisions to its manual of organization and procedure. (JX0011 at 5; CX0035 at 9 (“the secretary [of the

JEDEC Council] outlined the genesis for the changes the fact that a new set of policy statements and guidelines have been written that will be circulated to the Council for review and comment”)).

409. The 1993 revisions were motivated by the allegations that Wang made that it did not understand the patent policy to apply to patent applications. This caused immediate concern in the JEDEC organization, and there was an initiative almost from that moment forward, when that defense or allegation was first raised, to clarify the patent policy so that it would be clear in the future that "patent" meant patents and patent applications. (J. Kelly, Tr. 1930-32 (“there was litigation that arose out of a JEDEC standard-setting activity involving WANG Technologies. . . one of the defenses or allegations that WANG made in that case was that they did not understand the patent policy to apply to patent applications. This caused immediate concern in the JEDEC organization, and there was an initiative almost from that moment forward. . .to clarify the patent policy so that it would be clear in the future that ‘patent’ meant patents and patent applications, and there would never be a repetition of the situation presented in the WANG case.”)).

410. The proposed revisions were shown and discussed at JEDEC meetings. (JX0014 at 25; Williams, Tr. 791 (discussions led by Mr. Townsend), 892 (“I do know that we did discuss [the revisions] at multiple meetings.”); J. Kelly, Tr. 1936-37 (Mr. Townsend was personally involved in revision process)).

411. The proposed revisions to the language of the Manual of Organization and Procedure were discussed at the December 1992 42.3 meeting. (CX0045A at 11-14; JX0014 at 23-27; G. Kelley, Tr. 2416-17).

412. The final revisions to the language of the Manual of Organization and Procedure were discussed at the September 1993 JC-42.3 meeting. (JX0017 at 12-14).

413. Richard Crisp of Rambus attended meetings at which the revisions were shown and discussed (JX0014 at 1; JX0017 at 1). David Mooring of Rambus also attended the December 1992 meeting. (JX0014 at 1-2).

414. In October 1993, version “I” of the JEDEC Manual of Organization and Procedure was published. (CX0208 at 1).

415. The 1993 revisions make more explicit that the disclosure rule applied to applications and conformed with the manner in which the EIA/JEDEC patent policy had been interpreted and applied prior to October 1993. (J. Kelly, Tr. 1927-28 (“This manual [21-I] made more explicit the requirement to disclose both issued patents as well as patent applications”); G. Kelley, Tr. 2411 (“another change was the inclusion of patent applications in the wording of the patent section of our document”)).

416. One of the revisions provided additional clarity that the patent policy required disclosure of patent applications. While the wording the manual was revised, it did not reflect a substantive change in the policy. (CX2191 at 5 (notes of NEC representative describing “main” change to the manual without any mention of the patent policy); G. Kelley, Tr. 2415-16 (“Q. Based on your understanding of the JEDEC policy in the early 1990s, and based on your understanding as one of the individuals involved in working on the addition to the JEDEC manual, did you understand that the work that you were doing in the manual would change in any way the substance of the JEDEC disclosure policy? A. No.”); J. Kelly, Tr. 1927 (“this was a restatement of the patent policy, and it in no way varied the policy itself. It changed some of the verbiage.”); CX2057 at 177-78 (Meyer 12/13/00 Dep.) (“Q. But did the written policy itself change at any time between January of '91 and December of '96? A. We changed it. JEDEC council changed the wording. Q. Did that in your mind change the policy? A. No, it did not change the policy.”); Williams, Tr. 791-92 (“the policy wasn't what was being revised; only the manual was being revised. The policy, even from my very first time at JEDEC, was always the same, and that is you needed to disclose if you felt that you had IP. . . on something that was being discussed at JEDEC.”)).

417. Beginning in January 1992, the JEDEC Council worked on a set of revisions for the JEDEC manual. One of the revisions included a specific reference to patent applications in the wording of the patent section of the manual. (JX0011 at 5; G. Kelley, Tr. 2410-11). Throughout 1992 and into 1993, the Council circulated and discussed draft revisions to the manual. (CX0035 at 9; CX0039 at 12; CX0046 at 9; G. Kelley, Tr. 2411-16, 2419-23). In May 1993 and again in September 1993, the JEDEC Council reviewed and approved the revisions to the JEDEC manual. (CX0054 at 7; CX0055 at 2; G. Kelley, Tr. 2423-28).

418. JEP21-I was made available to all JEDEC participants. (J. Kelly, Tr. 1923-24; Landgraf, Tr. 1702-04 (“I'm not sure if I received this at my first meeting or second or third meeting, but it was given out by Mr. Townsend to all new members from companies”); Richard Crisp, Rambus' JEDEC representative, was provided a copy of the JEDEC 21-I Manual. (Crisp, Tr. 2977-78; CX0208A)).

G. Remedies for Violations.

419. There is no mechanism for EIA or JEDEC to force members to comply with the patent policy or any other rule. (J. Kelly, Tr. 1966 (“the entire process is voluntary, and as a voluntary standards development organization, we really don't have the power to impose sanctions against members who don't comply with the policy.”), 2006-07 (“we could write to the company and say we're very disappointed in your behavior. What we couldn't do is to impose sanctions against the company. . . as a practical matter, there is very little we can do other than a slap on the wrist to enforce these rules.”); Rhoden, Tr. 610-11 (“your actions, by definition, have to be voluntary, because there is no way that EIA or any of the organizations could, in fact, force you to do it.”)).

420. JEDEC is unable to impose sanctions on companies because participation in JEDEC provides a competitive advantage to companies and, therefore, must be open even to companies that violate the patent disclosure rules. (J. Kelly, Tr. 2006-07 (“participation in a JEDEC standard-setting activity confers a significant competitive advantage on the participants, and were we to act in a way that would deny them that competitive advantage, EIA and JEDEC would be subject to lawsuits for violation of the antitrust laws ourselves.”)).

421. JEDEC’s primary recourse is to remove the subject intellectual property from its standards. (J. Kelly, Tr. 2007-08 (“we could withdraw the standard”); G. Kelley, Tr. 2431-32 (“If the JEDEC organization . . . had found out that there was patent material that applied to a standard that we had approved without the knowledge of that patent material, then the validity of that standard was in question and we often either we removed the standard or expected the patent issue to be resolved.”), 2464 (“patent issues are almost terminal for a ballot to pass”)). *See, e.g.*, CX0346 at 1 (“TI did not disclose to the Committee that they had this patent until JEDEC approved some standards. The Committee is very suspicious of TI because TI did not pursue any requests for royalties until after the JEDEC standard was approved. . . A new ballot was issued . . . to rescind the standards affected by the TI patent.”).

422. JEDEC members, including Rambus, understood that failure to disclose means that the patent owner may be unable to enforce the patent against the standard. (CX1942 at 1 (“I [Lester Vincent] said there could be equitable estoppel problem if Rambus creates impression on JEDEC that it would not enforce its patent or patent [applications].”); CX1937 (billing records of Lester Vincent noting “Conference with Richard Crisp and Allen Roberts concerning equitable estoppel issue with respect to JEDEC.”); CX1990 at 1 (Lester Vincent forwarding materials to Rambus concerning Dell consent decree); CX0858 at 2 (“I [Richard Crisp] understand the concerns about the patent policy and some potential exposure we could have in the event of future litigation. [Equitable Estoppel and Laches]); Appleton, Tr. 6329 (“if [a company] fail[ed] to disclose [patents or patent applications], then. . . they couldn't come back later and try to enforce those against the standard that had been developed”); Lee, Tr. 6598-99 (“if [a company] failed to disclose the patent that may relate to the work of the committee and if it was adopted into the standard, that [company] would forego their right to enforce the patent against the standard.”); Rhoden, Tr. 611-12 (“any company that did not disclose necessarily gave up their right to that IP as it related to the standard. That is what I understood.”)).

H. Incidents of Non-Disclosure & JEDEC’s Response.

423. There have been occasions in which JEDEC participants did not disclose patent information that might related to JEDEC work. These incidents have resulted in either (1) rescission of the standard (Quad CAS); (2) the selection of an alternative standard (SEEQ); or (3) litigation (Wang). (See CCFE following).

1. Quad CAS.

424. The Quad CAS incident involved the alleged failure of Texas Instruments to disclose properly its issued patent relating to Quad CAS technology. The issue arose at the JC-42.3 subcommittee meeting in September 1993, when Micron accused Texas Instruments of having failed to comply with the JEDEC disclosure policy. (JX0017 at 6; CX0346 at 1 (JEDEC Secretary Ken McGhee writing to John Kelly that “TI did not disclose to the Committee that they had this patent until JEDEC approved some standards. The Committee is very suspicious of TI because TI did not pursue any requests for royalties until after the JEDEC standard was approved.”); CX0452 (McGhee 11/3/93 Letter distributed to all JC-42.3 members a memo, discussed by Jim Townsend at the September 1993 meeting, drawing their attention to “the existing rules of the EIA governing patentable matters,” and reminding them of their obligation to relevant “patents held and applied for”); Williams, Tr. 776-77 (“this was a case where it was found out that TI had. . . had a patent on the quad CAS device that had just been standardized or was in the process of being standardized, and it did pass, became a standard. . . I can't remember exactly where it was, but I remember a great uproar in the committee based upon it.”); Sussman, Tr. 1335 (“they proposed a quad CAS, and after the part was standardized, after some modules were standardized, then the company revealed its patent position, and we were rather upset. We had spent a lot of time and energy, wasted a lot of time and energy.”)).

425. Micron Corporation notified the Committee that TI had asserted patent claims against it and that TI was going to charge license fees and royalties for the use of the concept of Quad CAS. (G. Kelley, Tr. 2464). At the time there were pending Committee ballots pertaining to the use of Quad CAS as part of the SDRAM standard; when TI refused to comment on the patent issues pertaining to these ballots, the Committee determined unanimously to place the ballots on hold until the patent issue was resolved. (JX0017 at 6; G. Kelley, Tr. 2465-66). The Committee also voted to prepare a ballot to rescind portions of previously-passed standards pertaining to Quad CAS. (JX0017 at 7; G. Kelley, Tr. 2466-68). (CX2059 at 181-82 (Karp, Infineon Dep.) (Samsung, most likely Joel Karp, seconded the Micron motion to remove the Quad CAS standards.)).

426. The Quad CAS issue arose again at the December 1993 meeting of the JC-42.3 subcommittee, when there was an extensive discussion of the issue. Members stated that the key issue was the disclosure to the JC-42.3 subcommittee of the relevant patents and that Texas Instruments was not following the JEDEC disclosure policy. (JX0018 at 8 (Mr. Kelley noted that the letter from TI [explaining its position] does not address the key issue that the Committee was not informed of TI's patent. TI was asked why the Committee was not informed of the patents. TI did not respond because litigation is going on. . . . –Samsung: We are reluctant to vote yes [on the ballot relating to the proposed standard] because we do not think TI is following the patent policy. . . . Micron noted that all companies should have equal access to a standard developed by the Committee. . . . –Sanyo: It is understood that if and when TI conforms to the EIA policy, work should continue. . . . if TI has knowingly and intentionally violated the

EIA/JEDEC patent policy, EIA may need to consider additional actions/discussions with TI.); G. Kelley, Tr. 2475 (IBM may not participate if information being hidden); G. Kelley, Tr. 2470-72 (describing discussion that took place at the meeting)). *See also* (CX2955 at 2 (Joel Karp letter voting to rescind Quad CAS standards because “TI is unwilling to provide such a demonstration [of reasonable terms and conditions free of unfair discrimination] for review by potential licensees.”)).

427. The following month, Gordon Kelley of IBM wrote to Buf Slay of Texas Instruments, expressing concern that TI’s conduct could have an adverse impact on JEDEC’s work. (CX2384 (“I am and have been concerned that this issue can destroy the work of JEDEC. If we have companies leading us into their patent collection plates, then we will no longer have companies willing to join the work of creating standards; i.e., widely used designs. . . .If we allow JC-42 standards to be used for patent collection purposes, then we do a great disservice to the very sort of industry that feeds us. . . .If we on JEDEC council do not deal with [this issue] completely, we set ourselves up for bigger problems in the future.”)); CX3136 at 142 (Meyer Infineon Tr.) (recalling Mr. Kelley’s “patent collection plate” testimony); Appleton, Tr. 6331-32 (failure to disclose would discourage Micron from participating)).

428. At the following meeting in March 1994, the issue was revisited. TI requested a clarification of the Committee’s interpretation of the patent policy; in response to a question from the chairman, members stated unanimously that the policy was clear. (JX0019 at 5 (“Applicability of patents to use of JEDEC standards was discussed. The issue is warning, IBM noted. Failure to disclose a patent prevents the Committee from considering the standard. The Committee was asked if the patent policy is clear. The Committee felt it was clear.”)); CX2375 at 1-2 (notes of Mark Kellogg summarizing the Quad CAS discussion at the March 1994 meeting); Kellogg, Tr. 5028-29 (recalling that vote was unanimous that patent policy was clear)).

429. EIA legal counsel issued a memorandum stating that “[w]ritten assurance must be provided by the patent holder when it appears to the committee that the candidate standard may require the use of a patented invention.” (CX0353 at 1 (emphasis in original); *see also* CX0355 (memorandum from JC-42 Secretary, Ken McGhee, forwarding Mr. Kelly’s memorandum to all members of the JC-42 committee. (CX0355)).

430. Richard Crisp was present at the September 1993, December 1993, and March 1994 JC-42.3 subcommittee meetings, and reported details of the Quad CAS discussion back to others at Rambus. (CX0710 at 1 (TI was chastised for not informing JEDEC that it had a 1987 patent on quad CAS devices. . . . The bottom line is that all quad CAS devices will be removed from standard 21C.)).

431. Pursuant to these discussions, the JC-42.3 subcommittee rescinded the Quad CAS standard. (JX0018 at 9 (ballot to remove standard passed); CX0710 at 1 (Richard Crisp noting that the standard will be rescinded); G. Kelley, Tr. 2479-80 (conveying to the committee the

importance the Quad CAS lesson in light of rescission of standard); Williams, Tr. 776-77 (standard rescinded).

432. In early 1995, Texas Instruments agreed to comply with the JEDEC patent policy and removed their representative who failed to provide the Quad CAS disclosure. (JX0025 at 3 (“A letter from TI was received at JEDEC complying with the EIA patent policy”); G. Kelley, Tr. 2486). The Quad CAS ballot was taken off hold. (JX0025 at 3).

2. SEEQ.

433. A company named SEEQ proposed a JEDEC standard called silicon signature. (Sussman, Tr. 1338). SEEQ owned two patents relating to the technology, but disclosed and offered to license only one. (Sussman, Tr. 1338-39 (SEEQ “was telling us about silicon signature and offering it as a royalty-free license to anyone who wanted it, hoping that just as soon as we standardized this, the second patent, which would be die trace, which he had not said anything about, but because it was almost identical, would be insisted upon by the customers, and [SEEQ] could put a tax on us.”)). Upon learning of SEEQ’s second patent, the committee was willing to standardize the SEEQ technology, provided that SEEQ agreed to reasonable licensing terms. (CX0003 at 4 (“The Committee felt they would like to proceed with [the SEEQ technology] for PLDs as long as reasonable rates for use remained and that Seeq would put their position in writing. There was some question about whether die trace was included in the patent release.”)). When the committee learned that the second patent was not included in the patent release, JEDEC chose to standardize on a different technology. (Sussman, Tr. 1338-39 (“What we did, as we found out about the second application, is that we did not standardize either of [the SEEQ patents]. We standardized an alternate methodology.”); *see also* CX0711 at 188 (“So the conclusion I reach here is that we can abide by the patent policy on a case-by-case basis. . . The things we should not do are to not speak up when we know that there is a patent issue, to intentionally propose something as a standard and quietly have a patent in our back pocket we are keeping secret that is required to implement the standard and then stick it to them later (as WANG and SEEQ did.”)).

3. Wang.

434. Failure to disclose a relevant patent application precipitated litigation in the Wang matter. Wang failed to disclose a patent relating to memory modules and later attempted to enforce the patent against the industry. (Williams, Tr. 787 (“they [Wang] were part of the committee, they had helped set a standard, and then they went out and enforced their patents against everybody in the industry who used a SIMM module.”); Sussman, Tr. 1338 (“that ended up in a rather lengthy litigation, crossed multiple houses and cost the industry millions of dollars before the patent was found to be invalid.”); Landgraf 1697-98; JX0020 at 4 (“It as noted that the WANG patent case is coming up for trial on June 14.”)).

I. The Relationship to the ANSI Rules.

435. The American National Standards Institute (“ANSI”) is an umbrella organization that accredits standards-setting organizations. (J. Kelly, Tr. 1947-48 (“ANSI is one of several organizations in the United States that accredits other organizations to develop standards.”)).

436. ANSI also has the authority to adopt certain of the standards that are submitted to it by its qualified organizations for adoption as American national standards. (J. Kelly, Tr. 1947-48).

437. EIA has been a dues-paying member of the American National Standards Institute since the late 1970s. (J. Kelly, Tr. 1948-49). EIA forwards certain standards developed by EIA sectors to ANSI for adoption as American National Standards. (J. Kelly, Tr. 1948-49).

438. John Kelly was a member of the ANSI patent policy working group from 1990 until 2002 and was personally involved in the discussions and deliberations leading to the final approval of the ANSI guidelines. (J. Kelly, Tr. 1950-51 (“I got involved at a relatively late stage in the process, but I participated fairly actively in the discussions and the deliberations that led up to the final approval of the guidelines by the working group. And I have been also been involved in a number of discussions over the ensuing ten years about the guidelines and proposed amendments to the guidelines.”)).

439. The EIA patent policy is in compliance with, but not identical to, the ANSI patent policy guidelines. (J. Kelly, Tr. 1957-58).

440. ANSI has audited EIA and has always found EIA in compliance with ANSI patent policy during those audits. (J. Kelly, Tr. 2148-49 (“The patent policy is consistent with the ANSI patent policy, and my basis for saying that is that EIA has been audited by ANSI in general in terms of the record retention and also in terms of its written policies and never been found not to be in compliance with the ANSI patent policy.”), 2154-55 (“my understanding is we are in compliance with the policy and have been.”)).

441. The ANSI patent policy guidelines do not require rigid adherence to every single aspect of the ANSI patent policy. (RX1712 at 3 (ANSI guidelines “are suggestions -- adherence is not essential for standards developers to be found in compliance with ANSI's patent policy. Rather, this is an effort to identify possible procedures that a standards developer may wish to adopt, either in whole or in part, for purposes of effectively implementing the patent policy. Additional or different steps may also be selected for such purposes.”); J. Kelly, Tr. 1956-57 (“we were trying, as a member of the patent policy group, to establish some general guidance for the benefit of standards developers that they could either follow or not follow, in whole or in part, and we're emphasizing here that. . . standard developers had the option of adopting additional or different steps from those suggested from the guidelines that might be appropriate

in the case of their own standards development activities.”)).

442. One aspect of the EIA/JEDEC patent policy that goes beyond the requirements of ANSI’s patent policy is that the EIA/JEDEC policy requires the disclosure of patent applications as well as issued patents, whereas the ANSI patent policy requires the disclosure only of issued patents. (CX0208 at 19; J. Kelly, Tr. 1957-58 (“there is a material difference between the ANSI policy and the EIA/JEDEC policy, and that is that the EIA/JEDEC policy requires the disclosure of patent applications as well as issued patents.”)).

443. The EIA/JEDEC patent policy is consistent with the ANSI patent policy guidelines, notwithstanding the different treatment of patent applications. (J. Kelly, Tr. 1959). ANSI guidelines specifically acknowledge that a standards development organization may wish to at least consider including patent applications as well as patents in their patent disclosure policy. (RX1712 at 8 (“Similarly, a standards developer may wish to encourage participants to disclose the existence of pending U.S. patent applications relating to a standard under development.”); J. Kelly, Tr. 1959-60, 2154 (“there are options that individual standard developer organizations can adopt that are not identical to the ANSI policy to address specific issues. . . an example that we specifically give in these guidelines is that standard developers may elect to require the disclosure of patent applications as well as issued patents.”)).

444. Paragraphs 444 to 499 are unused.

IV. The Development of JEDEC DRAM Standards.

A. The First Generation SDRAM Standard.

1. The Origins of the Standard.

500. “Asynchronous DRAM” is a term that is used to describe DRAMs that are driven off the RAS and CAS signals where the RAS and CAS actually control the operation of the DRAM rather than a clock. (Jacob, Tr. 5394).

501. Page mode and extended data out or “EDO” DRAMs are types of asynchronous DRAM (Sussman, Tr. 1469; Polzin, Tr. 4031; Horowitz, TR. 8581). In the late 1980's page mode and EDO DRAMs were commonly used in the industry. (Sussman, Tr. 1361). Page mode and EDO DRAMs were standardized at JEDEC. (Sussman, Tr. 1362; Prince, Tr. 9020-9021).

502. In the late 1980's, microprocessors were demanding more performance out of DRAMs. (Kelley, Tr. 2388-2389).

503. In order to respond to this demand and to ensure that the new JEDEC standard would result in common parts that were plug compatible, the JC-42.3 subcommittee began to standardize certain aspects of DRAM performance and design relationships. (CX0035 at 14; G. Kelley, Tr. 2390-2391). Prior to that time, JC-42.3 work had generally focused on standardizing the location of pins, also known as pin-out diagrams. (G. Kelley, Tr. 2388).

504. A new generation of memory was needed because the industry anticipated that microprocessor and computer speeds would increase and the industry demanded memory that could operate at the same speeds. (CX2088 at 291-292 (Meyer, Infineon Trial Testimony, April 25, 2001)).

505. JEDEC entertains a number of proposals by members when working toward a standard for a new device. (Rhoden, Tr. 415 (“[W]hen we're working on a particular device or whatever, there will be proposals that are made that come from usually a number of different companies. Sometimes multiple proposals or multiple ideas, if you will, come from a particular company, but more often than not, it comes from a variety of companies. So, you will have several different proposals that will be made inside JEDEC as to what path we should take for the next improvement cycle, if you will, of what we're working on”)).

506. JEDEC members then decide which of these ideas to pursue. (Rhoden, Tr. 415-416 (“Well, the differences of opinion are something that people have to investigate to see if particular -- if the particular proposals are viable or if they -- it usually winds up being that engineers themselves come up with the ideas, so they're almost always reasonable ideas, and it's just a question of then deciding which path they're going to take.”)).

507. One option considered by the JC-42.3 subcommittee was to continue to develop a new generation of EDO DRAMs. (CX0711 at 1 (“HP, Micron and Mitsubishi are now saying that EDO is the right thing to do that it offers better performance than DRAM at a much lower cost than SDRAM.”)).

508. JEDEC also began to consider a DRAM that had been developed by IBM called “High Speed Toggle” (G. Kelley, Tr. 2584-2585). High speed toggle is also known as “HST”. (Kelley, Tr. 2441).

509. HST was a partially asynchronous and partially synchronous part, in that it had asynchronous inputs but synchronous outputs. (Kellogg, Tr. 5173 (“So what high-speed toggle was was a memory device that had asynchronous inputs. In other words, it had the fastest possible access path and clocked outputs, and the clock itself was a clock that transferred data on both edges, such that we could run a relatively low-speed clock in the memory device. So asynchronous, command and address, clocked output, clocking data on both edges of the clock.”)); Rhoden, Tr.437 (Q. Now, was IBM proposing a synchronous device or asynchronous device or was it something different? A. Well, in terms of data, it was a synchronous device because of the nature of how -- remember I said, I said it's a CAS clock. It's a function that's fundamentally synchronous. So, as we would toggle the CAS signal, column, clock, whatever -- whichever name you want to call it, you would get data out on -- from the rising edge and from the falling edge in a synchronous fashion.)).

510. In HST, IBM proposed to transfer data on both edges of the clock signal. (Kellogg, Tr.5173; Sussman, Tr. 1381; Rhoden, Tr. 436-437); CX2080 at 242 (Karp, Micron Dep.)(recalls that the toggle mode presentations had “ some relationship to both edges of a clock.”).

511. IBM and other companies continued to make HST presentations at JEDEC during 1990 and 1991. (JX0002 at 92 (IBM presentation of high speed toggle); JX0003 at 56-57 (IBM presentation of high speed toggle); JX0003 at 7 (motion to send IBM HST out on survey passed unanimously); CX0316 at 1 (DRAM TASK GROUP TOGGLE MODE Questionnaire); JX0004 at 6 (approval of issuance of HST survey ballot); CX0314).

512. At the May 9, 1991 JC-42.3 meeting, the subcommittee passed a motion to ballot the IBM HST presentation. (JX0005 at 12). At the same meeting Siemens also made a HST presentation that was like the IBM HST except it used a G\ pin instead of a new toggle pin. (JX0005 at 12).

2. The Decision to Adopt a Fully Synchronous DRAM Standard and a Single Edge Clock.

513. At the JEDEC JC-42.3 meeting in May 1991, Howard Sussman of NEC proposed a fully synchronous DRAM to JEDEC for the first time. (Sussman, Tr. 1364; CX2088 at 272-275

(Meyer, Infineon Trial)).

514. Mr. Sussman proposed to use a single edge clock to input and output data and a programmable mode register to set CAS latency and burst length. (Sussman, Tr. 1365-1367 and 1373-1375).

515. At the next JC-42.3 meeting on September 18, 1991, the subcommittee voted in favor of the IBM HST technology. However, there were four no votes and a number of comments. NEC and Samsung commented that the use of two clock edges can limit speed. (JX0007 at 8 (“NEC: Two edge trigger limits speed. . . . Samsung: Clock generation is difficult – two edge clock limits speed”). The subcommittee decided to put the ballot on hold until more resolution to the comments could be made. (JX0007 at 9).

516. Also at the JC 42.3 meeting on September 18, 1991, Mr. Sussman made a second presentation of NEC’s SDRAM proposal. (JX0007 at 13 and 160-162; CX2088 at 276 (Meyer, Infineon Trial Tr. ((4/25/01)). A number of other companies also presented synchronous DRAM proposals at this meeting, including Texas Instruments (JX0007 at 13 and 163-176 (first showing of an SDRAM proposal)), Toshiba (JX0007 at 13 and 177 (a first showing with a similar package and pinout to the NEC proposal)) and Hewlett Packard (JX0007 at 013(a presentation on SDRAM features)).

517. At the first JEDEC JC-42.3 meeting on December 4-5, 1991 (the first JEDEC meeting attended by Rambus (see CCF 867)), Mark Kellogg of IBM made a presentation comparing HST to synchronous DRAMs. (JX0010 at 5 and 84 (“Options: 1) high speed toggle (already passed ballot, on hold)”); Kellogg, Tr. 5172-5173).

518. Also at the JC-42.3 meeting of December 4-5, 1991, Howard Sussman presented the results of a non-JEDEC meeting that had been held in Portland, Oregon on October 24, 1991 to discuss high bandwidth DRAM. (JX0010 at 4; Sussman, Tr. 1373). The conclusion from that meeting was that a fully synchronous DRAM with all signals referenced to a single positive clock edge would best meet system requirements. (JX0010 at 50).

519. At the next JC-42.3 meeting held on February 27-28, 1992 NEC, Hitachi, Fujitsu, Toshiba, Mitsubishi and Sun all made presentations proposing to use fully synchronous DRAMs. (JX0012 at 39, 42 (NEC presentation); JX0012 at 69 (Hitachi presentation); JX0012 at 76 (Fujitsu presentation); JX0012 at 94 (Toshiba presentation); JX0012 at 60 (Mitsubishi presentation); (JX0012 at 110 (Sun Presentation)).

520. No further action on HST was taken at the February 1992 JC-42.3 meeting. High Speed Toggle items continued to be listed, however, on an active items list presented at the February 1992 meeting by the Subcommittee Chairman. (JX0012 at 19 (“Item 312.1 ... Toggle Mode, Ballot 91-119, IBM”), 20 (“Item 358 . . . G\Toggle Mode, Siemens”)).

521. At a DRAM Task Group meeting of April 9-10, 1992, NEC, Fujitsu, Toshiba, Samsung, Hitachi and Mitsubishi presented proposals for a fully synchronous DRAM. (CX0034 at 33 (NEC presentation; Fujitsu presentation), at 35 (Toshiba presentation; Samsung presentation; Hitachi presentation); at 36 (Mitsubishi presentation).

522. At the April 1992 DRAM Task Group meeting, IBM proposed a slightly modified version of its HST technology. (CX0034 at 32 (“IBM: ... A Synchronous RAS/CAS with Synchronous DQ * dual clock edge...”); Kellogg, Tr. 5175).

523. Following the April 1992 DRAM Task Group meeting, the JC-42.3 subcommittee decided to pursue a fully synchronous DRAM rather than IBM’s toggle mode. (G. Kelley, Tr. 2515).

524. Following the April 1992 DRAM Task Group meeting, the JC-42.3 Subcommittee decided to use a single edge rather than a dual edge clock (i.e., to input and output data only on the rising edge of the clock, rather than on both the rising and falling edges of the clock). (G. Kelley, Tr. 2515) The concept of using dual edge clocking “had generated quite a bit of interest.” Rhoden, Tr. 462-63 (“... actually we came very close to including it in the original SDRAM standard . . .)?”

525. The subcommittee decided to postpone implementing dual edge clocking until a later standard in part because the subcommittee believed current requirements could be met with a single edged clock. (G. Kelley, Tr. 2515 (“At the meeting, we discussed the advantages of a double-edged clock versus a single-edged clock and we decided as a group that we could meet the requirements of the high-performance systems for the next-generation DRAM without needing a double-edged clock for that doubling of the performance and that we would reconsider the double-edged feature in the next generation.”); Rhoden, Tr. 463-464)

526. Another factor in the decision to postpone implementing dual edge clocking until a later standard was that a number of companies had difficulty perfecting the clock signal to permit using both the rising and the falling edges. (Prince, Tr. 9024; Kellogg, Tr. 5180; Sussman, Tr. 1371).

3. The Decision To Include Programmable CAS Latency and Burst Length.

527. At the JC-42.3 meeting of December 4-5, 1991, Howard Sussman of NEC presented the results of a separate meeting in Portland concluding that the latency of data to the clock and the burst length should be programmable. (JX0010 at 50 (“The latency of data to the clock should be programmable. Implied setup with WCBR equivalent”) (“Burst sequence...and wrap length should be programmable”)). At the same meeting, Texas Instruments made a second showing of its SDRAM proposal that also included programmable CAS latency and

programmable burst length. (JX0010 at 56 (“FEATURES TO BE PROGRAMMED IN WCBR CYCLE: . . . WRAP LENGTH . . . DATA CLOCK LATENCY)); Rhoden, Tr. 419-420). Toshiba also made a second showing that included programmable CAS latency and burst length. (JX0010 at 67; Rhoden, Tr. 424). Wrap length and burst length are the same thing. (Rhoden, Tr. 419-420; Williams, Tr. 812-813; Sussman, Tr. 1374-1375).

528. The JC-42.3 Subcommittee considered a number of alternative methods of determining the CAS latency and burst length, including using a fixed burst length, using pins to set the CAS latency and burst length, and using fuses to set CAS latency and burst length. (Rhoden, Tr. 425-434; Kellogg, Tr. 5099-5102 and 5130-5131).

529. At the December 1991 JC-42.3 meeting, Samsung presented a proposal for SDRAMs that included fixed CAS latency and burst length. Samsung proposed using a single CAS latency of 2 and a single burst length of 8. (JX0010 at 71; Rhoden, Tr. 425-28; Kellogg, Tr. 5099-5101).

530. The Samsung proposal also included a fuse option to select between two different burst options. (JX0010 at 71; Rhoden, Tr. 427-428).

531. At the December 1991 JC-42.3 meeting, Mitsubishi presented a proposal for an SDRAM that would use two pins, BT and WP, to set the burst length and burst type. (JX0010 at 74; Kellogg, Tr. 5102). In its proposal, Mitsubishi provided for two burst length options, a burst length of 4 and 8. (JX001 at 64; Rhoden, Tr. 430-34).

532. At the December 1991 JC-42.3 meeting, Texas Instruments presented a proposal using the WCBR cycle to program the mode register to determine burst length and CAS latency. (JX0010 at 50 and 56). WCBR indicates a situation where the write signal is low and a CAS signal is sent before the RAS signal. While common in a test or refresh operation, CAS before RAS differs from a normal read or write operation where the RAS would be sent before the CAS. (Kellogg, Tr. 5107-5109).

533. WCBR was a cycle that had been used in fast page mode and EDO DRAMs to reflect a means by which a test mode could be entered and remain for some period of time. (Kellogg, Tr. 5106-5107).

534. The use of WCBR to program CAS latency and burst length appealed to JEDEC members because it was a familiar concept, was evolutionary and could easily be achieved. (Kellogg, Tr. At 5109-10 (Texas Instrument’s proposal to use WCBR “had two key messages to me. One is that it indicated I could use an evolutionary concept. In other words, I could use something I was familiar with and I’d been using for some period of time. It also implied that setting modes in a programmable method could be easily achieved.”); Sussman, Tr, 1382-83 (WCBR “is the same test mode methodology, programmable, that we have had for years.”)).

535. At the JC-42.3 meeting of February 27-28, 1992 NEC, Hitachi, Fujitsu, Toshiba and Mitsubishi all made SDRAM proposals that included programmable CAS latency and burst length. (JX0012 at 39 (NEC: “FEATURE. . . Programmable wrap-length (2,4,8,16, Full Page) . . . Programmable RAS,CAS latency using WCBR+Address-key”) and JX0012 at 42 (NEC: diagram indicating mode register programmability including programmability of CAS latency and burst length); JX0012 at 69 (Hitachi: “Programmable wrap length . . . Programmable RAS, CAS latency”) (Sussman, Tr. 1382-1383); JX0012 at 76 (Fujitsu: “Features: ... Programmable burst type and wrap length (4, 8, Full Column)”); JX0012 at 91 (Fujitsu: diagram indicating mode register programmability including programmability of CAS latency and burst length); JX0012 at 94 (Toshiba: “Basic Features of Synchronous DRAM: ... 3. Sequential column access with programmable wrap length . . . 6. Programmable latency”); JX0012 at 60 (Mitsubishi: “Target Specification of Synchronous DRAM: ... 2. *Programmable Wrap length 4 & 8 bit (Selectable by Address Key)*”). At the same meeting, Sun presented comments on what features it would like to see included in SDRAMs, including programmable CAS latency and burst length. (JX0012 at 110 (“Synchronous DRAM requirements . . . WCBR programming (latency, wrap len, etc. . .”).

536. At a DRAM Task Group meeting of April 9-10, 1992, NEC, Fujitsu, Toshiba, Samsung, Hitachi, Mitsubishi and IBM presented proposals that included programmable burst length. (CX0034 at 33 (“NEC: ... programmable Wrap 1,2,4,8, full page”); CX0034 at 33 (“Fujitsu: ... programmable wrap and burst of 1, 4,8, full page length); CX0034 at 35 (“Toshiba: ... programmable Wrap and burst of 4 and 8”); CX0034 at 35 (“Samsung: ... programmable Wrap and burst of 4, 8 full page length”); CX0034 at 35 (“Hitachi: ... programmable Wrap and burst of 1,2,4,8, full page”); CX0034 at 36 (“Mitsubishi: ... programmable Wrap and burst of 4,8,16,32, full page”); CX0034 at 32 (“IBM: ... Programmable Wrap of 2,4 or 8 words”).

537. At the next meeting of JC-42.3 on May 7, 1992, the minutes of the April DRAM Task Group meeting were presented to the full JC-42.3 subcommittee. (CX0034 at 4 and 30-37).

538. At the May 1992 meeting of the JC-42.3 Subcommittee, Samsung, NEC, Toshiba, Hitachi and Mitsubishi all made SDRAM presentations that included programmable CAS latency and burst length. (CX0034 at 44 (Samsung - Mode register field table showing programmability of CAS latency and burst length); CX0034 at 63 (NEC - Mode register table showing programmability of CAS latency and burst length); CX0034 at 83 (Toshiba - “Programmable Latency Clock Times . . . CAS Latency”) and 85 (Diagram indicating mode register programmability including programmability of burst length and CAS latency); CX0034 at 99 (Hitachi - “1. Feature . . . *Programmable wrap length (1,2,4,8, Full Page). . . *Programmable RAS, CAS latency. . .”); CX0034 at 108 (Mitsubishi - Access latency table showing programmability of CAS latency and burst length); CX0034 at 140 (Fujitsu -Register programming table including programmability of CAS latency and burst length).

539. At the May 1992 JC-42.3 meeting, Cray gave a presentation that proposed the use

of fuses to choose between two different CAS latencies, 2 and 3, and two burst lengths, full page and 8, for an SDRAM part. (CX0034 at 149 (proposing feature sets, which included CAS latency and Wrap Length, for two SDRAM configurations and stating, “[d]efault [s]et fuse programmable by supplier”); Sussman, Tr. 1388; Kellogg, Tr. 5103-5105). There were no other presentations of alternatives to programmable CAS latency and burst length at this meeting. (*See generally* CX0034).

540. On June 11, 1992, four SDRAM ballots were sent out to all members. (CX0252A at 1). One ballot sought approval for use of a programmable mode register to set CAS latency and burst length. (CX0252A at 1 (“Item 376.3 “Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register” JC-42.3-92-85”); Crisp, Tr. 3075-3076; Rhoden, Tr. 448; Williams, Tr. 811-812; Sussman, Tr. 1390-1391).

541. Crisp voted (for technical reasons) against all four of the ballots, including the proposal for the mode register. (JX0013 at 9-11). The ballot required anyone aware of patents involving the ballot to alert the Subcommittee during their response. Committee Ballot, JC-42.3-92-85, item 376.3 (June 11, 1992) (Proposed Standard for 16M bit x 4 Sync DRAM Mode Register). At the time that the mode register ballot was being considered, Crisp never said anything with respect to potential Rambus patents relating to that ballot. (Crisp, Tr. 3087; Williams, Tr. 819-820).

542. The results of the vote on the mode register ballot were presented at the next JC-42.3 meeting on July 21, 1992. (JX0013 at 9-12; Sussman, Tr. 1393). The initial tally showed 14 members in support of the proposal, 5 against and 7 abstentions. (JX0013 at 10). Various Subcommittee members offered comments, especially with respect to the need for a CAS latency of 4. (JX0013 at 10-11 (“Hitachi: We don’t like latency of 4 four. NEC agreed to review its need for the CAS latency of four cycles. There was a lot of discussion about this. Some felt it should be made optional.”). Finally, it was agreed to re-ballot the mode register proposal with an optional latency mode of four. (JX0013 at 11).

543. At the September 16-17, 1992 JC-42.3 meeting Sun made an SDRAM presentation that included programmable CAS latency and burst length. (CX0042 at 39-40 (Mode register table showing programmability of CAS latency; “Programmable Options: Several programmable options are associated with read and write accesses, as specified in the Mode Register. ... Wrap Length. Wrap length specifies the length of the burst for a read or write cycle”)).

544. On January 21, 1993, the DRAM Task Group made minor technical edits to the NEC mode register that included programmable CAS latency and burst length and had previously been balloted as “Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register” JC-42.3-92-85 (item 376.3). The DRAM Task Group decided that a re-ballot was not necessary and added the ballot to the pass-hold category. (CX0047 at 3 (“This ballot had been passed but was shown as up for re-ballot. The ballot will not be reissued but will be editorially changed.”)).

4. Other Technologies Considered In Connection With JEDEC Work on the SDRAM Standard.

(A) Low Voltage Swing Signaling.

545. During 1992 Jedec work included a number of presentations that included low voltage swing signaling. At the February 27, 1992, JC 42.3 meeting, NEC, Fujitsu, Mosaid, Sun and Intel all made proposals that included low-voltage swing signaling. (JX0012 at 39, 76, 104, 111, 113; Crisp, Tr. 3045-46). At this same meeting, the JC-42.3 Committee discussed GTL technology for use with SDRAM. (JX0012 at 36, 56-58, 60, 101-02, 104, 111).

546. At the April 8, 1992, Special SDRAM Task Group meeting, the JC 42.3 Subcommittee considered SDRAM proposals that included low voltage swing signaling. (CX0034 at 32 (IBM), 33 (NEC, Fujitsu), 35 (Samsung, Hitachi), 36 (Mitsubishi).

547. At the May 7, 1992, JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included low voltage swing signaling. (CX0034 at 59 (NEC), 122-123 (Fujitsu)).

548. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included low voltage swing signaling (CX0042 at 31) ("It is proposed that LVTTTL be used for I/O drivers and receivers.")).

(B) Dual Bank Design.

549. During 1992 and 1993 Jedec work included a number of presentations that included dual bank design. At the February 1992 JC 42.3 meeting, the Subcommittee addressed the topic of multiple active subarrays in two presentations (JX0012 at 34, 37) and multibank or dual bank design in other presentations (*See, e.g., id.* at 60). The Subcommittee considered proposals for multibank, or dual bank, design from NEC, Mitsubishi, Fujitsu, and Sun. (JX0012 at 39, 60, 76, 110).

550. At the May 7, 1992, JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included dual bank design. (CX0034 at 59 (NEC), 122-123 (Fujitsu)). During that meeting, Mr. Kelley of IBM, prompted by Mr. Meyer of Siemens, asked Mr. Crisp whether Rambus might have patent claims that related to dual bank design. (CX2089 at 130, 131, 136-137 (Meyer, Infineon Trial Tr.). Mr. Crisp gave no verbal response, but rather shook his head. Mr. Kelley then commented to the group that "they don't have anything to say about that." (*Id.*).

551. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included a dual bank design (CX0042 at 30) ("The 4M x 4 device is organized internally as two banks.")).

(C) Auto-Precharge.

552. At a number of meetings during the course of 1992, the JC-42.3 Subcommittee discussed using the auto-precharge technology in the SDRAM standard. (February 1992: JX0012 at 37, 39 (NEC), 76 (Fujitsu), 94 (Toshiba), 108 (Sun); April 1992: CX0034 at 32 (IBM), 33 (NEC), 35 (Hitachi); May 1992: CX0034 at 6, 150).

553. At the September 16-17, 1992, JC-42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included an "autoprecharge" option CX0042 at 45). Auto-precharge was incorporated as a feature in the JEDEC SDRAM 21-C standard, issued in November 1993. (JX0056 at 115).

(D) Source Synchronous Clocking.

554. At the April 1992 JC-42.3 Special Task Group meeting, the DRAM Task Group discussed the issue of source synchronous clocking. CX1708 at 2 ("Hitachi brought up the issue of source synchronous clocking."); Crisp, Tr. 3053-54 (recalling that a discussion on source synchronous clocking had taken place at this meeting)).

(E) Externally Supplied Reference Voltage.

555. At the February 27, 1992, JC 42.3 meeting, Samsung proposed an externally supplied reference voltage. (JX0012 at 58; Crisp, Tr. 3043, acknowledging that "vref" refers to externally supplied reference voltage).

556. At the May 1994 JC-42.3 Subcommittee meeting, Mr. Crisp observed various presentations regarding specific SDRAM configurations. Mr. Crisp wrote in an e-mail to Mark Johnson, an attorney for Rambus, "Note that many of the SDRAMs use an externally supplied reference voltage in the input buffers. I believe we have a claim we added to cover this configuration. We should make note of this." (CX0711 at 26, 27). Later in the same May 1994 meeting, Mr. Crisp noted, "(again we need to check claims about 'DRAM with input receivers using an externally supplied reference voltage'). We may be able to slow down or stop (or at least collect from) all of the CTT, GTL and HSTL devices if this claim is allowed (Allen, I believe this was one of the claims you, Lester, Tracy and I wrote up in late '91, right?)." (CX0711 at 26, 31).

557. On March 14, 1995, Fujitsu gave a presentation on "STBUS" signaling technology to the JC-16 Subcommittee. (CX0711 at 53, 54; *see also* CX0082 at 13). In an e-mail to Rambus executives and others, Mr. Crisp stated that Rambus had claims that anticipated Fujitsu's STBUS proposal because it was a proposal for a current source device that relied on an externally supplied reference voltage. (CX0711 at 53, 54 ("Taken along with the fact that they rely on an externally bussed reference (this should be anticipated by some of our claims), I would

say that this proposal may well infringe our work.”)).

5. Adoption of the SDRAM Standard.

558. At the JC-42.3 meeting on March 3-4, 1993, the subcommittee voted unanimously to send 14 SDRAM ballots to Council to become approved as a comprehensive standard for SDRAMs intended for publication as Release 4 of the 21-C standard. JX0015 at 14 (“VLSI moved to send all pass/hold ballots on to Council. Seconded by TI. The vote was: 26 yes, 0 no. Motion passed.”). The ballots were in fact sent to Council after the vote. (G. Kelley, Tr. 2554-2555; JX0016 at 5).

559. The subcommittee agreed to issue a press release stating that the Sync DRAM standard has been approved by subcommittee. (JX0015 at 14; G. Kelley, Tr. 2555). A copy of the release was attached to the minutes of the March meeting. (JX0015 at 99) (“Press Release ... At the March 4 meeting here the EIA/ JEDEC JC-42.3 Subcommittee on Memory unanimously approved 14 Synchronous DRAM ballots. These will be submitted to the JEDEC Council for their approval before publishing as a JEDEC standard. ... the following list of ballots [are included] ... 4 16M/18M SDRAM Mode Register Bit Definitions.”). Among the features included in this standard was programmable CAS latency and burst length. (JX0056 at 114).

560. At the JC-42.3 meeting on May 19-20, 1993, Gordon Kelley of IBM reported to the full JC-42.3 subcommittee that the SDRAM ballots had gone to Council and that all council members apart from AT&T had supported the ballots. He attached to the minutes a letter responding to ATT’s concern by proposing additions to the Mode Register. (JX0016 at 5 and 36-37(IBM) (table showing programmability of mode register including programmable CAS latency and burst length). Kelley also distributed copies of the ballots to the subcommittee. (JX0016 at 5; G. Kelley, Tr. 2557-2558).

561. On May 24, 1993 the JEDEC Council formally approved adoption of the comprehensive standard in Release 4 of the 21-C standard. (CX0054 at 8-10; G. Kelley, Tr. 2559-2560).

562. In November, 1993 JEDEC published the SDRAM standard as JEDEC Standard No. 21-C Release 4 (JX0056; Williams, Tr. 801). The standard included a programmable mode register that includes programmable CAS latency and burst length. (JX0056 at 114 (mode register table showing programmability of three elements, including latency mode and burst length); Rhoden, Tr. 456-458; Williams, Tr. 801-03; Sussman, Tr. 1399-1400).

563. For a manufacturer to produce JEDEC-compliant SDRAMs, the standard requires the manufacturer to design and produce SDRAMs with programmable CAS latency and burst length on a mode register. (Sussman, Tr. 1399-1401; see CCFF 25-28 and 114-116 discussing need for compatibility and interoperability).

564. The SDRAM and DDR SDRAM standards include low swing signaling (CX0234 at 116, 189-195), dual bank (CX0234 at 116, 145), source synchronous clocking (CX0234 at 164; Lee, Tr. 6682) and auto-precharge (CX0234 at 145, 151) features, and allows optional use of an externally supplied reference voltage (CX0234 at 84 (pin 40), 85 (pin 40), 86 (pin 49) and 87 (pin 49)).

6. Subsequent JEDEC Work Relating to the SDRAM Standard.

565. Work continued in the JC-42.3 subcommittee after the publication of the SDRAM standard in November, 1993. That work included improvements to the SDRAM standard and work on future generation of devices. (Rhoden, Tr. 460 (“Q. Now, what standard-setting work, if any, did the JC-42.3 subcommittee do between May of 1993 and June of 1996? A. Oh, a tremendous amount. The work -- inside JEDEC, there is a continuous time line of activity. Work -- it's -- while there are snapshots and we do collect groups of ballots at times, the work is continuous. We're always working on the improvements to what we have, improvements to what we've seen before and future generation of devices. So, that's three things we're always working on.”).

566. SDRAMs were not immediately adopted by the marketplace and as late as 1995 asynchronous DRAMs continued to make up approximately 97% of the market with Fast Page Mode approximating 87.2% and EDO's 9.9% of the market. (Rapp, Tr. 10248).

567. JEDEC members noted that SDRAMs were not being produced due to their overhead and yield issues. (JX0027 at 12 (“NEC noted that the amount of overhead for the JEDEC SDRAM made it unusable so it was not produced. Yield was the major issue also. Presently SDRAMs are being made, but a clear market is not there yet.”) and 13 (“It was noted that as compared to EDO, SDRAM is harder to make and the yields are lower.”).

568. JC-42.3 members showed a continued interest in asynchronous DRAMs and at the January 5, 1995 JC-42.3 meeting, Micron made a presentation of an asynchronous DRAM called Burst EDO that was based upon a page mode DRAM. (JX0023 at 69-79; Williams, Tr. 821 and 825-826).

569. Brett Williams of Micron testified that Burst EDO lost support, however, and was abandoned due to momentum behind SDRAM. (Williams, Tr. 829). He further testified that if Burst EDO had been adopted more work would have been done on it to improve its performance. (Williams, Tr. 829-830; see Jacob, Tr. 5395-5396 (discussing advantages of continuing to develop asynchronous over synchronous memory.).

570. Other JEDEC members made proposals aimed at reducing the costs of SDRAMs. At the March 15, 1995, JC-42.3 meeting, TI proposed reducing test cost by making CAS latency of 1 optional. The proposal included a mode register with programmable CAS latency and burst

length. (JX0025 at 107 (Mode register table showing programmability of CAS latency and burst length)).

571. At the May 24, 1995, JC-42.3 meeting, TI made a second showing of its proposal to make CAS latency of 1 optional. (JX0026 at 9). The proposal continued to include a mode register with programmable CAS latency and burst length. (JX0026 at 62 (SDRAM mode register table showing programmable CAS latency and burst length)). A motion to ballot the TI proposal was unanimously accepted. (JX0026 at 9). Crisp sent an e-mail from the meeting stating that “TI would prefer to eliminate the requirement for supporting CAS latency = 1 to reduce cost of speed testing by removing some testing permutations.” (CX0711 at 70).

572. At the September 11, 1995, JC-42.3 meeting, NEC made an SDRAM Lite presentation that proposed an SDRAM with a reduced feature set aimed at saving costs. (Rhoden, Tr. 475-6; Lee, Tr. 6625-27). That proposal suggested using a fixed CAS latency of 3 and a single fixed burst length. (JX0027 at 13, 66; Lee, Tr. 6626, 6629-30, 6632, 11,017; Sussman, Tr. 1416-17).

573. There was initial support for SDRAM Lite at the meeting with 23 members voting that an SDRAM Lite standard was needed and 4 voting against. (JX0027 at 12). It was agreed at the meeting that Desi Rhoden would prepare a survey ballot that JEDEC would issue. (JX0027 at 14).

574. At the JC-42.3 meeting on December 6, 1995, SDRAM Lite was further discussed. (JX0028 at 6; CX0711 at 191-92 (Crisp e-mail (12/6/95))).

575. On January 31, 1996, there was an interim meeting of JC-42.3 where results of the SDRAM Lite survey ballot were discussed. Included in the discussion was having fixed CAS latency and burst length. (JX0029 at 13, 14 (“Survey Ballot Results . . . Does your company want to include CAS latency of 2 in the reduced specification? . . . Does your company want to include Burst Length of 1 in the reduced specification? . . .”); Lee, Tr. 6630, 6632, 11018-11019). The survey ballot also asked members if they wanted to include auto-precharge in the reduced specification. (JX0029 at 15).

576. According to Terry Lee of Micron, the SDRAM Lite proposal lost support and was abandoned because it was recognized that the cost adder in the full SDRAM technology was not as great as initially thought and because members were frustrated at the length of time it was taking to get a standard. (Lee, Tr. 6634-6635).

577. SDRAMs began selling in volume in 1997, accounting for 33.5% of the DRAMs sold, and became the dominant product in the market in 1998, accounting for 60.8% of DRAMs sold. By that stage full page mode DRAMs had declined to 8.8% and EDO to 27.6% of DRAMs sold. (Rapp, Tr. 10248-10249).

B. The Next Generation SDRAM (DDR SDRAM).

1. The Beginnings of Work on the Standard.

578. JEDEC work on the next generation SDRAM that would eventually be named DDR SDRAM began with consideration of IBM's HST proposals in the late 1980's and early 1990's. (G. Kelley, Tr. 2584-2585 (“Q. Mr. Kelley, based on your recollection and your participation within JEDEC, what is your understanding of when JEDEC began work on the standard that became the JEDEC DDR SDRAM standard? A. In my mind, the consideration of using a double-edged clock actually began when I made the first presentation in 1988 and IBM reproposed in 1990 and 1991 and several other companies picked up in that -- on that concept in 1991. I think we had five companies showing what they called their own toggle mode in their presentations on the consideration of the first-generation synchronous DRAM. So in my mind, the consideration of the dual-edge clock began in 1988 and was essentially tabled because it was felt by the committee that it was not needed for the first generation part and that we would pick up the idea for consideration of the second generation part, which is now called DDR SDRAM.”); Sussman, Tr. 1427- 1428).

579. After the publication of the first generation SDRAM standard in November 1993, JEDEC worked both on implementations of and improvements on the SDRAM standard, including pin-out diagrams for specific SDRAM configurations, and on the standard for the next generation SDRAM. (Rhoden, Tr. 460-61 (“Q: Now, what standard-setting work, if any, did the JC-42.3 subcommittee do between May of 1993 and June of 1996? A: Oh, a tremendous amount. . . . We're always working on the improvements to what we have, improvements to what we've seen before and future generation of devices. . . . Q: Now, with respect to the SDRAM standard, what would future generation devices refer to? A: Well, we call[ed] them future generation DRAM –SDRAM Sometimes it was referred to as SDRAM II, sometimes it was just future DRAM. . . . Q: What standard did [that work] lead to? A: Well, the next generation standard would have been the DDR standard that actually came out later.”); G. Kelley, Tr. 2566-67 (“Q: . . . After adoption of the series of SDRAM ballots, what did the JC-42.3 subcommittee do next? A: I believe that the next item that we pursued was the next generation of synchronous DRAM. Q: What do you mean by ‘the next generation of synchronous DRAM? A: The one that we had just approved was the first synchronous DRAM in our JEDEC standards and we had already discussed at the early discussion of the synchronous DRAM that we would probably need to take some of the ideas of that first discussion and generate a second generation. We were now beginning that process.”); Sussman, Tr. 1402 (“Q: . . . What did the JC-42.3 committee do next [after it completed work on the SDRAM standard]? A: Start on the next evolutionary part.”); Williams, Tr. 820 (“Q: . . . after JEDEC published [the SDRAM standard], what work did it move on to next? A: It took up several different options, mainly looking at the next standard, the next generation of memory.”); *see also* CX0700 at 2 (Crisp e-mail from the May 19-20, 1993 JC-42.3 meeting: “Apple . . . is saying that the committee is rushing ahead to get a next generation standard before finding out the problems with the first generation

standard.”); CX0711 at 52, 54 (Crisp e-mail of March 1995 quoting Hans Wiggers as saying that JEDEC had been working for over two years to standardize a high-speed interface and has not yet reached consensus); MacWilliams, Tr. 4815 (“ . . . we first heard about DDR in '95 when we went out to ask for options, which was one of the options we considered, the higher-speed SDRAM. One of the options was DDR.”)).

580. Work on what became the DDR SDRAM standard was referred to as “next generation SDRAM,” “SDRAM II” or “future SDRAM.” The standard was later named DDR SDRAM after Fujitsu coined the term “DDR” in December 1996. (Rhoden, Tr. 408-09 (“ . . . what DDR was originally called by a lot of people that worked on it, we called it SDRAM II, and it wasn't until Fujitsu actually coined the term DDR that we came up with a different name, called it DDR as opposed to SDR II or something like that.”); Kelley, Tr. 2581 (“Q: What was your understanding of what Samsung Electronics meant by ‘future SDRAM’ [in a JEDEC presentation made in March 1996]? A: The committee always needs to be looking ahead to determine what they want for the generation of DRAM that they’re presently working on, which at this time I believed was the one we called DDR SDRAM . . .”); (Lee, Tr. 6636 (“This is a JEDEC survey ballot for future synchronous DRAM features, which later became known as DDR”)).

581. The work begun by JEDEC after adoption of the SDRAM standard included revisiting the dual edge clock that had been proposed by IBM as part of its HST presentations in the late 1980's and early 1990's. (Rhoden, Tr. 462-463, Sussman, Tr. 1403; G. Kelley, Tr. 2567 (“Well, clearly one of the ideas was the dual-edged clock control of the output that we had earlier called toggle mode and now was called dual-edge clock and became what we called DDR or double data rate.”).

582. The work begun by JEDEC after adoption of the SDRAM standard included discussion on adding on-chip PLLs. (Rhoden, Tr. 463; Sussman, Tr. 1403).

583. The various features that members had been talking about were gathered together in a presentation given by Fujitsu at JEDEC in December 1996. This was when the term DDR was first used. (Rhoden, Tr. 1197-1198 (“This was the Fujitsu presentation where they had taken a collection of the discussions that had taken place throughout -- in -- within previous meetings for the past decade or so, and they had pulled them together in a unified approach to the next generation part. Rather than talking about these features independently, they actually pulled them together, and that is a presentation from Fujitsu. They also happened to coin the name DDR. That's the first time that the DDR name shows up, is in the Fujitsu presentation.”)).

584. The first use of the term "DDR SDRAM" in late 1996 did not mark the beginning of the work on what became the DDR SDRAM. (G. Kelley, Tr. 2582 and 2585-86 (“Q: Mr. Kelley, would you agree that the first use of the term ‘DDR SDRAM’ in late 1996 marked the beginning of the work on what became the DDR SDRAM standard? A: Not in my mind.”); Rhoden, Tr.

408-09 and 1200; Sussman, Tr. 1429 (“Q. In the 1994 to 1996 time frame, you were attending the JEDEC meetings obviously. A. Yes, sir. Q. In that time frame, was there ongoing JEDEC work that led to the DDR standard? A. Yes.”); Lee, Tr. 6636).

585. The JEDEC patent disclosure policy and obligation of good faith applied to work relating to technologies incorporated in what ultimately became known as the DDR SDRAM standard before the name “DDR SDRAM” was first used in December 1996. (G. Kelley, Tr. 2586-87 (“QUESTION: Mr. Kelley, based on your understanding of the JEDEC disclosure policy, was a member's duty to disclose patents and patent applications relating to dual-edge clock technology triggered only by presentations occurring during or after December 1996? THE WITNESS: No. In my mind, we had been considered -- considering toggle mode, which is a dual-edge clock, in the early considerations of SDRAM in the 1990, 1991, 1992 time frame significantly. There were lots of presentations that included consideration in those early '90 years, so it did not begin with the later consideration of what the committee called DDR.”); Rhoden, Tr. 468, 492, 514; Sussman, Tr. 1381-1382, 1386, 1406-1407, 1409; G. Kelley, Tr. 2571; Landgraf, Tr. 1717, 1720; *see also* J. Kelly, Tr. 1983-1984 (For the duty to disclose to arise, it is not necessary that there be some formal activity within the relevant standard-setting committee that involves the technology or technologies covered by the patent or patent application) and 1984-1985 (The duty to disclose is “not tied to any procedural formality in the process at all.”)).

2. The Decision to Use Programmable CAS Latency and Burst Length.

586. Because the next generation SDRAM standard was designed as a follow-on to the first SDRAM standard, the JC-42.3 subcommittee’s assumption was that the features contained in the SDRAM standard would be carried over into the future, or next generation, SDRAM standard. (Peisl, Tr. 4378- 4379)

587. When it began work on the next generation SDRAM standard, the JC-42.3 subcommittee assumed that programmable CAS latency and programmable burst length would be carried over into the next generation standard. (Rhoden, Tr. 491).

588. In October 1995, JEDEC staff distributed to subcommittee members, including Rambus, a survey ballot requested at the September 1995 JC-42.3 meeting. (CX0260). The subject of the survey was “Future Synchronous DRAM (SDRAM) Features.” (CX0260 at 1). The survey ballot assumed that the future SDRAM standard would include programmable CAS latency and burst length. The ballot asked whether members thought it important to add any additional latency values to those already available. (CX0260 at 9 (“There are currently 4 reserved states in the mode register’s CAS latency field that could logically accommodate CAS latencies of 5, 6, 7, and 8. . . Does your company believe it is important to standardize CAS latencies beyond a CAS latency of 4?”)). The survey ballot also asked members whether they wanted the “wrap” functionality to be programmable. (CX0260 at 11 (“There may be advantages

to eliminating the “wrap” functionality or making it programmable.”)).

589. The results of the SDRAM Features Survey Ballot that had issued on October 30, 1995 were tallied at the same meeting on December 6, 1995. (JX0028 at 36-48). Mosaid made a presentation on the results of the survey. (JX0028 at 6). The CAS latency portion of the survey results showed that JC-42.3 members strongly supported adding into the mode register CAS latencies in excess of four. (JX0028 at 42). The results of the burst wrap survey were also presented. (JX0028 at 44).

590. At the March 20, 1996, JC-42.3 meeting, the RAM features and functions subcommittee made a presentation that included use of programmable CAS latency and burst length. (JX0031 at 64). Desi Rhoden, who made the presentation, assumed that JEDEC would continue to use programmable CAS latency and burst length in the next standard. (Rhoden, Tr. 491-492).

591. At the June 5, 1996, JC-42.3 meeting, EIA made two presentations that included programmable CAS latency and burst length. (JX0033 at 41- 46 and JX0033 at 47-49).

592. At the September 10, 1997 JC-42.3 meeting, the subcommittee voted unanimously to send a DDR mode register to Council. (JX0040 at 7-8; Lee, Tr. 6640-6641). That mode register included programmable CAS latency (CX0234 at 150; JX0057 at 12; Lee, Tr. 6641) and burst length (CX0234 at 150; JX0057 at 12).

593. The mode register was approved by Council and included in Release 9 of the 21-C standard published by JEDEC in August 1999 and subsequently in the consolidated DDR SDRAM Specification (JESD79) that was published by JEDEC in June 2000. (CCFF 657).

3. Consideration of On-Chip PLL/DLL.

594. After the release of the SDRAM standard, JEDEC began working on the next “evolutionary part”. (Sussman, Tr. 1402). JEDEC was considering on-chip PLL/DLLs as part of that work. (Sussman, Tr. 1403).

595. PLLs are very similar to DLLs. (Jacob, Tr. 5443).

596. Rambus co-founder Horowitz testified that a DLL is a type of PLL. (Horowitz, Tr. 8607).

597. The JEDEC subcommittee members used the terms PLL and DLL interchangeably. (Rhoden, Tr. 492).

598. The predominant purpose of JEDEC considering placing a PLL or a DLL on a

memory device was to guarantee that the memory controller would capture data during the data valid window. (Jacob, Tr. 5442-5443; Kellogg, Tr. 5154-5155; Lee, Tr. 6662-6664)

599. An on-chip PLL/DLL would account for delays occurring within the DRAM itself but would not account for delays that occur between the DRAM chip and the controller. (Kellogg, Tr. 5154).

600. The duty to disclose patents or patent applications relating to use of on-chip PLL or on-chip DLL technology was triggered while Rambus was still a member of JEDEC. (G. Kelley, Tr. 2587 (“Q. Again, Mr. Kelley, based on your understanding of the JEDEC disclosure policy, was a member's duty to disclose patents and patent applications relating to use of on-chip PLL or on-chip DLL technology triggered only by presentations occurring during or after December 1996? A. No. They had to be disclosed when the presentations were first considered in the '95, possibly even '94 time frame. I specifically remember '95.”)).

601. During the course of 1994, Richard Crisp of Rambus observed discussions in the JEDEC JC-42.5 subcommittee regarding using PLLs on memory modules to remove clock skew from the module. (CX0711 at 13, 14 (Crisp e-mail (3/8/94): the 200 pin DIMM (Dual In-line Memory Module) includes “an on-board PLL clock generator to remove clock skew from the module.”), at 31, 35 (Crisp e-mail (7/13/94): Mark Kellogg “argues that the PLLs, buffers, etc must be moved off the DIMM. They are still needed, but the idea is to put them on the motherboard.”)).

602. During the course of 1994, Richard Crisp of Rambus was present when the JC-42.3 subcommittee discussed putting PLLs on other types of memories, including SDRAMs. (JX0021 at 39 (Motorola SRAM Sleep and Doze Mode Proposal diagram shows “Phase Locks”); JX0022 at 34 (NEC SRAM Sleep and Doze Mode (informal) proposal table showing PLL)).

603. Richard Crisp and others at Rambus appreciated that memory manufacturers could incorporate PLLs/DLLs on SDRAMs to correct for clock skew. (CX0711 at 22, 23 (Crisp e-mail (5/24/94): “The use of DLL/PLL technologies could be incorporated by anyone to solve” one aspect of clock skew)).

604. At the September 13-14, 1994, JC-42.3 meeting, NEC made a presentation regarding PLLs on SDRAMs. NEC’s presentation showed an on-chip PLL circuit and proposed to include a PLL-enable bit in the mode register in order to enable on-chip PLLs. (JX0021 at 87 (Mode Register diagram showing PLL Enable Mode), 91 (diagram comparing access time with and without on-chip PLL) and 92 (slide discusses advantages and disadvantages of on-chip PLL); Rhoden, Tr. 466 (“NEC was proposing including a PLL on board the chip to actually synchronize the phased relationship of the internal clock to the external clock.”); G. Kelley, Tr. 2569-70 (The “PLL enable mode is for the addition of a feature called phase lock loop. . . . The proposal on the left [of JX0021, page 91] asks us to consider not putting the PLL on chip, in other words,

doing the phase lock loop operation with another device. And then the proposal on the right as a comparison shows us the option of putting the phase lock loop on the DRAM chip as a new feature. And the comparison shows why the inclusion of the phase lock loop on the chip buys performance.”);

605. Richard Crisp sent an e-mail from the September 1994 JC-42.3 meeting stating that NEC was proposing putting a PLL on an SDRAM. (CX0711 at 36-37 (“(NEC PROPOSES PLL ON SDRAM!!!) . . .**** They plan on putting a PLL on board their SDRAMs . . . ****I believe that we have now seen that others are seriously planning inclusion of PLLs on board SDRAMs. . . . What is the exact status of the patent with the PLL claim? ****”) (emphasis in original)).

606. Members viewing this presentation were under an obligation to disclose patents or patent applications relating to use of on-chip PLL technology. (G. Kelley, Tr. 2571; *see also* Rhoden, Tr. 468 (this presentation triggered a disclosure obligation)) Furthermore, members had an expectation that a member with any intellectual property relating to on-chip PLL should disclose that interest at the meeting. (Sussman, Tr. 1406-1407).

607. In terms of implementation, there was essentially no difference in the PLL proposed by NEC in September 1994 and a DLL. (Rhoden, Tr. 467-468).

608. At the May 24, 1995 JC-42.3 meeting, Hyundai, Texas Instruments and Mitsubishi made a presentation of the proposed Ramlink/Synclink standard at JEDEC. (JX0026 at 10-11). That presentation included discussion of on-chip PLLs, which the RamLink/SyncLink was planning to avoid. (JX0026 at 97 (“Avoid using PLL in DRAM components”)).

609. Discussions of features for the future SDRAM standard led to a request at the JC-42.3 meeting held on September 11, 1995 for a survey ballot to determine the features for the next-generation DRAM. On-chip PLLs were one of the features that had been discussed that led to the request for the survey ballot. (JX0027 at 14 (“A survey ballot was requested on the next generation issues stated above. Mr. Allen agreed to prepare the survey.”); Calvin, Tr. 1032 (“ . . . this survey was a result of trying to capture the top most things that were necessary for SDRAM to continue to evolve. This had been discussed at numerous meetings before, and many inputs were coming in and, well, this seems to be a big problem area, we should do this. And PLL/DLL was one of those discussions. So, this was just an attempt to say, how important is it, how would you rate it, in terms of need.”)).

610. In October 1995, JEDEC staff distributed to subcommittee members, including Rambus, the survey ballot requested at the September 1995 JC-42.3 meeting. (CX0260). The subject of the survey was “Future Synchronous DRAM (SDRAM) Features.” (CX0260 at 1). Question 3.9-1 asked members whether they believed that use of an on chip PLL or DLL was important to reduce the access time from the clock for future generations of SDRAMs future generations of DRAMs (CX0260 at 12 (“Does your company believe that on chip PLL or DLL is

important to reduce the access time from the clock for future generations of SDRAMs?”).

611. At the JC-42.3 meeting of December 6, 1995, the tally of the votes cast in the Future SDRAM Features Survey Ballot was announced. Eleven members voted “yes” and four members “no” to the question as to whether their company believed that “on chip PLL or DLL is important to reduce the access time from the clock for future generations of SDRAMs” (JX0028 at 45). On-chip PLL/DLL was included among issues with “strong support” in the conclusion of the SDRAM Feature Survey Ballot. (JX0028 at 35 (“ISSUES WITH STRONG SUPPORT . . . On chip PLL/DLLs to reduce clock access time”)).

612. Mosaid presented the results of the survey. Mosaid disclosed a pending patent application with claims relating to on-chip DLL technology, but stated that the patent likely to result from the application may not be necessary to use a standard. (JX0028 at 6 (“MOSAID noted that they had a patent pending on DLL and noted that it was a particular implementation and may not be required to use the standard.”); CX0711 at 192 (Crisp e-mail (12/6/95): Richard Foss of Mosaid “stated that MOSAID has a pending patent application for PLL/DLL on SDRAMs. His suspicion is that his patent will probably end up being an implementation patent rather than a concept patent. In the event the patent winds up being a concept patent, he says they will be compliance with the JEDEC patent policy.*****”)).

613. At the January 31, 1996, JC-42.3 interim meeting, Micron presented a proposal discussing the potential use of on-chip PLL/DLLs and echo clocks in Future SDRAMs. (JX0029 at 17 (“PLL/DLL circuits are being considered to reduce the apparent access time (i.e. as measured from the external clock) for read accesses”). Micron proposed using a single PLL on the controller or clock chip and echo clocks rather than on-chip PLLs. (JX0029 at 18 (“FUTURE SDRAM - CLOCK ISSUES PLL/DLL Circuits . . . Use centralized PLL/DLL (e.g. in clock chip) to generate two phases of clock signal”); Rhoden, Tr. 487). The Micron presentation triggered a duty to disclose under the JEDEC patent policy. (Rhoden, Tr. 488).

614. At the JC-42.3 meeting of March 20, 1996, Desi Rhoden, on behalf of the JC-42.3C RAM Features and Functions Letter Committee, made a presentation that included on-chip PLL/DLL. (JX0031 at 64 (table showing SDRAM features that includes on chip PLL/DLL); Rhoden, Tr. 492). This presentation triggered a disclosure under the JEDEC patent policy. (Rhoden, Tr. 493).

615. Samsung also made a Future SDRAM proposal that included discussion of alternatives to on-chip PLL/DLL. (JX0031 at 68-72; Rhoden, Tr. 513-514; Lee, Tr. 6691). This presentation triggered disclosure under the JEDEC patent policy. (Rhoden, Tr. 514).

616. At the JC-42.3 meeting of June 5, 1996, EIA made two presentations involving on/off-chip DLL. (JX0033 at 42 (“Latency, in the case of DLL on chip”) and 48 (“Latency (without DLL)”)).

617. During the course of its work relating to what ultimately became the DDR SDRAM standard, the JC-42.3 subcommittee also considered, as an alternative to on-chip PLL/DLL, the use of vernier circuits. (JX0036 at 58, 64; CX0367 at 3 (Presentation of Desi Rhoden: “The inclusion of the vernier in the memory for read data timing manipulation is good for all but the simple one memory device system.”); Kellogg, Tr. 5168 (“My recommendation was in support first of all for the vernier. We seriously felt that that was the optimal solution, looking at the total data capture issue.”); *see also* Lee, Tr. 6676-6678).

618. During the course of its work relating to what ultimately became the DDR SDRAM standard, the JC-42.3 subcommittee also considered, as an alternative to on-chip PLL/DLL, the use of an edge-aligned, bi-directional data strobe. (CX0368 at 1, 4 (Micron presentation regarding an edge-aligned, bi-directional data strobe: An edge-aligned strobe allowed implementation without DLL); CX0370 at 2 (Silicon Graphics presentation for a unidirectional data strobe for read operations; “DLLs introduce instability, cut into dram core cycle time.”) and 3; CX2713 at 2; Lee, Tr. 6651, 6654).

619. By the time of the JC-42.3 meeting of December 9-10, 1997, the subcommittee had decided to include an on-chip DLL in the DDR standard that could be turned on or off (Lee, Tr. 6680-6681). At this meeting the subcommittee discussed the timing of a device where the on-chip DLL was disabled or enabled. (JX0041 at 18; Lee, Tr. 6680-6681).

4. Consideration of Dual Edge Clocking.

620. Dual edge clocking means capturing data off both edges of the clock. (Lee, Tr. 6688).

621. In a DDR SDRAM, data transitions on both the rising and falling edge of the clock. (Rhoden, Tr. 389; Polzin, Tr. 3995 (“DDR techniques allowed you to capture the data on the falling edge and the rising edge to effectively double the data rate, hence the word “double data rate” or “DDR.”); Peisl, Tr. 4397 (“Both, the rising and falling edge of the clock. That’s the essential of the DDR standard.”)).

622. In a DDR SDRAM read operation, data is driven by a data strobe, or strobe clock, which transmits data in time with the rising and falling edges of the system clock. (Rhoden, Tr. 513 (Samsung was proposing a “strobe clock, which is essentially what we have [in DDR SDRAMs].”); Peisl, Tr. 4397 (data is being transmitted on the rising and falling edges of the clock); Sussman, Tr. 1427 (page 5 of the DDR SDRAM standard refers to two data transfers per clock cycle); Kellogg, Tr. 5172 (the DDR SDRAM standard called for transmission of data on both the rising and falling edges of the clock)).

623. JEDEC consideration of the dual edge clocking technology that was included in the DDR SDRAM standard began in 1988 when IBM presented its first HST proposals. (G. Kelley,

Tr. 2584-85 (“In my mind, the consideration of using a double-edged clock actually began when I made the first presentation in 1988 and IBM repropoed in 1990 and 1991 and several other companies picked up in that -- on that concept in 1991. I think we had five companies showing what they called their own toggle mode in their presentations on the consideration of the first-generation synchronous DRAM. So in my mind, the consideration of the dual-edge clock began in 1988 and was essentially tabled because it was felt by the committee that it was not needed for the first generation part and that we would pick up the idea for consideration of the second generation part, which is now called DDR SDRAM.”) and 2586-87 (“In my mind, we had been considered -- considering toggle mode, which is a dual-edge clock, in the early considerations of SDRAM in the 1990, 1991, 1992 time frame significantly. There were lots of presentations that included consideration in those early '90 years, so it did not begin with the later consideration of what the committee called DDR.”)

624. Dual edge clocking continued to be considered at JEDEC as IBM and other members made further HST proposals in 1990 and 1991. (G. Kelley, Tr. 2584-85; CCFF 511)

625. On January 3, 1991, the JC-42.3 subcommittee issued a survey ballot regarding a proposed standard for HST. (CX0251). It included questions on dual edge clocking. (CX0316 at 1 (“TOGGLE MODE offers increased data rate (Writes or Reads) by clocking data from all of the DRAM I/Os at both the falling and the rising edges of the ‘Toggle’ pin . . . Do you think that this kind of performance enhancement needs to be offered as a standard” yes (hand written).”).

626. At the May 9, 1991 JC-42.3 meeting, the subcommittee passed a motion to ballot the IBM toggle mode presentation. (JX0005 at 12). At the same meeting Siemens also made a toggle mode presentation that was like the IBM toggle mode except it used a G\ pin instead of a new toggle pin. (JX0005 at 12).

627. At the September 18, 1991 JC-42.3 meeting, the subcommittee voted in favor of the IBM toggle mode technology. However, there were four no votes and a number of comments. For example, NEC and Samsung commented that the use of two clock edges can limit speed. (JX0007 at 8). The subcommittee therefore decided to put the ballot on hold until more resolution to the comments could be made. (JX0007 at 9). At the same meeting Siemens made a second showing of its toggle mode technology. A motion to ballot was not made. (JX0007 at 10).

628. At the JC-42.3 Subcommittee meeting held on December 4-5, 1991, Mark Kellogg of IBM made a presentation comparing High Speed Toggle to synchronous DRAMs. (JX0010 at 5 and 84 (“Options: 1) high speed toggle (already passed ballot, on hold”)).(Kellogg, Tr. 5172-5173) The HST being presented by Kellogg was basically the same thing as dual edge clocking. (Sussman, Tr. 1380-1381; Prince, Tr. 8992 (“Q. And when you talk here about another method, was that -- are you describing dual-edged clocking? A. Yes, although at the time I would have said I was describing toggle mode. Yes. Q. And by that would mean using the rising edge and

the falling edge of the clock to – A. Yes, sir.”) The Kellogg presentation created an obligation on a member to disclose relevant patents or patent applications. (G. Kelley, Tr. 2506). A JEDEC member listening to this presentation with claims covering dual edge clocking should have disclosed those claims. (Sussman, Tr. 1381-82).

629. At a special meeting of the JC-42.3 Subcommittee Task Force held on April 14, 1992, IBM indicated a desire to have dual edge clock technology in the first-generation SDRAM standard. (CX0034 at 32 (“IBM: ... A Synchronous RAS/CAS with Synchronous DQ * dual clock edge...”); Rhoden, Tr. 443 (Mr. Hardell was “proposing using both edges of the clock for the transition of data and information inside the Synchronous DRAM.”); G. Kelley, Tr. 2514 (Mr. Hardell was proposing that JEDEC use the IBM invention, “an asynchronous DRAM with a synchronous output using both edges of the clock, the rising edge of the clock and falling edge of the clock, to output data.”); Sussman, Tr.1386 (“Hardell . . . is still pushing a double edge clock version of the part).

630. Mr. Sussman’s expectation as a JEDEC member was that a member with intellectual property relating to dual edge clocking technology would disclose that intellectual property. (Sussman, Tr. 1386). The same JEDEC disclosure rules apply to JEDEC task force meetings like this one as to regular JEDEC committee meetings. (Sussman, Tr. 1386)

631. The attendees at the meeting discussed the advantages of a dual edged clock against a single edged clock and decided that a dual edge clock was not needed to meet the requirements of the SDRAM standard that it was currently working on and that it would reconsider the dual edge clocking technology in the next generation standard (G. Kelley, Tr. 2515 (“At the meeting, we discussed the advantages of a double-edged clock versus a single-edged clock and we decided as a group that we could meet the requirements of the high-performance systems for the next-generation DRAM without needing a double-edged clock for that doubling of the performance and that we would reconsider the double-edged feature in the next generation.”); Rhoden, Tr. 462).

632. The proposal made by IBM at the April 14, 1992 Task Force meeting eventually wound up in the DDR standard. (Rhoden, Tr. 445-446 (“The differences [between Mr. Hardell’s presentation in April 1992 and the dual edge clock proposed for the DDR SDRAM ballot] was almost none. What Mr. Hardell was proposing is essentially what we ultimately wound up with in the standard for DDR.”); Rhoden, Tr. 483; Kellogg, Tr. 5176).

633. At a meeting of the JC-42.3 subcommittee held on May 24, 1995, Hyundai, Texas Instruments and Mitsubishi all made presentations relating to the Synclink technology. (JX0026 at 10-11 and 95-108 (Hyundai presentation); JX0026 at 10 and 109-110 (Texas Instruments presentation)); JX0026 at 11 and 111-112 (Mitsubishi presentation)).

634. The SyncLink presentations included proposals to use dual edge clock technology.

(JX0026 at 112 (“Strobe in Reference Clock both edge for input, positive edge for output”) (Mitsubishi presentation); Rhoden, Tr. 472 (“Mitsubishi was proposing here a reference clock. Both edge for input is basically, if you want to think about it, it's a dual edge input. Both edge for input and positive edge for output, they were using a combination, if you would.”); Calvin, Tr. 1026-1027; Sussman, Tr. 1405, 1408; G. Kelley, Tr. 2575 (“I understood that this was proposing a new concept of double-edge clock. It was similar to the concept that we had discussed for some time called toggle mode where you use the double-edge clock on output control. This was using a double-edge clock on input control with data coming into the DRAM.”); *see also* CX0711 at 156-57 (e-mail from Don Stark to all Rambus staff noting SyncLink’s use of both the rising and falling edges of the clock for data input)).

635. Mr. Sussman’s expectation was that a member with intellectual property relating to dual edge clocking should disclose that interest in response to this presentation. (Sussman, Tr. 1409).

636. JEDEC never standardized the Synclink architecture. (G. Kelley, Tr. 2579; Sussman, Tr. 1415).

637. In October 1995, JEDEC staff distributed to subcommittee members, including Rambus, a survey ballot requested at the September 1995 JC-42.3 meeting. (CX0260). The subject of the survey was “Future Synchronous DRAM (SDRAM) Features.” (CX0260 at 1). Question 3.9-4 asked members whether they believed future generations of DRAMs could benefit from using both edges of the clock for sampling inputs. (CX0260 at 12 (“Does your company believe that future generations of SDRAMs could benefit from using BOTH edges of the clock for sampling inputs?”)). This question related dual edge clocking. (Calvin, Tr. 1033; Lee, Tr. 6689).

638. At a meeting of the JC-42.3 Subcommittee held on December 6, 1995, the results of the survey ballot were tabulated and announced. No clear consensus on the proposed use of dual edge clock in the next generation standard was reached, with seven members responding that the next generation of SDRAMs would benefit from using dual-edge clock technology and nine members responding that it would not. (JX0028 at 45.). Two specific comments relating to dual edge clock technology were recorded in the results of the survey ballot, both supportive of using the technology. ((JX0028 at 45) (“Mitsubishi . . . Dual CLK input/output is simple and effective.”) (“HP . . . Use positive edge for address/command & both edges for data.”)).

639. At a meeting of the JC-42.3 Subcommittee held on March 20, 1996, Samsung made a presentation proposing to use dual edge clock technology in the future SDRAM standard. (JX0031 at 71 (“Future SDRAM - Proposal – Proposed Clocking Scheme . . . – Data in sampled at both edge of Clock into memory . . . – Use both edge of the Strobe clock to sample the memory Data into Controller”); Rhoden, Tr. 512; Calvin, Tr. 1035; Landgraf, Tr. 1719-1720; G. Kelley, Tr. 2581-2582; CX2114 at 85 (Karp, FTC Dep.)).

640. This presentation triggered disclosure under the JEDEC patent policy. (Rhoden, Tr. 514; G. Kelley, Tr. 2582; Landgraf, Tr. 1720 (“Q. Based on your understanding of the JEDEC patent policy, would a member who held patents or patent applications on dual edge clock have been required to disclose that information at this time? A. Yes, the committee had been discussing for a number of meetings what the next generation of Synchronous DRAM should be looking like and what kind of features, and a result of MOSAID's survey ballot as well as other discussions and meetings, the committee was driving towards a set of features for next generation SDRAM for higher performance, and all of these were in the direction of a proposed standard. So, all these presentations were bits and pieces that ended up into the double data rate standard.”).

641. At the same meeting in March 1996, JEDEC considered running a single-edged clock faster in order to double the data rate. (JX0031 at 64; Rhoden, Tr. 542-43 (VLSI proposed using higher speed clocks to achieve data rates of up to 300 mhz)).

642. During the course of its work relating to what ultimately became the DDR SDRAM standard, the JC-42.3 Subcommittee also considered, as an alternative to dual edge clocking, the use of a single edged clock. (CX0371 at 3; Lee, Tr. 6710-13 (showing and discussing two Texas Instruments presentations, one proposing to use a high-speed single-edged clock, and one proposing to use a lower speed single-edged clock with an on-chip clock frequency doubler to double the clock speed of the external clock signal).

643. At the September 10, 1997, JC-42.3 meeting, the subcommittee voted to send a ballot including dual edge clocking to Council. (JX0040 at 8; Lee, Tr. 6714-6715).

644. In 1999-2000, Jedec considered interleaving SDRAM chips on the module in order to double the data rate. (CX0150 at 109-117). In December 1999, Kentron made a proposal to Jedec to interleave SDRAM chips on the module. (CX0150 at 115) (“Operate each bank with its individual CLK . . . Provide/Sample data for every rising edge of both CLKs.”).

5. Other Technologies Considered In Connection With the DDR SDRAM Standard.

(A) Externally Supplied Reference Voltage.

645. At the May 1994 JC-42.3 meeting and the March 1995 JC-16 meeting Richard Crisp of Rambus observed presentations regarding externally supplied reference voltage. (CX0711 at 25, 27; CX0711 at 52, 54).

646. JEDEC included externally supplied reference voltage as an optional feature in the DDR SDRAM standard. (CCFF 564).

(B) Source Synchronous Clocking.

647. During the March 15, 1995 JC 42.3 meeting, Mr. Crisp recorded a Fujitsu representative's suggestion that it would be necessary to use two clocks, a clock-in and clock-out, for high speed operation. (CX0711 at 58). In an e-mail sent to Rambus executives and others, Mr. Crisp stated, "It appears that they are starting to figure out that we have a very good idea with respect to source synchronous clocking. Of course they may get into patent trouble if they do this." (*Id.*).

648. JEDEC included a bidirectional data strobe, or DQS strobe, as part of the DDR SDRAM standard. (CX0234 at 164). The data strobe might be considered to be a form of source synchronous clocking. (Lee, Tr. 6682).

6. Adoption of the DDR SDRAM Standard.

649. In August 1999 JEDEC issued Release 9 of the 21-C standard. (CX0234).

650. Release 9 expanded the original SDRAM standards to include DDR SDRAMs. (CX0234 at 143). It included programmable CAS latency and burst length as well as on-chip DLL and dual edge clocking. (CCFF 653-658)

651. Users requested that JEDEC take everything that related to DDR out of Release 9 and put it in a separate specification. (Rhoden, Tr. 1293-1294). In response to user requests, JEDEC took all of the DDR specifications that had previously issued in Release 9 of the 21-C standard (CX0234) and put them together in one document. (Rhoden, Tr. 1293-1294). That document, entitled "Double Data Rate (DDR) SDRAM Specification" and numbered "JESD79" was published in June 2000. (JX0057; Rhoden, Tr. 1293-1294).

652. Apart from the possibility of some slight updating and clean-up, JESD79 contains the same DDR related material as in Release 9 of the 21-C standard. (Rhoden, Tr. 1294).

7. The Content of the Adopted DDR SDRAM Standard.

653. The DDR SDRAM Standard incorporated in Release 9 of 21-C and JESD79 included many features that had been previously adopted in the first generation SDRAM standard as well as new features such as dual edge clocking and on-chip DLLs. (Sussman, Tr. 1428-1429 ("Many of the features of the Synchronous DRAM are part of the double data rate Synchronous DRAM. Key items that we've added is that now the customer base, the user base, has more experience with higher edge clocks. We're using both edges of the clock rather than just a single edge. Now that we're going faster, we've added this DLL/PLL that used to be on the system board for only some of the systems. So, basically we're adding other system-level features that we know about and arguing about adding them into the component.")); Gross, Tr. 2296-2297

(DDR “was an improvement and had a lot in common with the prior technology SDRAM relative to the way it was utilized to get data in and out of the device.”); Peisl, Tr. 4429 (“DDR was an evolutionary concept in regards to SDR on JEDEC level. Several features of SDR had been taken over into DDR, so it was more or less a logical step for the industry committee to go from SDR to DDR and this is meant by the engineering word "easier"); McWilliams, Tr. 4822 (“DDR is perceived to be evolutionary in that it added some strobes for the data bus but preserved most of the paradigms of SDRAM.”); Bechtelsheim, Tr. 5871- 5872 (DDR is “a modest design change from the original synchronous DRAM in terms of the conceptual similarity of the two designs.”); CX2451 at 20).

654. All of the features included in the DDR SDRAM standard had been considered in the first generation SDRAM standard. (CX2767 at 5 (“Everything that exists within DDR was considered in the previous SDRAM generation but postponed to make sure we could keep the final cost in line with the previous technology (EDO).”)

(A) On-chip DLL.

655. The DDR SDRAM standard requires use of on-chip DLLs. (CX0234 at 176 (“DLL Enable/Diasable Mode for DDR SDRAM/SGRAM . . . The following defines the DLL disable/enable bit in the Extended Mode Register”) and at 197 (“DDR SDRAMs/SGRAMs incorporate an internal DLL (Delay Lock Loop) or equivalent circuitry to shift the output data in time such that the output data is nominally aligned with the input clock, CK.”); JX0057 at 8 (Functional block diagram showing an on-chip DLL); Lee, Tr. 6643 (“Q. Based on your understanding, does the JEDEC DDR SDRAM standard require the inclusion of on-chip DLL? A. Yes”); Rhoden, Tr. 564 (“Q. So, on-chip DLL is not really a requirement for JEDEC Standard 21-C is it? A. Oh, quite the contrary, sir. It is a requirement.”) and 1295; Sussman, Tr. 1427; Peisl 4391-4392)

(B) Dual Edge Clocking.

656. The DDR SDRAM standard requires use of dual edged clocking. (JX0057 at 24; Kellogg, Tr. 5172) The JESD79 DDR SDRAM specification covers SDRAMs that have dual edge clocking. (JX0057 at 5; Sussman, Tr. 1427; Kellogg, Tr. 5172) (JX0057 at 21 (“Each subsequent data-out element will be valid nominally at the next positive or negative clock edge.”).

(C) Programmable CAS Latency and Burst Length.

657. The DDR standard requires the use of programmable CAS latency and burst length. (CX0234 at 150 (mode register table includes SDRAM and DDR SDRAM CAS latency and burst length values); Geilhufe, Tr. 9742-9744; Lee, Tr. 6625)). In June 2000, JEDEC published a Double Data Rate (DDR) SDRAM Specification (JESD79), which was unique to DDR SDRAM.

It continued to include a programmable mode register to define CAS latency. (JX0057 at 12 (“The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst, type, a CAS latency, and operating mode, as shown in Figure 1. The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again of the device loses power. . .”).

8. The Implementation of the Standard.

658. The JEDEC SDRAM and DDR SDRAM standards determined what features were required to be present in JEDEC-compliant DRAMs. (Peisl, Tr. 4384 (“JEDEC's standards were the only source for our own specifications, meaning that Infineon – Siemens or Infineon chip specifications were entirely directed towards the -- 100 percent compatibility towards the JEDEC specifications. The reason for that is very simple, because we knew that all the other industry, all the other DRAM vendors and the controller people were working towards the same specification.”); CX0167 at 28 (Oh, Dep. Tr. 28 (“Q. Why do you say that [JEDEC-related trip reports are] very important? A. Again, JEDEC is the committee who decides the standards of DRAMs, so the DRAMs we are producing are standard parts, so it's very important.”)).

659. Paragraphs 659 - 699 are unused.

V. Rambus - Early Company History & Strategy.

A. The Founding of Rambus.

700. Company documents date the founding of Rambus Inc. to March 1990, when the company received venture capital funding from three firms. (CX0545 at 5; RX0081 at 19). By 1992, its headquarters were located in Mountain View, California, in Silicon Valley. (RX0081 at 1, 3).

701. Rambus is, and at all relevant times has been, a corporation as “corporation” is defined by Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44; and at all relevant times has been and is now engaged in commerce as “commerce” is defined in that same provision. (Rambus Answer at 5, ¶ 6).

702. Rambus was founded to solve “the memory bottleneck” – that is, the perception that existing memory designs of the time “ha[d] not kept up with the speeds of today’s microprocessors.” (CX0545 at 7; see also, e.g., CX0533 at 2 (“the bandwidth of the next generation of processors has far outstripped the capabilities of current memory designs”); CX1282 at 4; RX0081 at 4).

703. Rambus intended to achieve the goal of fixing the memory bottleneck through an “revolutionary” new memory design. (RX0081 at 2). The trademarked name given by Rambus to this “revolutionary DRAM architecture and high speed chip-to-chip data transfer technology” was Rambus DRAM or “RDRAM.” (RX0081 at 3). RDRAM refers to a type of DRAM that is manufactured in accordance with specifications established by Rambus. (CX2112 at 46 (Mooring, Dep.)).

704. Early on, Rambus realized that it was important to its business strategy to protect the intellectual property rights to its technology. (CX0535 at 1). Part of its early strategy to do this was to pursue an application for “a basic, broad patent filed in all major industrial nations” and thereafter “follow up with additional patents on inventions created during the development of the technology.” (CX0535 at 1 (November 1990 Rambus Business Plan)).

705. The only business model that “made any sense” to Rambus co-founder Michael Farmwald “was to patent the technology, convince others to build the device, and charge them royalties.” (Farmwald, Tr. 8095; CX2106 at 26 (Farmwald, Dep.) (“When we were first formed, it was my view that we could not possibly raise enough money to build DRAMs. DRAM fabs cost, even back then they cost, order of a billion dollars. You couldn’t really build DRAMs without owning your own fab, and so a business plan which involved actually building and selling DRAMs was hopeless, and so from the very beginning we were a royalty-based company.”)).

706. The objective of Rambus, as framed in 1989, was not merely to secure patent rights over widely adopted DRAM industry standards, but to “Make A Lot Of Money At The Same Time.” (CX1282 at 5). Rambus intended to achieve this objective, while avoiding the costs of chip fabrication, by charging royalties and license fees for the use of its technology. (*Id.* at 22 (“Nearly All Income in Form of Royalties”).

707. Rambus founder Farmwald knew that “companies never like to pay royalties if they can get out of it.” (CX2106 at 27 (Farmwald, Dep.) (“Rambus was and has always been a royalty-based company, a company that was going to charge royalties. I knew that people would not lightly pay royalties. The DRAM business is a very big business.”)).

708. At the outset, the strategy was to become an industry standard. The founders of Rambus recognized that this plan was not without risks. Two “Risks” in particular identified in the June 1989 Rambus business plan were:

- Need to Establish RamBus as a standard . . .
- Income Depends Mostly on Royalties

(CX1282 at 27). The founders recognized that these two considerations were linked. Thus, its early business planning recognized that “RamBus must be established as a standard to effect large royalty payments.” (CX0533 at 19).

709. The founders also recognized that, once the DRAM industry had adopted a standard, there were strong barriers to change or entry. (RX0015 at 15 (“Once a DRAM or vendor has committed to an architecture unlikely to change.”); *id.* at 9 (“The DRAM industry’s penchant for standardization combined with the RamBus marketing strategy of licensing all the major vendors make it extremely unlikely that any potential competitor would be able to gain critical mass enough to challenge an already established and ubiquitous RamBus chip.”)).

B. Funding the Start-Up.

710. In an effort to receive funding for the start-up of what would become Rambus Inc., the founders approached various venture capital firms: Kleiner Perkins (KPCB), one of the largest venture capital firms in the world; Merrill Pickard Anderson and Eyre (MPAE); and Mohr Davidow. (Farmwald, Tr. 8099). As part of meetings with the venture capital firms, the founders prepared presentations and showed them documents, such as early business plans. (Farmwald, Tr. 8100). These meetings occurred around the time of a June 1989 RamBus Business Plan (CX0533). (Farmwald, Tr. 8100-8101; CX0533 (also included in record as RX0015 and CX0570)).

711. The start-up had significant “financial considerations” and according to the June 1989 business plan, “RamBus” founders (Mr. Farmwald, Mark Horowitz, and James Mannos),

were only able to invest \$75,000 in “seed money” and were seeking an additional \$1.5 million in equity investment. (CX0533 at 4). This amount would only fund the company through “the completion of a prototype and to the development of [its] initial DRAM vendor partnerships.” (CX0533 at 4). Until it signed its revenue producing partners, estimated expenses were \$100,000 per month. (CX0533 at 5).

712. In a meeting with one of the venture capital firms, co-founder Michael Farmwald noted that “much depends on getting a standard which depends upon our patents.” (CX1702 at 3 (emphasis in original); Farmwald, Tr. 8130-31).

713. In March 1990 Rambus Inc. was born when it finally received venture capital funding of \$1.86 million from three firms. (CX0545 at 5; RX0081 at 19).

C. The Basic Rambus Technology.

714. Because from the start the founders believed that “[r]oyalties are the lifeblood of Rambus” (CX2106 at 220 (Farmwald, Dep.)), Rambus placed great importance on promoting and protecting its proprietary technology. The Rambus founders “felt we had a very significant invention. We felt that the only way to protect and to extract value from that invention was to patent it.” (CX2106 at 27 (Farmwald, Dep.)).

715. Rambus saw its proprietary RDRAM technology as offering dramatic improvements over existing memory technology of the time. In 1992 it claimed that RDRAM technology “achieves a ten-fold increase in component throughput” and would result in “dramatically increasing system price/performance.” (RX0081 at 3). In addition, Rambus claimed that use of the RDRAM technology “assures a smaller system with fewer components, and provides the user with a modular, scalable solution.” (*Id.*).

716. The high-speed chip-to-chip data transfer RDRAM technology was intended to be used not only in memory chips themselves, but also to be implemented in other chips including memory controllers, processors, graphics/video chips and other high performance components used in virtually every computer system. (RX0081 at 3). The proprietary Rambus technology was targeted at mainstream applications from consumer digital video products through desktop computers and graphics up to massively parallel computers. (*Id.*).

717. Central to the RDRAM technology was the use of a “narrow, high speed bus” to connect chips and speed the transfer of signals and data between them. (RX0081 at 3, 7). This narrow bus was “a precisely specified, physical and electrical interconnect” between the chips. (*Id.* at 7). The use of a narrow, high-speed bus to carry data between chips is the “basic notion” of the proprietary RDRAM technology (Horowitz, Tr. 8618), and is a characteristic that distinguishes the technology from other memory technologies. (Rhoden, Tr. 400).

718. The typical synchronous DRAM uses a large number of dedicated lines to carry control, address and data signals between the memory controller and the memory chip. (Rhoden, Tr. 401). Control signals specify whether data is being written to or read from the memory; address signals specify the portion of the memory chip that is being accessed; data signals specify the content that is being written to or read from memory. (Rhoden, Tr. 280-82). A typical synchronous DRAM bus contains 100 to 120 parallel lines that are dedicated to carrying control, address and data signals respectively between the memory controller and memory chip. (Rhoden, Tr. 401).

719. By contrast, the RDRAM technology uses a small number of very high speed signals to carry all address, data and control information. (RX2183 at 5). As originally implemented, the RDRAM technology used a narrow bus of only eight lines to carry control, address and data signals between the memory and controller. (Rhoden, Tr. 400-401). In later implementations of the RDRAM technology, this was widened to a bus of sixteen lines (Farmwald, Tr. 8190).

720. In implementing the narrow bus, RDRAM technology contemplates the use of circuitry on the chips at either end of the bus connection to optimize the signals flowing across the connection. (Horowitz, Tr. 8488-90). This circuitry contains high-level logic which implements a protocol for the chip-to-chip information transfer. (RX0081 at 7; Horowitz, Tr. 8489-90).

721. One of the ways that RDRAM technology achieves a high-speed data transfer over the narrow bus is through “multiplexing,” which means that the bus can carry different pieces of information at different points in time. (Horowitz, Tr. 8620). This aspect of the RDRAM interface protocol means that over several clock cycles the bus can carry a combination of address and control and data signals on one or more of the same bus lines. (Horowitz, Tr. 8620-21). (See Rhoden, Tr. 402-03).

722. Another aspect of the RDRAM technology is the use of a “packetized” data transfer protocol. (Horowitz, Tr. 8621; Rhoden, Tr. 403-405). This term means that information is bundled and the bundle may be sent over multiple clock cycles rather than transmitted all at once. (Jacob, Tr. 5465; Rhoden, Tr. 404).

723. The RDRAM technology also contains other distinctive aspects, including a clocking system sometimes referred to as a loop clock to assist in controlling the synchronization of the data transfer between chips (Rhoden, Tr. 404; Horowitz, Tr. 8647), and a method of physically packaging the RDRAM memory chips so that multiple chips could be vertically mounted on one another to occupy a small space (Horowitz, Tr. 8623).

724. The RDRAM technology was sufficiently distinctive that it was widely considered “revolutionary” in the industry and was promoted as such by Rambus. (Farmwald, Tr. 8113-14,

8148, 8304-05, 8463-65; Horowitz, Tr. 8571; Gross, Tr. 2291, 2295-96, 2326; Heye, Tr. 3686-87; MacWilliams, Tr. 4822; Bechtelsheim, Tr. 5817, 5845; Tabrizi, Tr. 9138).

D. The Basic Rambus Patent Application.

725. Rambus filed patent application serial no. 07/510,898 (the '898 application) in the U.S. Patent and Trademark Office on April 18, 1990. (CX1451 at 001-02; Nusbaum, Tr. 1507). The '898 patent application included a descriptive portion, called the "specification," that was 62 pages long and included 15 original drawings. (CX1451 at 3-63, 140-150; Nusbaum, Tr. 1496-97). The '898 patent application contained 150 original claims. (CX1451 at 64-125).

726. In addition to this basic United States patent application, Rambus pursued foreign applications in a number of countries based on the '898 application. (See CCF 1115-21, 1669-75).

727. Despite the stated strategy of seeking "a basic, broad patent" (CX0535 at 1), the specification portion of the United States '898 patent application described the "present invention" as a narrow, multiplexed bus structure. (CX1451 at 9-10, 14; Jacob, Tr. 5461-63; Nusbaum, Tr. 1642-43). (See discussion at CCF 1283 et seq.). Rambus employee Richard Crisp, its representative to JEDEC from 1992 to 1996, read this original patent application in the early 1990's and believed that it was intended to describe the RDRAM system invention, and that it was limited to the proprietary RDRAM technology. (Crisp, Tr. 2927-28).

728. Rambus recognized the possibility that its pending patents would not issue, or would not issue with claims sufficiently broad in scope to block others. (CX0533 at 19 ("Potential Risks and Problems . . . Will patent be enforceable and broad enough to stop imitators.")). But this risk was of less concern to the Rambus founders, who from very early on – based on input from their attorneys – possessed a high degree of confidence in the likelihood of the patents issuing "largely as filed." (CX0535 at 3 ("The base patent was filed in April of 1990. It has been reviewed by all partners who've signed and several others and found to be a strong, broad patent with high odds of being issued largely as filed."); *see also* CX1702 at 3 (1989 notes of founder Michael Farmwald recording comments of a patent attorney who "says 'he takes adequate patent coverage as a given' & says that if we do the job right it will be very hard to get around"))).

729. In connection with the prosecution of its '898 patent application, Rambus was issued a communication by the patent examiner at the United States Patent Office containing a restriction requirement. (Nusbaum, Tr. 1511). A restriction requirement reflects that the examiner has reviewed the application and determined that the application contains claims describing multiple claimed inventions; the applicant is required to elect which of the claimed inventions it wishes to pursue in the application. (Nusbaum, Tr. 1510). The restriction requirement received by Rambus was an 11-way restriction requirement; Rambus responded by

restricting its original application and filing ten divisional patent applications on March 5, 1992, all of which claimed priority based on the filing date of the original '898 application, April 18, 1992. (Nusbaum, Tr. 1511-12; First Stipulations, No. 22, Exhibit A; DX14).

730. Over time, Rambus filed numerous additional continuation and divisional patent applications claiming priority based on the filing date of the original '898 application. (First Stipulations, No. 22, Exhibit A). Prior to June 1996, Rambus filed a total of seventeen continuation and divisional patent applications claiming priority based on the filing date of the original '898 application, and had been issued six United States patents on such applications. (*Id.*). As of April 2003, Rambus had filed sixty-three continuation and divisional patent applications claiming priority based on the filing date of the original '898 application, of which ten were still pending. (*Id.*). As of April 2003, at least 43 United States patents had been issued to Rambus from continuation and divisional applications claiming priority to the original '898 application. (First Stipulations, No. 13).

731. Over time, various of the Rambus continuation and divisional patent applications claiming priority to the '898 application embodied changes and amendments to the claims made in the original '898 application and came to describe aspects of the original invention in ways that were not limited to the proprietary RDRAM technology. (See, e.g., Crisp, Tr. 2927-28). By 2000, Rambus had secured several patents, issued on the basis of continuation and divisional applications claiming priority to the original '898 application, which it asserted against manufacturers of JEDEC-standard SDRAM and DDR memory chips. (See, e.g., First Stipulations, No. 14-16 (August 2000 infringement suit by Rambus against Infineon was based on 56 claims of 4 patents claiming priority to the '898 application)).

E. Promoting Rambus RDRAM Technology as the DRAM Standard.

732. The Rambus founders recognized that the characteristics of the DRAM industry made for the possibility of a lucrative payoff for the company. Early Rambus investors were informed that “[t]he primary business of the RamBus Company” would be to license proprietary technology “to manufacturers of DRAM chips and microprocessors;” that “[t]he DRAM market is . . . highly sensitized to the concept of standardization;” and that Rambus possessed “the ability to set world wide standards for the next generation of DRAM chips and memory subsystems.” (CX0533 at 9).

733. Investors were told that “the patented RamBus technology . . . has the opportunity to establish a single high performance DRAM standard”; that in part due to “[t]he DRAM industry’s penchant [sic] for standardization,” once the Rambus technology was licensed to “all major vendors,” it would be “extremely unlikely that any potential competitor would be able to gain critical mass enough to challenge” Rambus; and that such considerations, including the existence of “strong barriers to entry” by “potential competitors,” made Rambus an “exceptionally attractive investment opportunity.” (CX0533 at 9).

734. In its early planning, Rambus executives recognized that the company faced a sort of chicken-and-egg problem – namely, “Most computer companies will want to wait until RamBus DRAMs are easily available,” whereas “DRAM and CPU companies need to be convinced that computer builders will use it.” (CX1282 at 27). Rambus intended to deal with this in part through the terms upon which it licensed its technology. Rambus recognized that there was a “trade-off of royalty size vs. incentive to develop alternatives” to the Rambus technology (CX0533 at 14), and initially intended to offer licenses at “low enough royalties to discourage ‘rolling your own.’”(CX0533 at 15). However, early planning suggests that once Rambus was established as an industry standard, Rambus intended to charge larger royalty payments. (CX0533 at 19 (“RamBus must be established as a standard to effect large royalty payments.”)).

735. Rambus hired its first (and to date only) CEO – Geoffrey Tate – who joined Rambus in May 1990. (CX0545 at 5). Shortly before arriving on the job as the Rambus CEO, Mr. Tate set forth on paper some of his own strategic thinking for the company. (CX2073 at 52 (Tate, Dep.)) Mr. Tate recorded, among others, each of the following thoughts:

- “RAMBUS has a potential for a very strong value-added in a large number of high-volume systems applications combined with a strong barrier-to-entry in the form of a broad patent;”
- “There are always ways to get around any patent is the assumption that we should make;”
- “If RAMBUS can be seen as a standard . . . it may be very difficult for second solution to develop critical mass in the marketplace;” and
- a “high priority” for RAMBUS should be “to avoid a contending standard from developing.”

(CX0569 at 3).

F. Rambus Efforts to License RDRAM Technology.

736. By the time of a November 1990 business plan prepared by Rambus CEO Tate and discussed with the Rambus Board of Directors. (CX2073 at 85, 87 (Tate, Dep.)) Rambus had set out plans for a phased licensing and promotion of the Rambus proprietary RDRAM technology. At an early stage, Rambus would establish “partnerships” with a small number of semiconductor companies to develop new chip products embodying the RDRAM technology, by persuading them that the quality of the RDRAM technology could give them a competitive advantage over other semiconductor companies. (CX0535 at 1). Rambus also would seek to develop relationships with key systems companies to commit to introducing systems using chips

with the RDRAM technology. (*Id.* at 1-2). Later, the RDRAM technology would be announced publicly “in a big way” when a “critical mass” of partnerships was in place and there had been technical demonstration of the RDRAM technology. (*Id.* at 2). Follow-on licenses then would be sought with other semiconductor and systems companies. (*Id.*).

737. The 1990 business plan recognized that if the Rambus royalty demands for its RDRAM technology were perceived as unreasonable, this might motivate potential licensees to “work around” Rambus patents, in order to avoid paying royalties. (CX0535 at 2 (expressing concern that license fees and royalty rates not be set “so high as to create high motivation to work around them”).

738. In order to prevent the development of competitive technology, Rambus strategy was among other things to take care in its efforts to promote its proprietary RDRAM technology. In its promotion efforts, Rambus in 1990 resolved to “sign non-disclosures with all parties exposed to the technology” and “only license partners to use the technology in a specific manner specified by Rambus.” (CX0535 at 1). The result, it hoped, was to make it “impossible or very difficult for anyone to develop a competitive technology to Rambus.” (*Id.*).

739. By November 1990, Rambus had already begun its efforts to promote and protect its technology. (CX0535 at 4-5). At that date Rambus had filed for, but not yet obtained, a base patent on its technology (*id.* at 3) and had entered into license contracts that compelled partners to use Rambus technology patents and trade secrets only for use in RDRAM-compatible chips (*id.* at 4).

740. By June 1992, Rambus had signed license agreements with NEC, Toshiba and Fujitsu. (CX0543A at 11). By January 1994, Rambus had signed license agreements with Hitachi, Oki, Lucky Goldstar and Intel. (CX0547 at 12).

741. In the course of negotiating with DRAM manufacturers and others, Rambus encountered resistance to its business model, and specifically to the amount of the royalties. (CX0543A at 14 (identifying Sun and Tseng as specific examples); CX0711 at 13 (“Terry Walther of Micron . . . Said they are very nervous about doing a deal. Don’t like license type business he says.”); CX0711 at 61 (“Farhad [Tabrizi] . . . says their #1 issue with the Rambus business proposal is the royalty rate.”)).

742. Rambus estimated the projected weighted average royalty rate for 1993 to be 1.4%. (CX0547 at 12).

743. As Rambus continued to negotiate with potential licensees in the mid-1990's, it continued to encounter resistance with respect to the royalty rates it was seeking. (CX0733 (“Big stumbling block is royalties – they [Samsung] want numbers in 1% or less range.”)).

744. Rambus also sought to restrict the field of use of its license agreements to so-called RDRAM compatible uses only. Most companies accepted this term. Samsung, however, insisted on an agreement without field of use restrictions. (CX0767 (“In my view at this point we can either sign the Samsung contract as is or forget them as a licensee. They have made it abundantly clear that without the ability to use Rambus technology in non-Rambus applications there will be no deal.”)).

745. Rambus was prepared to make compromises during this time period in order to conclude license agreements with DRAM manufacturers. (CX0767; CX0733 (“they [Samsung] want numbers in 1% or less range. We are to try to put together a win/win proposal based on their inputs.”); CX0711 at 62 (Crisp proposed to Hyundai a DRAM royalty rate declining with volume to 1.25%)).

G. Rambus License Presentations.

746. Continuing for many years, Rambus pursued a strategy of actively promoting its proprietary RDRAM technology to companies that were in a position to manufacture memory chips or related chipsets. (See Crisp, Tr. 2931; CX0543A at 7-8).

747. Rambus efforts to promote adoption of its proprietary RDRAM technology included making presentations concerning the proprietary RDRAM technology to memory chip manufacturers and other firms. (E.g. CX2107 at 63 (Oh, Dep.); Bechtelsheim, Tr. 5818-19; G. Kelley, Tr. 2537; Kellogg, Tr. 5052-53). In connection with such efforts, Rambus commonly entered into non-disclosure agreements (“NDAs”) that prohibited the firms from disclosing information concerning the proprietary Rambus technology to others without the consent of Rambus. (E.g. Bechtelsheim, Tr. 5818-19; Rhoden, Tr. 521; Kellogg, Tr. 5052-53).

748. The focus of these presentations was on the advantages Rambus saw of the proprietary RDRAM technology and the unique characteristics of that technology, including its unique bus architecture. (E.g., G. Kelley, Tr. 2538; Sussman, Tr. 1429-31). Rambus’ presentations of the RDRAM technology in the 1992-93 time frame involved a DRAM with a multiplexed bus. (CX2114 at 61-62 (Karp, Dep.)). Joel Karp, who was with Samsung at the time, viewed the Rambus RDRAM as “more revolutionary than evolutionary.” (CX2114 at 63 (Karp, Dep.)).

749. Craig Hampel, Rambus technical director who beginning in 1993 participated in numerous meetings and presentations with DRAM manufacturers and other firms to discuss Rambus technology (Hampel, Tr. 8672, 8729-31), was not aware of any instance in which Rambus representatives told the DRAM manufacturers which aspects of RDRAM were Rambus inventions, or were protected by Rambus patents or patent applications. (Hampel, Tr. 8732-33). Rambus President David Mooring testified that slides used by Rambus in presentations to Rambus customers would “definitely not have put anybody on notice” of the coverage of patents

but would only have generic information about aggregate numbers of Rambus patents and/or patent applications. (CX2112 at 180 (Mooring, Dep.)).

750. Gary Harmon, former Rambus Chief Financial Officer, was involved in negotiating RDRAM licenses for Rambus in the 1993-96 time frame. (CX2070 at 42 (Harmon, Dep.)). Mr. Harmon recalled being involved in discussions with Oki, Fujitsu, Toshiba and NEC from Japan; LG, Hyundai and Samsung from Korea; and Intel, LSI Logic, IBM, Texas Instruments, and Cirrus Logic from the United States, among others. (CX2070 at 42-43 (Harmon, Dep.)). Mr. Harmon did not recall any discussions on the scope or extent of Rambus patents during these negotiations. (CX2070 at 42 (Harmon, Dep.)).

751. Howard Sussman, an employee of NEC and later Sanyo Semiconductor (Sussman, Tr. 1321-22), first learned about Rambus through a presentation made by a Rambus employee in 1991. (Sussman, Tr. 1429). The content of the presentation focused on what were portrayed as the key features of the Rambus RDRAM, which included the use of a low-voltage CMOS driver and packetized input/output (*Id.* at 1430-31). When Mr. Sussman later saw Rambus's European patent application, he did not see anything in it that related to the work going on in JEDEC. (*Id.* at 1445).

752. In April 1992, Gordon Kelley of IBM attended a presentation by Rambus at IBM comparing the proprietary Rambus RDRAM technology with SDRAM. (G. Kelley, Tr. 2537). Following that presentation, Mr. Kelley believed that the Rambus RDRAM was fundamentally different from the SDRAM technology under discussion at JEDEC that any Rambus patents or patent applications would not apply to SDRAMs. (G. Kelley, Tr. 2537-38 (“... the Rambus DRAM was so different from the synchronous DRAM being discussed at JEDEC that I just did not believe that anything [patents or patent applications] that Rambus had on the RDRAM might apply to the SDRAM or to JEDEC.”); *id.* at 2546 (same); *id.* at 2504 (he only understood Rambus intellectual property as applying to the Rambus DRAM)).

753. Desi Rhoden was employed at Hewlett Packard when he began to learn about the Rambus technology in the early 90's. (Rhoden, Tr. 396). Rambus came to HP to give a presentation about their new memory that they were developing. (*Id.*). The presentation was made pursuant to a non-disclosure agreement between Rambus and HP. (Rhoden, Tr. 521). Although Rambus did not say anything at that presentation about pending Rambus patent applications, Rhoden assumed that Rambus probably did have patent applications. (Rhoden, Tr. 521). Rambus never suggested to him that its proprietary technology extended outside the RDRAM architecture. (Rhoden, Tr. 521-22).

754. Andreas Bechtelsheim, a Vice-President for technology at Sun (Bechtelsheim, Tr. 5752), was involved in presentations and discussions with Rambus and understood that Rambus had patent rights that covered its proprietary RDRAM technology. (Bechtelsheim, Tr. 5828-29; 5841-42).

755. Mark Kellogg, an employee of IBM (Kellogg, Tr. 5017), learned about Rambus technology through a presentation by Rambus to IBM in the early 1990's. (Kellogg, Tr. 5052-53). At that time, Mr. Kellogg expected that any Rambus patent activity would be associated with the Rambus proprietary RDRAM product that they were showing to IBM, which was a narrow I/O, high-bandwidth, packetized memory device or card with a loop-back structure and a few other elements. (Kellogg, Tr. 5053).

756. Terry Lee, an employee at Micron, learned about Rambus technology in part from a meeting with Rambus held in 1995. (Lee, Tr. 6601-02). Following the meeting, he and a colleague, Mr. Kevin Ryan, reviewed a set of patent abstracts. (*Id.* at 6607-08). Mr. Lee concluded that the patents appeared to apply specifically to the RDRAM bus structure. (*Id.* at 6610-11 (the RDRAM bus is “the narrow bus with the command/address/data multiplexed with this Rambus architecture and Rambus signaling scheme.”)).

H. The Rambus Alternative Business Strategy.

757. During 1990 and 1991, Rambus focused on its business model of trying to license its proprietary RDRAM architecture. (CCFF 733-736).

758. In December 1991, Rambus attended its first JEDEC meeting “to learn what the competition was working on.” (CX0837 at 1).

759. In February 1992, Rambus engineer Billy Garrett reported back to staff at Rambus concerning events at a JEDEC meeting he was attending: “SDRAMs will happen. They may happen sooner than we want . . .” (CX0672 (“What has happened in the last week borders on the remarkable.”)).

760. In March 1992, Rambus Vice President Allen Roberts contacted outside patent counsel Lester Vincent to discuss JEDEC. (CX1941 at 1). Mr. Vincent’s notes of the meeting reflect the statement, “Said need preplanning before accuse others of infringement.” (*Id.*) Two days later, on March 27, 1992, Mr. Roberts and Richard Crisp met with Lester Vincent in person to discuss JEDEC. (CX1942).

761. In April and May, 1992, Mr. Crisp attended a JEDEC special task group meeting and a regularly scheduled meeting of the JEDEC JC-42.3 Committee respectively. (CCFF 893-99, 902-09). Also in May 1992, Mr. Crisp met with Mr. Vincent to discuss adding claims to Rambus’s pending patent applications. (CCFF 900-01, 910).

762. During this time period, while still pursuing its principal objective of promoting its proprietary RDRAM technology, Rambus was developing an alternative business strategy to deal with the emerging competitive threat posed by the efforts of JEDEC to develop a standard SDRAM technology, as discussed at length below. (CCFF 800 et seq.).

763. By June 1992, Rambus CEO Geoffrey Tate transmitted to the Rambus Board of Directors a comprehensive five-year business plan, which, he explained, was based on “inputs from all of the executives.” (CX0543A at 1). As reflected in the “Executive Summary” of this June 1992 Business Plan, Rambus remained committed to:

- “establish[ing] strong intellectual property barriers”;
- “establish[ing] Rambus as the new interface standard”; and
- “establish[ing] a very high profit stream of technology royalties.”

(CX0543A at 3).

764. With respect to the key goals of establishing Rambus as the new interface standard and establishing a high profit stream of technology royalties (CX0543A at 3), the June 1992 Business Plan acknowledged that Rambus faced two principal impediments: “Resistance to Business Model” and “Competitive Solutions.” (*Id.* at 14). Regarding the former, The Plan reported that some firms “have had a very negative reaction to our business model” including resistance to paying royalties to Rambus and fear that the royalties would make chips containing the Rambus technology “too expensive.” (*Id.*). The principal competitive threat to RDRAM was JEDEC’s emerging standards for “Synchronous DRAMs” which did not suffer from the same “price negative and risk negative associated with Rambus.” (CX0543A at 17; see also *id.* at 16 (“many system customers perceive . . . that Sync DRAMs will be sourced more broadly and more quickly,” and hence “will be much cheaper,” than RDRAMs)).

765. The June 1992 Business Plan continued to emphasize that the “#1 strategy” of Rambus was “to get our parts proven and in the market.” (CX0543A at 16). But the plan also stated a second, alternative patent-based strategy for attacking SDRAMs:

Finally, we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in a position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs.

(CX0543A at 17).

766. The Rambus pursuit of this alternative strategy is the core of the present case, and is discussed at length below. (CCFF 800 et seq.).

767. Paragraphs 767 - 799 are unused.

VI. Rambus Participation in JEDEC.

A. Beginning In Early 1992, and Continuing Throughout the Entire Time It Was a Member of JEDEC and Thereafter, Rambus Intended to Use Its Patents To Monopolize the Technologies Incorporated In the JEDEC Standards.

1. Throughout The Time It Was a Member of JEDEC and Thereafter, Rambus Acted With Knowledge and Intent to Monopolize.

800. From the outset, Rambus planned to obtain monopoly power in the market for technologies used in synchronous DRAMs. (CCFF 708, 709, 732-35; *see also* CX0543A at 7 (“Rambus’s objective is to establish Rambus Technology as the new high volume standard in the 90’s. Our target is to achieve penetration of 50% of DRAMs (and the associated logic ICs) by 1997.”)).

801. Rambus originally planned lawfully to obtain monopoly power in the market for technologies used in synchronous DRAMs by persuading the market to adopt and license its RDRAM technology. (CCFF 736-45).

802. Throughout its entire time at JEDEC, Rambus continued to intend lawfully to obtain monopoly power in the market for technologies used in synchronous DRAMs by persuading the market to adopt and license its RDRAM technology. (CCFF 746-56, 1238-53.)

803. Beginning in 1992, Rambus developed a second plan to monopolize the market for technologies used in synchronous DRAMs, one that did not depend on the market adopting RDRAMs. This second plan was to obtain and later enforce patents covering technologies used in SDRAMs, including JEDEC-compliant SDRAMs. (CCFF 757-66, 911-18, 937-38; *see also* CX0543A at 16-17 (Draft Business Plan: “Our #1 strategy to counter Sync DRAMs therefore is to get our [RDRAM] parts proven and in the market. . . . Finally, we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs. Our action plan is to determine the exact claims and file the additional claims by the end of Q3/92.”); CX1941 at 1 (Vincent notes: “Need preplanning before accuse others of infringement”); CX1949 at 1 (Vincent notes: “what to include in divisional applications . . . so cause problems with synch DRAM...”); CX0702 at 1 (Ware e-mail: “This claim has been written up and filed. This is directed against SDRAMs.”); CX1970 at 1 (Vincent notes: “Enforcement; Sync DRAMS.”); CX0763 at 1 (Crisp e-mail: “I would hope we sue other companies, in particular those that are not licensed.”); CX0831 (Tate e-mail: “tony’s #1 objective right now is to . . . determine what should proactively be done to strengthen our IP position relative to competition.” and requesting staff to forward e-mail talking about “competitive technology developments/directions (e.g. JEDEC meeting

reports, etc.)”); CX1730 at 1 (Tate notes: “SDRAM – now – next . . . 1. Understand our IP . . . 3. Assess our current patents – what claims/strength do we have vs. competition 4. What can we do? . . . 5. Plan of action 6. Implement”)).

804. SDRAM and DDR SDRAM were sources of competition for RDRAM. (Crisp, Tr. 2932 (“Q: . . . you understood that certain people at Rambus believed that DDR SDRAMs could be a potential threat to Rambus’ business, right? A: Yes, that’s correct.”); CX0606 at 2 (“Mr. Mooring then spoke on Rambus vs. Sync. positioning, potential competition from IEEE Ramlink strategy, staffing, marketing communications.”); CX0831 (Tate e-mail citing “JEDEC meeting reports” as an example of “competitive technology developments/directions”); CX0837 at 1 (Crisp e-mail: “At the time we began attending JEDEC we did so to learn what the competition was working on . . .”); CX2069 at 654 (Crisp, Infineon Dep.) (“Q. And DDR was perceived to be a potential threat; right? . . . THE WITNESS: It had that potential, yes.”); CX2073 at 212 (Tate, Micron Dep.) (Tate “understood [SDRAMs] were something that customers were talking about as a competitive alternative.”)).

805. From the time that Rambus first developed its plan, Rambus focused on SDRAMs, and on the SDRAM standard being developed in JEDEC. (CX0606 at 2 (Board of Directors Minutes: “Mr. Crisp reported on the SDRAM status at JEDEC, the Rambus patent strategy and system level difficulties with SDRAMs.”); CX0543A at 16-17 (Draft Business Plan: “Our #1 strategy to counter Sync DRAMs . . .”); CX1949 at 1 (Vincent notes: “what to include in divisional applications . . . so cause problems with synch DRAM...”); CX0702 at 1 (Ware e-mail: “This claim has been written up and filed. This is directed against SDRAMs.”); CX1970 at 1 (Vincent notes: “Enforcement; Sync DRAMS.”); CX0745 at 1 (Roberts note: “This is Lester’s attempt to write the claims for the MOST/SDRAM defense.”); CX0831 (Tate e-mail: “tony’s #1 objective right now is to . . . determine what should proactively be done to strengthen our IP position relative to competition.” and requesting staff to forward e-mail talking about “competitive technology developments/directions (e.g. JEDEC meeting reports, etc.)”).

806. From the time that Rambus first developed this plan, Rambus intended to obtain patents with claims covering SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC. (CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24, 1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99; *see also* CX0543A at 17 (Draft Business Plan: “. . . there are additional claims we can file for our patents that cover features of Sync DRAMs. . . . Our action plan is to determine the exact claims and file the additional claims by the end of Q3/92.”); CX0606 at 2 (Board of Director Minutes: “Mr. Crisp reported on the SDRAM status at JEDEC, the Rambus patent strategy and system level difficulties with SDRAMs.”); CX0831 (Tate e-mail: “tony’s #1 objective right now is to . . . determine what should proactively be done to strengthen our IP position relative to competition.” and requesting staff to forward e-mail talking about “competitive technology developments/directions (e.g. JEDEC meeting reports, etc.)”); CX0738 (Dillon e-mail: “We may be able to make a broader claim for auto-precharge for

any DRAM and therefore gain leverage over SDRAM and MOST.”); CX0740 (Tate e-mail: “this stuff is real critical – I’d like a list of which claims we are making that read directly on current/planned sdrams . . . so i can track progress from lester’s periodic status lists.”); CX1730 at 1 (Tate notes: “SDRAM – now – next . . . 1. Understand our IP . . . 3. Assess our current patents – what claims/strength do we have vs. competition 4. What can we do? . . . 5. Plan of action”).

807. Rambus intentionally joined JEDEC and renewed its membership. (CX0602 at 2 (Rambus’s application for membership) and 6-7, 10-12 (its payment of dues); CCF 878-79, 954, 982, 1039).

808. Rambus intentionally followed the proceedings of JEDEC. (CCFF 871-77, 880-84, 893-98, 902-09, 921-27, 929-31, 940-45, 950-53, 959-61, 968-76, 978-80, 983-86, 996-99, 1009-17, 1026-27, 1031-38, 1041-48, 1062-68, 1070-73, 1078-82, 1096-99.)

809. From the time that Rambus first developed this plan, Rambus intentionally took specific action to obtain patents with claims covering SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC. (CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24, 1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99; *see also* CX1949 at 1 (Vincent notes: “what to include in divisional applications . . . so cause problems with synch DRAM..”); CX0702 at 1 (Ware e-mail: “This claim has been written up and filed. This is directed against SDRAMs.”); CX0745 at 1 (Roberts note: “This is Lester’s attempt to write the claims for the MOST/SDRAM defense.”); CX0831 (Tate e-mail: “tony’s #1 objective right now is to . . . determine what should proactively be done to strengthen our IP position relative to competition.” and requesting staff to forward e-mail talking about “competitive technology developments/directions (e.g. JEDEC meeting reports, etc.)”); CX2092 at 192 (Crisp, Infineon Trial Tr.) (“Q: Am I right, sir, that Rambus was intentionally drafting claims to intentionally cover JEDEC SDRAMs? A: Partially true, yes.”)).

810. Rambus intentionally took information learned at JEDEC and used it to help obtain patents with claims covering SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC. (CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24, 1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99; *see also* CX2092 at 192 (Crisp, Infineon Trial Tr.) (“Q: Am I right, sir, that Rambus was intentionally drafting claims to intentionally cover JEDEC SDRAMs? A: Partially true, yes.”); *id.* at 132 (“Q: And the ideas that you had to add claims to the Rambus patent applications for the mode register and for programmable CAS latency, those were ideas that were spurred on by your attendance at the JEDEC meeting in April and May and participating in this SDRAM standardization effort, right? A: Yeah. Those were our inventions. We had invented those for the RDRAM.”)).

811. Various Rambus JEDEC representatives believed Rambus had pending patent applications that, if issued, would likely cover SDRAMs that complied with the JEDEC SDRAM and DDR SDRAM standards. (CCFF 884, 887, 892, 900-01, 910, 917, 918, 932-36, 937, 938, 939, 948, 958, 962-67, 987-93, 7000-03, 1004-08, 1009-17, 1018-25, 1028-30, 1040, 1049, 1057-58, 1069, 1073, 1077, 1089, 1098; *see also* CX0543A at 17 (Draft Rambus Business Plan: “. . . we believe that Sync DRAMs infringe on some claims in our filed patents; . . .”); CX2070 at 97 (Harmon, Micron Dep.) (Harmon heard “from various people that Rambus’ patents were so fundamental and so broad that they likely covered technology that was being used by any other high-speed DRAM.”); CX2073 at 221-22 (Tate, Micron Dep.) (“I recall that our feeling [in 1992] was that synchronous DRAMS sure looked like they were stemming from inventions that we had done first, and that our understanding is that patents are supposed to protect your inventions, and we assumed that our patents had been filed to do so. And that led us to a conclusion that, hey, we must have some claims they are infringing. . .”). Farnwald, Tr. 8208 (“We certainly in general thought that we had pretty broad claims and that they certainly might cover synchronous DRAMs”).

812. From the time that Rambus first developed this plan, Rambus intended to enforce its patents against SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC, if necessary to monopolize the market for technology used in DRAMs. (CCFF 887, 889-91, 917, 918, 938, 948, 955-57, 981, 997, 1002, 1018-24, 1037, 1059-60, 1069, 1083-87; *see also* CX0543A at 17-18 (Draft Rambus Business Plan: “. . . we will be in position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs.”); CX1941 at 1 (Vincent notes, “Need preplanning before accuse others of infringement”); CX1970 at 1 (Vincent notes: “Enforcement; Sync DRAMS.”); CX0763 at 1 (Crisp e-mail: “I would hope we sue other companies, in particular those that are not licensed.”); CX1730 at 1 (Tate notes: “SDRAM – now – next . . . 3. Assess our current patents – what claims/strength do we have vs. competition 4. What can we do? . . . 5. Plan of action 6. Implement”)).

813. Rambus intentionally did not inform others in the industry about the content of its pending patent applications. (CCFF 909 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111, 1238-59, 1676-1700).

814. Rambus intentionally did not inform JEDEC about any of its pending patent applications. (CCFF 909 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111; CX0837 at 2 (Crisp e-mail: “We decided [during the beginning of the period after we joined JEDEC] that we really could not be expected to talk about potential infringement for patent that had not issued . . .”); *id.* (“ . . . we should re-evaluate our position relative to what we decide to keep quiet about, and what we say we have.”); CX0711 at 68, 73 (Crisp e-mail: in response to Mr. Kelley’s request to inform JEDEC of whether Rambus knows of any patents that may read on SyncLink, “I think it makes no sense to alert them to a potential problem they can easily work around. . . . We may not want to make it easy for all to

figure out what we have especially if nothing looks really strong.”); CX0673 (Crisp e-mail: “Siemens expressed concern over potential Rambus Patents covering 2 bank designs. Gordon Kelley of IBM asked me if we would comment which I declined.”); Crisp, Tr. 3174-75 (Mr. Crisp did not say anything about patent applications at the time he disclosed Rambus’s ‘703 patent; Vice President Mooring chastised Mr. Crisp after disclosing the ‘703 patent.)).

815. After it withdrew from JEDEC, Rambus intentionally took specific action to obtain patents with claims covering SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC. (CCFF 1625-75).

816. After it withdrew from JEDEC, Rambus intentionally did not inform others in the industry about the content of its pending patent applications. (CCFF 1676-1700; *see also* CX0919 at 1 (Tate e-mail: “2. do *NOT* tell customers/partners that we feel DDR may infringe—our leverage is better to wait”); CX0942 (“Our policy so far has been NOT to publicize our patents and I think we should continue with this.”); CX1075 at 2 “We’ve made no comment on whether DDR infringes our patents. . . . Our position is there is insufficient data.”); Hampel, Tr. 8731-33 (Hampel had contacts with Rambus customers “15 to 40 times a month” and he testified that he was not aware of “any instance in which Rambus representatives told the DRAM manufacturers which features of RDRAM were protected by Rambus patents or patent applications”)).

817. Beginning in late 1999, Rambus intentionally began threatening to enforce its patents against manufacturers of SDRAMs and DDR SDRAMs and manufacturers of controllers and graphics controllers that interface with SDRAMs and DDR SDRAMs. Rambus intentionally sent letters and made presentations to companies stating that their products infringed Rambus patents. Rambus intentionally sued two DRAM manufacturers in U.S. federal courts, filed counterclaims against two DRAM manufacturers in U.S. federal courts, and sued three DRAM manufacturers in various foreign courts, in all cases alleging infringement of Rambus patents. (CCFF 1950-2032) .

818. Rambus acted with knowledge that the purpose of JEDEC was to develop open standards. (CCFF 318, 320, 371, 383-85, 418, 430, 823, 871-85, 880, 902-906, 921, 929, 940, 942-43, 950, 959, 968-69, 978-79, 983-85, 994-95, 996, 1009, 1026, 1034-36, 1041-42, 1062-66, 1078, 1080, 1601-02; *see also* CX0903 at 2 (Crisp e-mail: “The job of JEDEC is to create standards which steer clear of patents which must be used in compliance with the standard whenever possible.”)).

819. Rambus acted with knowledge that JEDEC and its members were concerned about a company enforcing patents against companies practicing a JEDEC standard. (CCFF 318, 320, 371, 383-85, 418, 430, 823, 871-85, 880, 902-906, 921, 929, 940, 942-43, 950, 959, 968-69, 978-79, 983-85, 994-95, 996, 1009, 1026, 1034-36, 1041-42, 1062-66, 1078, 1080, 1601-02).

820. Rambus acted with knowledge that JEDEC had a disclosure policy requiring disclosure of patents and patent applications. (CX0672 at 1 (Garrett email: “Fujitsu indicated that they do have patents applied for, but that they will comply with the JEDEC requirements to make it a standard!!!”); CX685 at 1 (Mooring e-mail: “IBM raised the issue that they were aware that some “voting” JEDEC attendees have patents pending on SDRAMs that they have not made the committee aware of. They will come to the next meeting with a list of the offenders.”); CX2092 at 60 (Crisp, Infineon Tr.) (“Sometime in 1995 I received a copy of the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that’s right.”); CX2104 at 950-51 (Crisp, Micron Dep.) (“Q And when you got it [JEDEC manual 21-I] and read it, then it was clear that the manual required disclosure of both patents and patent applications, wasn’t it? A Yes, if they related to the work of the committee.”); CX2104 at 851-52 (Crisp, Dep.) (Crisp’s understanding of JEDEC’s written patent policy was that JEDEC members “wanted to know about both patents and patent application that might relate to the works that were going on within JEDEC.”)).

821. Rambus representatives acted with knowledge that Rambus’s membership in and attendance at JEDEC meetings gave rise to a risk of equitable estoppel, which might prevent Rambus from enforcing its patents against JEDEC members in the future. (CX1942 at 1 (Vincent Notes: “I said there could be equitable estoppel problem if Rambus creates impression on JEDEC that it would not its patent or patent appl[icatio]n”); CX3125 at 321 (Vincent, Infineon Dep.) (“The downside risk was that somebody was going to raise the issue of equitably estoppel if Rambus attended JEDEC”); CX1958 at 1, 15-16 (“Stambler v. Diebold, Inc. . . . Plaintiff’s claim is estopped. ‘Plaintiff had a duty to speak out and his silence was affirmatively misleading. Plaintiff could not remain silent while an entire industry implemented the proposed standard and then when the standards were adopted assert that his patents covered what manufacturers believed to be an open and available standard.”); Diepenbrock, Tr. 6214-17 (Diepenbrock told “Mr. Crisp that he was running a risk that equitable estoppel might apply to his actions at JEDEC.” “. . . [T]his risk to Rambus was that some of its patents could be rendered unenforceable”).

2. Rambus Understood That Its Interests And Actions as a JEDEC Member Were Contrary to the Purposes and Rules of JEDEC, and It Participated in JEDEC in Bad Faith.

822. Rambus did not participate in JEDEC in good faith. (Sussman, Tr. 1460-61 (Rambus did not comply with “the good faith requirements set forth [in the EIA Legal Guides]”); Kelley, Tr. 2745-46 (Richard Crisp “was not dealing in good faith with me.”); Appleton, Tr. 6396 (Micron is asserting its complaint that Rambus was “in violation of antitrust laws, that there was fraud and bad faith.”); CCF 803-821).

823. Richard Crisp, the JEDEC representative for Rambus beginning in May 1992, understood that the job of JEDEC was to create, whenever possible, standards that steer clear of patents that must be used in compliance with the standards. (CX0903 at 1; Crisp, Tr. 2941).

824. Mr. Crisp believed that the most valuable patents are ones that must be used to be in compliance with the standard. The reason is that such patents cannot be avoided. (CX0903 at 1; Crisp, Tr. 2941 (“Q: And the reason they’re valuable is that such patents cannot be avoided. Is that right? A: Well, in the situation to where you want to build a device that’s compliant with the standard, whatever the standard is.”)).

825. Rambus pursued interests contrary to those of JEDEC and its members. Rambus never had any plans to manufacture, use or support products that conformed to the JEDEC SDRAM or DDR SDRAM standards. (Crisp, Tr. 2931). Rather, Rambus was promoting its RDRAM architecture. (Crisp, Tr. 2931)

826. Individuals at Rambus, including Mr. Crisp, believed that JEDEC-compliant DDR SDRAMs could be a potential threat to Rambus business. (Crisp, Tr. 2931-32; *see also* CX0831 (Tate identified JEDEC as an example of a competitive DRAM); *see also* CCFF 918, 1089, 1616-24, 1626, 1676-78, 1685, 1687, 1690-95).

827. Mr. Crisp, Billy Garrett, and others at Rambus hoped that JEDEC would fail to develop a widely used standard for SDRAM and DDR SDRAM, as they did not want to see potential competitive devices appear on the market. (CX0672 at 1 (Garrett e-mail: “SDRAMs will happen. They may happen sooner than we want, and they may become quite standardized and highly multi-sourced.”); CX1708 at 3 (“It really looks like there is a lot of momentum against us in the main memory arena. It seems like the group is pretty set on using the SDRAMs for memory.”); Crisp, Tr. 2933 (“Q: You didn’t have any particular interest in seeing JEDEC succeed in developing a widely used standard for SDRAM, did you? A: I think that answer is correct, yes. Q: You also didn’t have any interest in seeing JEDEC succeed in developing a widely used standard for DDR SDRAM, did you? A: I was not interested in seeing potential competitive devices appear on the market.”)).

828. Mr. Crisp withheld technical information that might have helped JEDEC. (CX0711 at 23 (Crisp May 1994 email: “The key thing everyone is missing is the failure to appreciate that the pinouts set over a year ago eliminate the possibility of routing the clocks in a way that naturally avoids the problems of clock skew”); CX0711 at 169 (Crisp September 1995 email: “Another thing they are going to do is have VTT track Vref, which Srinivas tells me is something we have determined to be a no-no based on our work in the lab”).

829. Rambus voted “no” on four ballots relating to technologies proposed for the SDRAM standard. (CCFF 921-27). As least some JEDEC members believed that Rambus was voting “no” in an attempt to delay completion of a standard that would compete with RDRAM.

(Sussman, Tr. 1395 (“ . . . the activity of Rambus was more to delay the standardization process as this was basically a competing option for the Rambus DRAM, so not assisting in the standards.”)).

830. At the very first JEDEC meeting he attended for Rambus, Mr. Crisp witnesses some dissension among some JEDEC members at the meeting, and suggested to Rambus colleagues that word of the dissension be leaked to the press to the competitive advantage of Rambus. (CCFF 893-99; Crisp, Tr. 2934-35; CX1708 at 5). Mr. Crisp told his colleagues that such an action could lead to censure by JEDEC but “should help our air war.” (CX1708 at 5; Crisp, Tr. 2935 (the term “air war” referred to the desire of Rambus to have people use the proprietary RDRAM architecture)).

831. Gordon Kelley identified a proposal to plant a story with the press about dissension within JEDEC as “an example of not having good faith or not showing good faith” because it could “undermine the JEDEC process.” (G. Kelley, Tr. 2523-24).

832. Knowing that JEDEC’s purpose was to develop open standards, Rambus, without informing JEDEC, nevertheless used information obtained from JEDEC to ensure that it developed patents with claims that covered the JEDEC standards. (CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24, 1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99).

833. One of the reasons why Rambus began attending JEDEC meetings was to learn what its competition was working on. (CX0837 at 1-2) (Crisp 1995 email: “At the time we began attending JEDEC we did so to learn what the competition was working on and what sort of performance systems using that technology would be able to achieve and what sorts of issues would arise when designing with the devices (primarily SDRAM/SGRAM).”).

834. Rambus used the information it obtained at JEDEC to help refine the claims in its pending patent applications to ensure that its claims would cover the JEDEC standards. (CX2092 at 192 (Crisp, Infineon Tr.) (“Q: Am I right, sir, that Rambus was intentionally drafting claims to intentionally cover JEDEC SDRAMs? A: Partially true, yes.”); CX0831 (Tate e-mail: “tony’s #1 objective right now is to understand competitive technology, get up to speed on all of our patents filed, assess how many and how strong our current patents /claims are vs. competition, and determine what should proactively be done to strengthen our IP position relative to competition”; and requesting staff to forward to him copies of JEDEC meeting reports).

835. During his time as JEDEC representative for Rambus, Mr. Crisp learned that meetings of JEDEC committees and subcommittees were conducted in accordance with the EIA Legal Guides. (Crisp, Tr. 2945).

836. Mr. Crisp was aware that the EIA Legal Guides provided that all EIA standardization programs shall be carried on in good faith. (Crisp, Tr. 2946-47).

837. Mr. Crisp was aware that JEDEC was controlled by EIA rules regarding use of patents. (Crisp, Tr. 2947-48). Mr. Crisp understood that the EIA rules stated that requirements in EIA standards which called for the use of patented items should be avoided. (Crisp, Tr. 2948). Mr. Crisp understood that the EIA rules provided that no program of standardization should refer to a product on which there is a known patent unless all the technical information covered by the patent was known to the standards committee. (Crisp, Tr. 2948).

838. Mr. Crisp understood that the purpose of JEDEC was to develop open standards. (CX0903 at 2 (Crisp e-mail: “The job of JEDEC is to create standards which steer clear of patents which must be used in compliance with the standard whenever possible.”)).

839. Mr. Crisp understood that JEDEC and its members were concerned about a company enforcing patents against companies practicing a JEDEC standard. (CX0711 at 1 (Crisp e-mail: “TI was chastized for not informing JEDEC that it had a 1987 patent on quad CAS devices . . . The bottom line is that all quad CAS devices will be removed from standard 21C.”); CX0711 at 16 (Crisp e-mail: “The whole [quad CAS] issue got pretty nasty . . . Sussman . . . made a motion that TI withdraw from JEDEC pending resolution of the patent issue!”); CX0903 at 2 (Crisp e-mail: “The job of JEDEC is to create standards which steer clear of patents which must be used in compliance with the standard whenever possible.”)).

840. Mr. Crisp, during the time he was the primary JEDEC representative for Rambus, understood that there was a patent policy at JEDEC. (Crisp, Tr. 2949). One of the ways that Mr. Crisp learned of the patent policy was because at the meetings of the JC42.3 Committee that Mr. Crisp attended, Jim Townsend generally started the meeting with a discussion of the patent policy. (Crisp, Tr. 2949).

841. Mr. Crisp was aware that JEDEC had a disclosure policy requiring disclosure of patents and patent applications. (CX2104 at 851-52 (Crisp, Micron Dep.) (Crisp’s understanding of JEDEC’s written patent policy was that JEDEC members “wanted to know about both patents and patent application that might relate to the works that were going on within JEDEC.”); CX2092 at 168 (Crisp, Infineon Tr.) (“Q: And what [the slide] said and what [Mr. Townsend] said to everyone in the committee is that the policy applied equally to patent applications as it did to patents, right? A: I think he said that. I don’t remember it very clearly, but I think he said that.”)).

842. Mr. Crisp and other Rambus representatives knew that certain JEDEC members disclosed patent applications at JEDEC. (Crisp, Tr. 2950-51) (“Q: And you recall that that [patent tracking list] includes not just patents, but also patent applications? A: I think it included a few patent applications from my recollection.”); CX2104 at 851-52 (Crisp, Micron Dep.)

(Crisp's understanding of JEDEC's written patent policy was that JEDEC members "wanted to know about both patents and patent application that might relate to the works that were going on within JEDEC."); CX0672 at 1 (Garrett email: "Fujitsu indicated that they do have patents applied for, but that they will comply with the JEDEC requirements to make it a standard!!!"); CX685 at 1 (Mooring e-mail: "IBM raised the issue that they were aware that some "voting" JEDEC attendees have patents pending on SDRAMs that they have not made the committee aware of. They will come to the next meeting with a list of the offenders.")).

843. Throughout the period when Rambus participated in JEDEC, Mr. Garrett and Mr. Crisp informed executives and others at Rambus that JEDEC members disclosed pending patent applications that pertained to the work at JEDEC. (E.g. CCF 882-83, 1080; CX0672 at 1 (Garrett email reporting February 1992 disclosure of Fujitsu patent application); CX0711 at 169 (Crisp September 1995 email: "Fujitsu stated yesterday that they have patents pending on SSTL"); CX0711 at 192 (Crisp December 1995 email: "MOSAID has a pending patent application for PLL/DLL on SDRAMs . . . they will be in compliance with the JEDEC patent policy."); *see also* CX0685 at 1 (Mooring December 1992 email noting IBM comment that some "JEDEC attendees have patents pending on SDRAMs"))).

844. Mr. Crisp was aware of the patent tracking lists shown by Mr. Townsend, which included both patents and patent applications. (Crisp, Tr. 2950). Mr. Crisp received minutes from JEDEC meetings, which generally included the slides from Mr. Townsend's presentations concerning the patent policy. (Crisp, Tr. 2951).

845. As of mid-1995, Rambus representative Mr. Crisp knew that JEDEC manual 21-I called for the disclosure of patent applications. (CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); CX2104 at 950-51 (Crisp, Micron Dep.) ("Q And when you got it [JEDEC manual 21-I] and read it, then it was clear that the manual required disclosure of both patents and patent applications, wasn't it? A Yes, if they related to the work of the committee.")).

846. During the period when Rambus participated in JEDEC, Mr. Crisp spoke with Desi Rhoden, longtime member of JEDEC and later Chairman of JEDEC (Rhoden, Tr. 283, 284-85), to inquire about the JEDEC patent disclosure policy. (Rhoden, Tr. 518-19). Mr. Crisp inquired specifically about the application of the policy to patent applications; Mr. Rhoden informed Mr. Crisp that in the patent disclosure policy, the word patent applied to everything that was in the patent process, and necessarily included patents and patent applications. (Rhoden, Tr. 519).

847. Mr. Rhoden told Mr. Crisp that if he would like to have a legal opinion, he could contact John Kelly. (Rhoden, Tr. 519). During the time that Rambus was a member of JEDEC, Rambus never contacted John Kelly, the legal counsel for JEDEC, with any questions about

EIA's or JEDEC's rules. (J. Kelly, Tr. 2057).

848. On at least two separate occasions, Mr. Crisp refused to respond to questions from Mr. Gordon Kelley, the Subcommittee Chairman, regarding the possible existence of Rambus patents relating to a presentation at JEDEC. (May 1992: CCF 902-909, 1247-48; CX0673 at 1 (“Gordon Kelley of IBM asked me if we would comment which I declined.”); CX2089 at 130-131, 136-137 (Meyer, Infineon Trial Tr.); September 1995: CCF 1044, 1062-68; JX0027 at 26 (“At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synlink proposal.”)).

849. Rambus knew that its failure to disclose the existence of its issued '327 patent and its pending patent applications to JEDEC could serve to equitably estop Rambus from enforcing its patents as to JEDEC participants. (Order, February 26, 2003 at 9; Order, February 27, 2003; *see also* CCF 885-91, 955-57, 1056-61, 1083-87, 1090).

850. Rambus representatives understood that Rambus's membership in and attendance at JEDEC meetings gave rise to a risk of equitable estoppel. Rambus representatives understood that risk to be that the doctrine of equitable estoppel might prevent Rambus from enforcing its patents against JEDEC members in the future. (CCF 885-91, 955-57, 1056-61, 1083-87, 1090; CX1942 at 1 (Vincent notes: “I said there could be equitable estoppel problem if Rambus creates impression on JEDEC that it would not its patent or patent appl[icatio]n”); CX3125 at 321 (Vincent, Infineon Dep.) (“The downside risk was that somebody was going to raise the issue of equitably estoppel if Rambus attended JEDEC”); CX1958 at 1, 15-16 (“*Stambler v. Diebold, Inc.* . . . Plaintiff's claim is estopped. ‘Plaintiff had a duty to speak out and his silence was affirmatively misleading. Plaintiff could not remain silent while an entire industry implemented the proposed standard and then when the standards were adopted assert that his patents covered what manufacturers believed to be an open and available standard.”); Diepenbrock, Tr. 6214-17 (Diepenbrock told “Mr. Crisp that he was running a risk that equitable estoppel might apply to his actions at JEDEC.” “. . . [T]his risk to Rambus was that some of its patents could be rendered unenforceable”)).

851. On at least seven separate occasions, Rambus in-house or outside legal counsel informed Rambus representatives, including Rambus CEO Geoff Tate, Rambus Vice President Allen Roberts, and Rambus's primary JEDEC representative Richard Crisp, that they faced a risk that, based on Rambus's participation in JEDEC, the doctrine of equitable estoppel might preclude Rambus from enforcing its patents against JEDEC members. (CCF 885-91, 955-57, 1056-61, 1083-87, 1090; CX1942 (Vincent notes, 3/27/92: “I said there could be equitable estoppel problem”); CX1958 at 1, 12 (Vincent letter and attachment, 5/5/93: “Two possible legal theories for non-enforcement: 1) estoppel? 2) antitrust?”); CX3126 at 552-54 (Vincent, Dep.) (at some point in time, Vincent talked with Crisp about the upside potential versus downside risk of participating in standard setting bodies); CX0837 at 1 (Crisp e-mail, 9/23/95: “Tony's worst case scenario regarding estoppel”); CX1990 at 1 (Vincent letter, 12/19/95 (“the [FTC] charged that

Dell restricted competition in the personal computer industry and undermined the standard-setting process by threatening to exercise undisclosed patent rights against computer companies adopting the VL-Bus standard.”); CX3124 at 190-94 (Vincent, Dep.) (describing meeting over lunch with Geoff Tate and Maria Sobrino at which they discussed the Dell consent order); CX3126 at 537-40 (Vincent, Dep.) (describing 1/11/96 meeting at Rambus to discuss the Dell consent order and the IEEE letter); *see also* CX3126 at 554 (Vincent, Dep.) (Vincent may have had another conversation with Crisp and Tony Diepenbrock); CX3127 at 113-14 (Vincent, Dep.) (same)).

852. Lester Vincent does not recall being aware of the EIA Legal Guides, the JEDEC Manual 21-I, the Townsend presentations at the JC-42.3 meetings, the patent tracking list, the JEDEC sign-in sheet, internal Rambus emails discussing disclosures within JEDEC, specific requests made to Rambus regarding Rambus patents, any specific presentations made within JEDEC, or emails within Rambus commenting on whether presentations at JEDEC would be covered by Rambus patent rights. (Vincent, Tr. 7996-98). Yet, he still advised Rambus that there was a downside risk that somebody could raise the issue of equitable estoppel. (CX3126 (Vincent Dep. at 191, 197, 320); CX3127 (Vincent Dep. at 114-115); *see also* CX1928 (Vincent notes, undated: (“– No further participation in any standards body (if there has been any) – do not even get close!!”))).

853. Rambus knew or should have known from its pre-1996 participation in JEDEC that developing JEDEC standards would require the use of patents held or applied for by Rambus. (See Order, February 26, 2003 at 9; *see also* CCFF 884, 887, 892, 900-01, 910, 917, 918, 932-36, 937, 938, 939, 948, 958, 962-67, 987-93, 7000-03, 1004-08, 1009-17, 1018-25, 1028-30, 1040, 1049, 1057-58, 1069, 1073, 1077, 1089, 1098).

854. Mr. Crisp admitted that he went to JEDEC meetings and saw proposals for standardization for SDRAM; that following the presentations he or others met with the Rambus’s outside patent lawyer to work on claims for pending Rambus patent applications; and that the intent was to make the claims broad enough that they would cover an SDRAM using the features that Mr. Crisp had seen at the JEDEC meetings. (CX2092 at 70-72 (Crisp, Infineon Trial Tr.) (“Q: And what you did in those meetings [with the Rambus patent lawyer] was work on new claims for the Rambus pending patent applications, and your intent was to make them broad enough that they would cover an SDRAM using the features you had seen at the prior [JEDEC] meetings. Isn’t that right? A: In some cases that was true.”); *id.* at 134 (“ . . . Rambus was adding claims, in Rambus’ words, specifically directed to the SDRAM; isn’t that right? . . . A: I believe that there were some people at Rambus that were attempting to do that.”); *id.* at 139-40 (after the July 1992 JEDEC meeting, he had conversations with Mr. Vincent about amending or adding claims to the original 1990 application); *id.* at 132 (“Q: And the ideas that you had to add claims to the Rambus patent applications for the mode register and for programmable CAS latency, those were ideas that were spurred on by your attendance at the JEDEC meeting in April and May and participating in this SDRAM effort, right? A: Yeah. Those were our inventions. We

had invented those for the RDRAM.”); *id.* at 192 (“Q: Am I right, sir, that Rambus was intentionally drafting claims to intentionally cover JEDEC SDRAMs? A: Partially true, yes.”)).

855. Programmable CAS latency, programmable burst, double edge data transfer and PLL/DLL, as related to the patents asserted against Infineon by Rambus, were all technologies that Mr. Crisp saw discussed at JEDEC and for which Rambus had patent applications that covered aspects of the technologies. (CX2092 at 258-59 (Crisp, Infineon Trial Tr.) (“Q: And those are the very features that you saw at JEDEC and that you met with your lawyer about and that Rambus’ patent applications ultimately changed into; isn’t that right? A: I think those issues were discussed there in some form or another, and we certainly had patent applications that covered aspects of those, of those technologies.”)).

856. While Rambus was a member of JEDEC, Mr. Garrett or Mr. Crisp saw JEDEC members propose to incorporate into a JEDEC standard:

1. low voltage swing signaling,
2. programmable CAS latency,
3. programmable burst/wrap length,
4. externally supplied reference voltage,
5. two banks,
6. dual edge output/input,
7. source synchronous clocking,
8. auto-precharge, and
9. on-chip PLL or DLL.

(Crisp, Tr. 3024, 3035-45, 3052-53; 3107-08, 3165, 3200-3201; *see also* DX0028; CX0670 at 1 (programmable latency and wrap length, single clock edge); CX0672 at 1 (two banks, reduced voltage swing parts); CX1708 at 2 (source synchronous clocking); CX0680 at 1-2 (programmable latency, programmable burst length, two banks, auto-precharge); CX0711 at 25, 31 (externally supplied reference voltage); CX0711 at 52, 54 (externally bussed reference voltage); CX0711 at 36-37 (on-chip PLL); CX0711 at 56, 58 (source synchronous clocking); CX1320 (double edge clocking); CX0905 (CX1320 contained confidential JEDEC material); *See also* CCF 876, 894, 901, 919, 925, 926, 930, 933, 937, 939, 948, 960, 962-65, 989-93, 997-98, 1000-03, 1004-06, 1010-16, 1032, 1037, 1045, 1070-73, 1078-81, 1098).

857. While Rambus was a member of JEDEC, Mr. Garrett or Mr. Crisp believed that Rambus might have pending applications containing claims covering, or be able to obtain – based on its April 1990 application – patent rights covering:

1. low voltage swing signaling,
2. programmable CAS latency,
3. programmable burst/wrap length,

4. externally supplied reference voltage,
5. two banks,
6. dual edge output/input,
7. source synchronous clocking,
8. auto-precharge, and
9. on-chip PLL or DLL.

(Crisp, Tr. 3027-3028, 3060-64, 3104-08, 3164-71, 3178-80; CX1949 at 1 (Vincent notes: “*1) DRAM – multiple open row addresses 2) DRAM – programmable latency via control reg . . . 4) using phase lock loop on DRAM . . .”); *id.* at 5 (“must claim source synch clocking”); CX0672 (regarding reduced voltage-swing parts: “. . . we could use our patents to keep current-mode interfaces off of DRAMs . . .”); CX0702 (identifying programmable CAS latency, DRAM with PLL clock generation, DRAM with multiple open rows, DRAM with externally supplied reference voltage, and DRAM using low-voltage-swing signal levels); CX0738 (“We may be able to make a broader claim on auto-precharge for any DRAM . . .”); CX0734 (Roberts believed that, based on the teachings of the ‘898 application, Rambus could enhance its claim coverage with respect to, *inter alia*, “Use of both edges of the clock,” “Multiple . . . internal DRAM memory regions (banks),” “selective precharging of banks” and “Use of control registers . . . which control RAS and CAS access timing”); CX1949; CX0711 at 25, 31 (regarding externally supplied reference voltage: “(Allen, I believe this was one of the claims you, Lester, Tracy and I wrote up in late ‘91, right?”); CX0711 at 36-37 (“What is the exact status of the patent with the PLL claim?*****”); CX0711 at 56, 58 (regarding source synchronous clocking: “Of course they may get in to patent trouble if they do this”); *see also* CCFF 876, 894, 901, 919, 925, 926, 930, 933, 937, 939, 948, 960, 962-65, 989-93, 997-98, 1000-03, 1004-06, 1010-16, 1032, 1037, 1045, 1070-73, 1078-81, 1098).

858. Every patent that Rambus has asserted in patent litigation involving the SDRAM and DDR standards can trace its lineage to one of two patent applications in the ‘898 family: either the 08/222,646 (“‘646”) or the 07/847,961 (“‘961”). (First Stipulations, No. 22; Exhibit A to First Stipulations, No. 22; Nusbaum Tr. 1506-1508; *see also* DX0014). The ‘646 and ‘961 applications, as well as the ‘490 application which was a continuation of the ‘961 application, and the ‘327 patent which issued from the ‘646 application, were pending while Rambus was a member of JEDEC (CCFF 1008, 1028, 1049, 1076-77, 1092-95) and contained claims that related to ongoing work at JEDEC (CCFF 1028, 1049, 1125-63, 1164-82, 1199-1215, 1216-37). Rambus never disclosed to other JEDEC participants the existence of its patent or pending patent applications that were required for use of the developing JEDEC standards. (Order, February 26, 2003 at 9; Order, February 27, 2003; *see also* CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

859. At no time while Rambus was a member of JEDEC did it inform JEDEC of the existence of its issued U.S. patent no. 5,513,327. At the time of its withdrawal from JEDEC, Rambus did not inform JEDEC of the existence of its issued U.S. patent no. 5,513,327. (Crisp,

Tr. 3381, 3384; CX0887; CCF 1092-95, 1109-14).

860. At no time while Rambus was a member of JEDEC did it inform JEDEC of the subject matter of any of its pending patent applications. At the time of its withdrawal from JEDEC, Rambus did not inform JEDEC of the subject matter of any of its pending patent applications. (Crisp, Tr. 3386-87; CX0887 (Rambus's withdrawal letter from JEDEC: "Rambus has also applied for a number of additional patents in order to protect Rambus technology."); *See also* CCF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

861. At no time while Rambus was a member of JEDEC did it inform JEDEC that it had pending patent applications containing claims that related to the on-going work of JEDEC. (CX2092 at 148 (Crisp, Infineon Tr.) ("Q: Did you ever stand up in JEDEC in the four years that you attended meetings and watch the SDRAM standardization, did you ever stand up and say, Stop doing this; I own it? A: No, I never said that."); Crisp, Tr. 3176 ("Q: Between the time that you disclosed the '703 patent [in September 1993] and the time that you submitted the withdrawal letter to JEDEC, you did not disclose any Rambus patent applications at JEDEC, did you? A: That's correct."); CX0887 (Rambus's withdrawal letter from JEDEC); *See also* CCF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

862. At no time while Rambus was a member of JEDEC did it inform JEDEC that it believed it had pending patent applications containing claims that related to the on-going work of JEDEC. (Crisp, Tr. 3084 ("Q. My question is you did not say anything with respect to Rambus – potential Rambus patents. Isn't that right? A. Yes, that's correct"); Crisp, Tr. 3064 ("Q. So you just sat there in silence and watched these presentations go forward. Isn't that right? A. Yes, that's correct"); *see also* Crisp, Tr. 3066, 3067-68 ("Q. And at this meeting, Mr. Sussman said that he didn't think that that foreign Rambus patent application would be a concern for the JEDEC SDRAM standardization effort. . . And you didn't say anything at that time to contradict Mr. Sussman, did you? A. I think that's correct, yes."); *See also* CCF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111)

863. At no time while Rambus was a member of JEDEC did it inform JEDEC that it believed it could easily amend its pending patent applications to add claims that related to the on-going work of JEDEC. (CCF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

864. At no time while Rambus was a member of JEDEC did it inform JEDEC that it planned to amend its pending patent applications to add claims that related to the on-going work of JEDEC. (CCF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

865. At no time while Rambus was a member of JEDEC did it inform JEDEC that it was working with its patent counsel for the purpose of amending its pending patent applications to add claims that would relate to the on-going work of JEDEC.(CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

866. Never once did Mr. Crisp inform JEDEC that Rambus believed it had invented, and could claim patent rights to, technologies being discussed at JEDEC. (CX2092 at 148, 150 (“Q. But you never once in four years of attending JEDEC meetings told JEDEC what they were doing was stealing Rambus’ designs, did you? A. That’s correct, I never once did say that.”); *id.* at 187 (“Q. [N]ever once in four years did you stand up and say, I own that; you can’t have it, right? A. That’s correct”).

B. As A JEDEC Member, Rambus Simultaneously Pursued Patent Applications Covering JEDEC Work While Withholding From JEDEC Any Meaningful Information Concerning Rambus Intellectual Property Rights.

867. The first Rambus employee to attend a JEDEC meeting on behalf of the company was William (“Billy”) Garrett, who first attended a meeting in early December 1991. (CX0670 at 1). Mr. Garrett was later replaced as the Rambus primary representative at the JC 42.3 Committee by Richard Crisp, who served as primary representative from May 1992 until Rambus withdrew from JEDEC. (Crisp, Tr. 2929). Rambus submitted a letter withdrawing as a member of JEDEC in June 1996. (CX0602 at 8; CX0887; CX0888).

868. For a brief period of time, Rambus considered presenting its proprietary RDRAM design to JEDEC for evaluation as a standard. (CX0671 at 1 (Tate email in Dec. 1991 referring to “develop[ing] a plan . . . to take Rambus to JEDEC”); CX1705 at 30 (Roberts handwritten notes: “12/18 Board Meeting . . . JEDEC submission. talk to Richard about creating a plan for JEDEC”)). Rambus co-founder Horowitz testified that one of the reasons Rambus initially joined JEDEC was its desire to have RDRAM adopted as an industry standard. (Horowitz, Tr. 8588-89; see also CX2101 at 279 (Horowitz, Micron Dep.)). Rambus was invited to attend its first JEDEC meeting as a guest of Toshiba, in part because Toshiba suggested Rambus consider taking the RDRAM to JEDEC. (CX2054 at 43-44 (Mooring, Infineon Dep.)).

869. However, while Rambus perceived its technology as revolutionary (Farmwald, Tr. 8304-8305), it came to recognize that customers would not move to Rambus unless their applications required the added performance (Farmwald, Tr. 8334). (See also CX2106 at 73 (Farmwald, Dep.) (“[T]he main feedback was that it was considered too big a leap. That it was too revolutionary. That they wanted evolutionary approaches, and that SDRAMs were perfectly fine for the next generation.”); Horowitz, Tr. 8571, 8577, 8579-8582 (although Rambus’ technology was revolutionary, customers chose the least-risk solution that met their needs and not necessarily the “best” solution); CX1322 at 15).

870. Shortly after its representatives began attending JEDEC meetings, Rambus recognized that it might be able to assert patent rights over technologies under consideration at JEDEC in connection with a proposed synchronous DRAM standard and future generations of DRAM technology. (CCFF 884, 885-92, 911-20, 937-38). While it publicly promoted its proprietary RDRAM technology as the solution for computer memory technology, Rambus secretly sought to gain advantage over the competing technological standards under development at JEDEC. (See, e.g., CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24, 1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99). Over the course of its participation as a JEDEC member, Rambus secretly pursued steps to confirm and enhance its patent rights over JEDEC standard technologies, while withholding from JEDEC any meaningful information concerning its intellectual property rights. (See, e.g. CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

December 1991 - JEDEC Committee Meeting

871. In December 1991 William Garrett was present for Rambus at the JEDEC JC-42.3 Committee meeting in Maui, Hawaii, participating as a non-member. (JX0010 at 2). Jim Townsend of Toshiba made a presentation concerning the JEDEC patent policy and showed the patent tracking list. (JX0010 at 11). Rambus was a guest at the invitation of Toshiba. (Rambus Answer at 20, ¶ 40).

872. Among the matters discussed at the December 1991 meeting were a variety of patent-related matters, including separate patent disclosures by IBM, DEC, Siemens, and TI; a response to patent-related questions by TI and Motorola; clarifications of patent licensing policies by Siemens and Hitachi; and expressions of patent-related concerns on proposals by Fujitsu and Samsung. (JX0010 at 3, 5, 8-11; G. Kelley, Tr. 2437-45). In particular, in response to an inquiry by Texas Instruments (TI), the purpose of the patent tracking list was explained as a means to track and identify patented items pertaining to Committee proposals. (*Id.*). Several members provided clarifications, updates or corrections pertaining to identified patents. (*Id.*; G. Kelley, Tr. 2438-39). Hitachi provided a written statement of its general policy to license its patents on reasonable and non-discriminatory terms. (JX0010 at 11, 139).

873. One specific area where patent issues arose at the December 1991 Committee meeting concerned a proposed standard for a packaging technology known as V-PACK. (JX10 at 8-9 (Items 329.1 and 329.2, JEDEC Ballot JC-42.3-91-66A); Williams, Tr. 779-782; CX2114 at 31 (Karp, Dep.)). The balloted proposal for incorporating VPACK as a JEDEC standard failed due to patent issues. (JX10 at 8-9; Williams, Tr. 781-782; CX2114 at 31).

874. Joel Karp, who at the time represented Samsung on the Committee, recalled that the patent holder, Texas Instruments (“TI”), offered to license at a 1% royalty. (CX2114 at 32; *see also* CX2078 at 139-140 (Karp, Dep.)). The 1% royalty rate is not referenced in the JEDEC

minutes, but is based on Mr. Karp's own recollection of the event. (CX2114 at 41). Mr. Mooring of Rambus recalls seeing a letter indicating TI was willing to license its patents on VPACK at a "reasonable royalty rate," in the one percent range. (CX2112 at 88 (Mooring, FTC Dep.)). Mr. Karp's experience, based on the V-PACK events, was that members of JEDEC balked at paying even a 1% royalty. (CX2078 at 139, 141-42).

875. Mr. Karp's handwritten notes from the December 1991 JEDEC meeting confirm that other manufacturers opposed the standardization of V-PACK because they did not want to pay royalties. (CX2080 at 228-229 (Karp, Dep.)). As Mr. Karp testified, "I think they [the DRAM producers] are saying they won't pay anything." (*Id.* at 229).

876. Mr. Garrett prepared a report of the December 1991 Committee meeting that he circulated to Rambus colleagues. (CX0670 at 1). The report stated that there were "several synchronous presentations" and outlined the important points of each. (*Id.*). Mr. Garrett specifically noted that both Howard Sussman and Texas Instruments proposed to use programmable CAS latency and programmable burst length. (CX0670 at 1 ("NEC2) Latency should be Programmable. (This would be accomplished with a WCBR cycle 1 51 Burst sequence and wrap length should be programmable TI - most important points ... Programmable WCBR cycle for Wrap or Burst note, length, sequence and clock Latency ... Their proposal seems to be well though[t] out."); see also Crisp, Tr. 3037-38 (Mr. Garrett's e-mail described CAS latency and programmable wrap length, which sometimes is used interchangeably with burst length)). Mr. Garrett's e-mail also noted that Mitsubishi proposed to use pins for wrap note and wrap type which would allow changes on the fly. (CX0670 at 1).

877. According to Mr. Garrett, all of the companies making proposals were currently working on their own solutions and were committed to meeting their customers' needs; the Committee was trying to get some agreement to reduce the proliferation of different parts. (*Id.*). Most proposals, he said, were incremental additions to existing DRAMs. (*Id.* at 2).

December 1991 - Rambus Applies for JEDEC Membership

878. Within days after returning from the December 1991 Committee meeting, Mr. Garrett submitted for Rambus an official membership application to JEDEC and paid the company's membership dues. (CX0602 at 2-3). On its membership application Mr. Garrett noted that Rambus "agree[d] to participate in the activities of" the JC-42.3 Committee, which was charged with overseeing the development of JEDEC Synchronous DRAM standards. (*Id.* at 3).

879. On January 12, 1992, Rambus CEO and President Tate circulated a draft business plan. The draft business plan made no mention of patent rights applicable to competing DRAM technologies. (CX0542). Several days later, handwritten notes from Rambus Vice President Allen Roberts' personal notebook suggest - discussion with "Richard" about creating a plan for

JEDEC. (CX1705 at 30 (“Board meeting ... JEDEC submission. Talk to Richard about creating a plan for JEDEC.”)).

February 1992 - JEDEC Committee Meeting

880. In February 1992 the JEDEC JC-42.3 Committee met in Seattle, Washington. (JX0012 at 1). The Chairman Mr. Townsend made a presentation concerning the patent policy and showed the patent tracking list. (JX0012 at 5, 28-29).

881. Among the matters discussed at the February 1992 meeting were several patent-related matters. (JX0012 at 5). These included clarifications by Texas Instruments (TI) concerning patents that it had previously disclosed to the Committee. (*Id.*). Siemens provided clarifications on several previously identified patents, and provided a written statement of its intent to license two specified patents on reasonable and non-discriminatory terms. (*Id.* at 5, 30).

882. Mr. Garrett prepared a detailed report of the discussions at the meeting for his Rambus colleagues that stated he was in attendance. (CX0672 at 1).

883. The first item that Mr. Garrett reported to his Rambus colleagues was a presentation by Fujitsu concerning a new generation of DRAMs; the presentation was reported by Mr. Garrett to be “particularly good and well thought of.” (CX0672 at 1). In connection with the presentation, Fujitsu discussed its intellectual property claims – specifically, its rights under pending patent applications: Mr. Garrett reported “Fujitsu indicated that they do have patents applied for, but that they will comply with the JEDEC requirements to make it a standard!!!” (*Id.*, emphasis in original).

884. In contrast to the statement made to JEDEC by Fujitsu, Mr. Garrett’s report noted to his colleagues the possibility that Rambus might be in a position to assert patent claims over aspects of JEDEC work on SDRAM standards. (CX0672 at 1 (Rambus “could influence the voltage standard if we want, or we could use our patents to keep current-mode interfaces off of DRAMs”)).

Spring 1992 - Rambus Consultations With Patent Counsel

885. By late 1991 Rambus was represented by an outside patent attorney, Lester Vincent, of the firm Blakely, Sokoloff, Taylor & Zafman, in connection with patent matters, including the preparation and revision of its patent applications. (*See, e.g.*, CX3125 at 279-80 (Vincent, Dep.); CX1932). Mr. Vincent’s work for Rambus over the years included patent prosecution and offensive and defensive work regarding patents. (CX3123 at 9 (Vincent, Dep.)).

886. In late 1991, prior to the March 1992 meeting between Mr. Vincent and Messrs. Roberts and Crisp, Mr. Crisp had consulted with Rambus concerning Rambus patent applications

and the use of “low swing signals on DRAM.” (CX1932; CX3125 at 279-80 (Vincent, Dep.)).

887. By March 1992, Rambus began to consult with Lester Vincent concerning JEDEC (CX3123 at 62 (Vincent, Dep.)). In a March 25, 1992, teleconference, Lester Vincent and Rambus Vice President of Engineering, Allen Roberts, discussed the possibility of Rambus asserting patents over SDRAMs, as well as the potential legal implications of such a strategy. (CX3125 at 296-98, 299-302 (Vincent, Dep.); CX1941 at 1). Among other things, Mr. Vincent’s handwritten notes record that the conversation concerned “Jedec” and the “need [for] pre planning before accuse others of infringement.” (CX1941 at 1). The notes contain the reference “Jedec Committee => Standards for DRAMs” and reflect discussion of “Advising JEDEC of patent applications.” (*Id.*). The notes state “Allen will get JEDEC bylaws re patents.” (*Id.*).

888. Two days later, on March 27, 1992, Mr. Vincent met with Rambus employees Allen Roberts and Richard Crisp and continued this discussion. (CX3125 at 310, 311-313 (Vincent, Dep.); CX1942). At this meeting Mr. Vincent was informed that Rambus was a member of JEDEC (CX3125 at 311-312 (Vincent, Dep.); CX1942 at 1) and that “Rambus attended [a] meeting with a hundred others where JEDEC’s proposal to establish [a] standard for small swing signals for sync DRAM was discussed.”(CX1942 at 1; CX3125 at 312-313 (Vincent, Dep.)).

889. The issue that Rambus wanted to talk about with Mr. Vincent in late March 1992 was whether attending JEDEC was a problem. Mr. Vincent warned that there could be an “equitable estoppel problem” in connection with the enforcement of Rambus patents if Rambus created an impression on JEDEC that it would not enforce its patents or patent applications. (CX3125 at 317-18 (Vincent, Dep.); CX1942 at 1). Mr. Crisp advised that the “strongest case of equitable estoppel is when you say you will not enforce your patent” and that the issue was “less clear-cut if Rambus is merely silent.” (*Id.*). He cautioned that Rambus “cannot mislead JEDEC into thinking that Rambus will not enforce its patent.” (*Id.*).

890. Mr. Crisp recalled that in this meeting Mr. Vincent advised Messrs. Roberts and Crisp that even if Rambus did go to JEDEC meetings, stayed silent and didn’t do anything else, there was still a risk that Rambus patents might be unenforceable. (CX2092 at 98 (Crisp, Infineon Trial Tr.)). Mr. Vincent was trying to tell Messrs. Roberts and Crisp that if Rambus insisted on going, the least it should do is don’t do anything to mislead anybody. (*Id.*).

891. In the same time period, Mr. Vincent advised Mr. Crisp and Mr. Roberts that he “didn’t think it was a good idea” for Rambus to continue participating in JEDEC, given the downside risk associated with potential equitable estoppel claims that might prevent enforcement of Rambus patents. (CX3125 at 320-21 (Vincent, Dep.)) (“Q. Did you tell Richard Crisp and Allen Roberts that at this March 27th, 1992, meeting, that they should not participate in JEDEC? . . . A. . . . I believe at some point early on . . . I believe I said I didn’t think it was a good idea”; “Q. The downside risk was that someone was going to raise the issue of equitable estoppel if Rambus attended JEDEC? A. Right. . . .”)).

892. In late March and early April 1992, Mr. Vincent conferred further with Rambus. A handwritten note of Mr. Vincent of a teleconference with Rambus CEO Geoffrey Tate on March 30, 1992, makes reference to “possible infringer” and obtaining copies of Rambus patent applications; the note states “we [sic] call me if he wants to go over the claim coverage.” (CX1943; CX1325 at 321-22 (Vincent, Dep.)). On April 1, 1992, Mr. Crisp asked Mr. Vincent to fax him abstracts of Rambus patent applications (CX1944; CX3125 at 322 (Vincent, Dep.)), which Mr. Vincent did several days later. (CX1945 at 1). Later in April, Mr. Vincent’s time records indicate he reviewed JEDEC publications. (CX3128 at 185-86 (Vincent, Dep.); CX1933 at 20).

April 1992 - JEDEC Task Group Meeting

893. In April 1992, Richard Crisp attended a JEDEC Synchronous DRAM Task Group meeting in Dallas, Texas. (Crisp, Tr. 2933-34; CX1708).

894. At the April 1992 task group meeting, Mr. Crisp learned that there was “a lot of momentum against” the RDRAM technology and that the group was “pretty set on using the SDRAMs for memory” in the new standard under consideration. (CX1708 at 3). He observed presentations involving a programmable mode register, including programmable burst length. (Crisp, Tr. 3054-55).

895. Mr. Crisp reported to Rambus colleagues that there was intense focus by JEDEC members on minimizing the costs associated with SDRAMs. (CX1708 at 1 (IBM “cited pricing as being the driving force.”); *id.* at 2 (“Compaq (Dave Wooton), like the others stressed that price was the major concern for all their systems.”); *id.* (“Sun echoed the concerns about low cost. They really hammered on that point.”)).

896. Mr. Crisp concluded that SDRAMs were likely to be significantly lower-priced items as compared to RDRAM devices. (CX1708 at 3). Mr. Crisp attributed this price difference, in large degree, to the fact that makers of RDRAMs would be forced to pay license fees and royalties to Rambus. (*Id.* (“it seems unlikely that we are going to be able to do better on price than the SDRAMs (license fees in need of recapture, royalties to be paid, bigger die size).”).

897. Mr. Crisp believed there was dissension among some JEDEC members at the meetings, and in the aftermath of the meeting suggested to Rambus colleagues that this be leaked to the press to the competitive advantage of Rambus. (Crisp, Tr. 2934-35; CX1708 at 5). In an email to colleagues, Mr. Crisp suggested a headline to be carried on trade publications EETimes and Nikkei Electronics. (CX1708 at 5 (“RIFT forms in JEDEC SDRAM working group: major system houses now leaning away from JC42 committee recommendation.”)). Mr. Crisp suggested specific trade press journalists who might be willing to help with the story. (*Id.*).

898. Mr. Crisp recognized that one downside of the idea was that the JEDEC discussions were confidential and a leak could lead to censure by JEDEC “if we weren’t tossed out.” (CX1708 at 5; see also CCF 830-31). But getting the story in industry publications “should help our air war.” (*Id.*). This referred to the desire of Rambus to have people use the proprietary RDRAM architecture. (Crisp, Tr. 2935).

899. Gordon Kelley of IBM wrote a letter to Ken McGhee of JEDEC following the April 1992 Committee meeting expressing concern with possible leaks to the press. (CX0035 at 16; G. Kelley, Tr. 2516-19). Mr. Kelley testified that Mr. Crisp’s suggestion that Rambus leak information from the April 1992 meeting was “an example of not having good faith or not showing good faith.” (G. Kelley, Tr. 2523-24).

Early May 1992 - Discussion With Patent Counsel

900. In early May 1992, within weeks after the April 1992 SDRAM Task Group meeting, Rambus was once again consulting with its outside patent counsel, Lester Vincent, concerning the possibility of asserting patent claims against the SDRAM standard under consideration. In his notes from a May 2, 1992, teleconference, Mr. Vincent wrote that “Richard Crisp wants to add claims to the original application” and referred specifically to “claims to mode register to control latency output timing depending upon clock cycle.” (CX1946 at 1).

901. Each of the items mentioned as those for which Mr. Crisp desired to add new patent claims had, by this point in time, been proposed for inclusion in the SDRAM specifications during JEDEC meetings attended by Mr. Garrett or Mr. Crisp. (CX0670 at 1 (Garrett email describing “the definition of synchronous DRAMs” as including the following, among other features: “Fully Synchronous DRAM with all signals referenced to a single (positive) clock edge. . . . Latency should be Programmable. . . . Burst sequence and wrap length should be programmable”)).

May 1992 - JEDEC meeting - Crisp declines to comment

902. In May 1992 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in New Orleans, Louisiana. (CX0034A at 1). The Chairman Mr. Townsend made a presentation concerning the patent policy and tracking list, and secretary Ken McGhee spoke concerning the EIA patent policies. (CX0034A at 4, 7).

903. By May of 1992 there were concerns by some members of the JC-42.3 Committee that a particular aspect of JEDEC’s work on SDRAM standards might implicate Rambus patents. Siemens and IBM, which had been working on a joint project relating to the development of next-generation memories, had noted similarities between SDRAM and the two-bank design used in proprietary RDRAM, and had learned of rumors that Rambus had demanded royalties from Samsung. (CX2088 at 317-319, CX2089 at 41-43 (Meyer, Infineon Trial Tr.); RX0286A at

2; RX0289 at 1).

904. During the May 1992 Committee meeting there was discussion that made reference to Motorola and Rambus as firms about which there were possible patent issues pertaining to the dual bank design. The Chairman Mr. Kelley of IBM, prompted by Willi Meyer of Siemens, asked Mr. Crisp whether he would like to comment on the issue. Mr. Crisp gave no verbal response, but rather shook his head. Mr. Kelley then commented to the group that “they don’t have anything to say about that.” (CX2089 at 130-131, 136-137 (Meyer, Infineon Trial Tr.)).

905. Mr. Crisp reported to his Rambus colleagues that at the May 1992 Committee meeting Siemens and Philips had expressed concern over potential Rambus patents covering two-bank designs. (CX0673 at 1). According to Mr. Crisp, “Gordon Kelley of IBM asked me if we would comment which I declined.” (*Id.*).

906. At the May 1992 Committee meeting, Howard Sussman of NEC commented to the group that he had seen a copy of a Rambus foreign patent application. (CX2092 at 128 (Crisp, Infineon Trial Tr.)). According to Mr. Crisp, the essence of the comment was that Mr. Sussman had obtained a copy of the application from the foreign patent office, had read it and it should not be a concern for the JEDEC standardization effort. (CX2092 at 129 (Crisp, Infineon Trial Tr.)). Mr. Crisp was there, heard the comment, and didn’t say anything different. (CX2092 at 130 (Crisp, Infineon Trial Tr.)).

907. The chairman of the meeting, Gordon Kelley, testified that prior to the May 1992 meeting Mr. Crisp had spoken to him about the possibility of Rambus scheduling a presentation concerning DRAM design. Concerned about the rumors of possible patent issues with Rambus, Mr. Kelley asked Mr. Crisp if he was aware if there were patents or patent issues relating to the possible presentation, and asked if Rambus agreed with the JEDEC policy on patent disclosure and licensing. Mr. Crisp told Mr. Kelley that he could not agree for Rambus on the policy for licensing; Mr. Kelley responded that if Rambus agreed with the patent policy, he could make a presentation. (G. Kelley, Tr. 2486-87). Mr. Kelley testified that Mr. Crisp never said anything that made Kelly believe that Rambus would not comply with the JEDEC patent disclosure policy. (G. Kelley, Tr. 2488-89).

908. At the May 1992 Committee meeting, after “lengthy discussion,” the Committee agreed to issue ballots on several items, including the SDRAM Truth Table and Test Mode Entry. (CX0034A at 3).

909. At the May 1992 Committee meeting Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Late May 1992 - Discussion With Patent Counsel

910. In late May 1992, Rambus patent counsel Lester Vincent communicated with Richard Crisp of Rambus concerning further proposed amendments to Rambus pending patent applications. (CX1947; CX3125 at 330-31 (Vincent, Dep.); Crisp, Tr. 3068-69). According to Mr. Vincent's notes, Mr. Roberts told him "Richard has claims for cases we have filed plus claims for divisionals," including adding claims to "mode register and control latency." (*Id.*).

Rambus June 1992 Business Plan

911. In June 1992, Rambus CEO Geoffrey Tate transmitted to the Rambus Board of Directors a comprehensive five-year business plan, which, he explained, was based on "inputs from all of the executives." (CX0543A at 1). The minutes of the Board's June 25, 1992 meeting reflect that this "5-Year Business Plan" was discussed. (CX0604 at 2).

912. As reflected in the "Executive Summary" of this June 1992 Business Plan, Rambus remained committed to:

- "establish[ing] strong intellectual property barriers";
- "establish[ing] Rambus as the new interface standard"; and
- "establish[ing] a very high profit stream of technology royalties."

(CX0543A at 3).

913. The June 1992 Business Plan reported that Rambus was making good progress in obtaining patents over its inventions. It reported that "Rambus Technology is currently covered by 18 [filed] patents, with over 300 claims, filed in the United States. Most of the patents have been or will be filed in other major countries in Europe and Asia." (CX0543A at 5). The Plan stated that the filed patents were "extensive and fundamental" and said that "[i]t is Rambus' opinion . . . that companies will not be able to develop Rambus-compatible technology or Rambus-like technology without infringing on multiple fundamental claims of the patents." (*Id.* at 9).

914. With respect to the key goals of establishing Rambus as the new interface standard and establishing a high profit stream of technology royalties (CX0543A at 3), the June 1992 Business Plan acknowledged that Rambus faced two principal impediments: "Resistance to Business Model" and "Competitive Solutions." (*Id.* at 14). Regarding the former, The Plan reported that some firms "have had a very negative reaction to our business model" including resistance to paying royalties to Rambus and fear that the royalties would make chips containing the Rambus technology "too expensive." (*Id.* (emphasis added)).

915. According to the 1992 Business Plan, the principal competitive threat to RDRAM

at this time continued to be JEDEC's emerging standards for "Synchronous DRAMs" which did not suffer from the same "price negative and risk negative associated with Rambus." (CX0543A at 17; see also *id.* at 16 ("many system customers perceive . . . that Sync DRAMs will be sourced more broadly and more quickly," and hence "will be much cheaper," than RDRAMs)).

916. The June 1992 Business Plan outlined multiple alternative strategies for responding to the competitive threat posed by Synchronous DRAMs. According to the Plan, "Our #1 strategy to counter Sync DRAMs is to get our parts proven and in the market." (CX0543A at 16). In addition, the Plan contemplated that Rambus would seek "to gain momentum rapidly in non-main-memory markets where Sync DRAMs are NOT an issue." (*Id.* at 17).

917. In addition to these strategies, the June 1992 Business Plan stated a patent-based strategy for attacking SDRAMs:

Finally, we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in a position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs.

(CX0543A at 17). The Plan referred to an "action plan" pursuant to which Rambus would identify and file additional patent claims and thereafter inform SDRAM manufacturers, all during 1992. (*Id.*) The disclosure portion of this action plan was not executed, however. During the time that Rambus was a member of JEDEC, its representative Mr. Crisp did not disclose any Rambus patent applications or patents to JEDEC, except for the '703 patent disclosed in September 1993. (Crisp, Tr. 3316, 3176).

918. The belief that Rambus had intellectual property claims to JEDEC SDRAM technology was widespread at Rambus. Vice-President Mooring could not recall any Rambus executive having a belief different than that expressed in the June 1992 business plan concerning Rambus patent coverage over SDRAM technology. (CX2079 at 155-56 (Mooring, Micron Dep.)) (Note; pending R objection] Former Rambus Chief Financial Officer Gary Harmon testified that from the time he started at Rambus in 1993, he heard "from various people that Rambus' patents were so fundamental and so broad that they likely covered technology that was being used by any other high-speed DRAM." (CX2070 at 97 (Harmon, Micron Dep.)). The source of this information was Mr. Tate, Mr. Mooring and others "who just gave the general impression that Rambus technology was broad." (CX2070 at 98 (Harmon, Micron Dep.)). This view extended to DDR when it was discussed in later years. (CX2070 at 100-01 (Harmon, Micron Dep.)).

919. On June 11, 1992, the JC-42.3 Committee issued a series of four ballots. (CX252A; CX253; CX254). One of the four ballots, item 3763, proposed to include with the SDRAM

standard a programmable mode register incorporating programmable CAS latency and burst length. (CX0252A at 3; Crisp, Tr. 3075-76; Rhoden, Tr. 448; Williams, Tr. 811-812; Sussman, Tr. 1390-1391)). The ballot directed: "If anyone receiving this ballot is aware of patents involving this ballot, please alert the Committee accordingly during your voting response. (CX252A at 2).

920. On June 22, 1992, Mr. Crisp spoke to Mr. Lester Vincent regarding pending Rambus divisional patent applications. (CX3125 at 332-33 (Vincent Dep.); Crisp, Tr. 3076-79). Mr. Crisp wanted to file a preliminary amendment soon, but Mr. Vincent recommended waiting a few months because Rambus was not losing any rights. (CX3130 at 81-82 (Vincent, Dep.)).

July 1992 - Committee Meeting and Vote on Elements of the SDRAM Standard

921. In July 1992 Richard Crisp and David Mooring were present for Rambus at the JEDEC JC-42.3 Committee meeting in Denver, Colorado. (JX0013 at 1-2). The Chairman Mr. Townsend showed the patent policy and tracking list. (JX0013 at 4).

922. At the July 1992 meeting, the Committee tabulated and discussed the results of the four ballots that had been approved at the June 1992 meeting of the Committee. (JX0013 at 9-10). The proposals that had been circulated for a vote included one concerning the use of a mode register for programming CAS latency. (JX0013 at 10).

923. The proposals carried by more than the two-thirds required by the Committee rules. (JX0013 at 9-10; Rhoden, Tr. 451-52). Pursuant to the established procedures of the Committee, comments were made by members concerning the proposals and addressed in open discussion by the Committee. (JX0013 at 9-10; Rhoden, Tr. 452).

924. Among the matters discussed at the July 1992 Committee meeting were concerns by IBM over patent issues. (JX0013 at 9 ("Patent issues must be cleaned up before we proceed.")). During the meeting the Motorola representative received a letter from the company legal staff concerning a Motorola patent; the letter was shown by the Committee chairman and accepted by the Committee as complying with the JEDEC patent policy. (*Id.* at 9, 136).

925. Richard Crisp was present at the July 1992 meeting of the Committee and participated for Rambus in the discussion and the vote on the proposals, including the mode register proposal. (JX0013 at 1, 9-10). David Mooring of Rambus also was present. (JX0013 at 2). Rambus voted "no" to the proposals. (*Id.* at 9-10; CX2112 at 78-79 (Mooring, Dep.)).

926. Mr. Mooring, who was present for Rambus at this Committee meeting, was aware as of early 1991 that programmable CAS latency and programmable burst length either surely or likely were Rambus inventions. (CX2054 at 84-85 (Mooring, Infineon Dep.)) Mr. Mooring recalled that in the 1992-93 time period there was "some belief we [Rambus] actually had patent

applications on SDRAM.” (CX2054 at 89-90 (Mooring, Infineon Dep.)). Rambus CEO Tate and Richard Crisp were individuals within Rambus who held or professed such beliefs. (CX2056 at 252 (Mooring, Infineon Dep.)).

927. Mr. Crisp cast the vote for Rambus and made technical comments concerning the proposals, but despite the discussion of patent issues at the meeting did not say anything concerning Rambus patents or patent applications. (Crisp, Tr. 3082-84, 3087; Rhoden, Tr. 453-54; Williams, Tr. 816-20; (CX2056 at 236, CX2112 at 78 (Mooring, Dep.)). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

August 1992 - Conference with Patent Counsel

928. Rambus patent counsel Lester Vincent conferred by telephone with Richard Crisp in late August 1992 concerning amendment of Rambus patent claims. (CX3130 at 99-100 (Vincent, Dep.); CX1930 at 42).

September 1992 - Committee Meeting

929. In September 1992 Richard Crisp and Billy Garrett were present for Rambus at the JEDEC JC-42.3 Committee meeting in Crystal City, Virginia. (CX0042A at 1; Crisp, Tr. 3093-3096). The Chairman Mr. Townsend reported on the patent policies and showed the patent tracking list. (CX0042A at 2).

930. Mr. Garrett and Mr. Crisp reported to senior executives of Rambus, including CEO Tate, Vice-President Roberts and board member Farmwald, concerning the matters under discussion at the meeting; among the matters discussed and reported were the inclusion of programmable CAS latency and programmable burst length in the SDRAM standard under discussion by the Committee. (CX0680 at 1, 2; Crisp, Tr. 3094-95).

931. Notwithstanding these discussions at the September 1992 meeting of the Committee, Mr. Crisp did not inform the Committee in September 1992 of the Rambus efforts to seek claims in its patent applications pertaining to SDRAM features. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

September 1992 - Conference With Patent Counsel

932. In September 1992, approximately a week after the JEDEC Committee meeting, Mr. Crisp had a face-to-face meeting with Lester Vincent about further pursuit of divisional patent applications on behalf of Rambus. (CX1949).

933. Mr. Vincent's notes of his September 1992 meeting with Mr. Crisp reflect detailed discussion of a number of additional areas suggested by Mr. Crisp for coverage under patent claims by Rambus; these included programmable CAS latency, multiple open rows (or banks), source synchronous clocking and other concepts that had been under discussion at the most recent and past JEDEC meetings and reported to Rambus management by Messrs. Crisp and Garrett. (Crisp, Tr. 3097-3105; CX1949 at 1,2,5,7; CX3125 at 337-38, 338-340, 348-49 (Vincent, Dep.)). Mr. Vincent's notes make specific reference to "caus[ing] problems with Sync DRAM" and "SDRAM stuff worried about." (CX1949 at 1, 7; CX3125 at 339, 349 (Vincent, Dep.)).

934. Mr Vincent's notes of his September 1992 meeting with Mr. Crisp indicate, with respect to access time, that a broad independent claim was desired. (CX1949 at 2 ("make Indep. Claim => broad")) (emphasis in original); CX3128 at 235-36 (Vincent, Dep.)).

935. Mr. Vincent's notes of his September 1992 meeting with Mr. Crisp reflect a desire to include claims covering use of phase lock loops, or PLLs, on DRAMs, (CX1949 at 1, 5, 7; CX3125 at 338-40, 345, 346-47 (Vincent, Dep.)). Mr. Vincent's notes indicate, with respect to PLLs on DRAMs, that they wanted to cover the concept of using PLLs or DRAMs, not just specific PLL circuits. (CX1949 at 5 ("=> many different ways of designing PLL – want to cover concept of deskewing input"); *id.* at 7 ("=> claim usage of such circuit on a DRAM – not particular PLL")) (emphasis in original); CX3125 at 346-47 (Vincent, Dep.)).

936. Mr. Vincent's notes of his September 1992 meeting with Mr. Crisp discuss including coverage of packet-oriented commands. (CX1949 at 1 ("DRAM-packet oriented comm."); *id.* at 4 ("=>Rambus=> wants to claim memory device that receives commands via packets"); CX3125 at 338-40 (Vincent Dep.)). Mr. Vincent's notes state "so cause problems w/ . . . Ramlink," and "Richard => will get me copy of the Ramlink spec." (CX1949 at 4; CX3125 at 342, 343 (Vincent, Dep.)).

September 1992 - Rambus Business Plan

937. In September 1992, Rambus CEO and President Geoffrey Tate circulated a revised business plan. (CX0545; CX2061 at 229 (Tate, Dep.)). That document stated: "Sync DRAMs infringe claims of Rambus filed patents and other claims that Rambus will file in updates later in 1992." (CX0545 at 21).

October 1992 - Rambus Board Briefing

938. In October 1992 Mr. Crisp and Mr. Mooring made presentations to the Rambus Board of Directors concerning among other things the status of SDRAM activity at JEDEC and the Rambus patent strategy. (CX0606 at 2; Crisp, Tr. 3108-09). Mr. Crisp made a presentation to the board concerning the status of SDRAM at JEDEC, and thereafter told the Board that

Rambus was making efforts to broaden the Rambus patent applications to cover SDRAMs. (CX2092 at 162-63 (Crisp, Infineon Trial Tr.); CX2082 at 752 (Crisp, Dep.)). The issue of whether Rambus patents cover JEDEC standards was discussed at a Rambus Board meeting in 1992. (CX2054 at 62 (Mooring, Dep.)).

November 1992 - Conference with Patent Counsel

939. In November 1992, after first informing CEO Tate and Vice-President Roberts, Richard Crisp and Michael Farmwald of Rambus met with Mr. Vincent, the Rambus patent counsel, to discuss Rambus patent claims. (CX682; CX1930 at 59; CX3130 at 107-08 (Vincent, Dep.); Crisp, Tr. 3109-11). The purpose of the meeting was to discuss claims to be added to Rambus patent applications (CX682); the topics discussed included multiple row addresses and synchronization (CX1930 at 59). The concept of multiple row addresses was broad enough to embrace the two bank design feature that had been discussed at JEDEC in connection with the SDRAM standard. (Crisp, Tr. 3097-98, 3110).

December 1992 - Committee Meeting

940. In December 1992 Richard Crisp and David Mooring were present for Rambus at the JEDEC JC-42.3 Committee meeting in Fort Lauderdale, Florida. (JX0014; CX0042A at 1-2; Crisp, Tr. 3113-14).

941. Mr. Mooring reported to various Rambus executives, including CEO Tate, that views on the on the SDRAM features had “almost consolidated,” and predicted that consensus on the standard would be reached by March 1993. (CX0685 at 1; CX2055 at 103 (Mooring, Dep.)). Mr. Mooring also reported that, at the December 1992 meeting, IBM had stated that it was aware that some voting attendees at the Committee meetings had “patents pending on SDRAMs” that they had not made the Committee aware of. (*Id.*) Mr. Mooring’s report reflects his recollection of the JEDEC meeting from the following day; he was merely reporting what IBM had said at the meeting. (CX2112 at 105, CX2055 at 100 (Mooring, Dep.)).

942. During the course of the December 1992 meeting, Committee chairman Jim Townsend made a presentation concerning the EIA patent policy and draft revisions to the JEDEC manual pertaining to the patent policy. (JX0014 at 3, 25; Crisp, Tr. 2984-86). Among other things, the language contained in the presentation materials stated that the patent policy applied to situations involving the discovery of patents that may be required for the use of a patent subsequent to its adoption. (JX0014 at 21). The presentation materials also made repeated reference to the need to make disclosure of “patented or patentable items,” and stated that the term “patented” also included “pending patents on items and processes under consideration.” (JX0014 at 25; Crisp, Tr. 2986-88).

943. These revisions were later embodied in the next version of the JEDEC manual.

(CX208A at 19).

944. Notwithstanding these discussions at the December 1992 meeting of the Committee, Mr. Crisp did not inform the Committee in December 1992 of the Rambus efforts to seek claims in its patent applications pertaining to SDRAM features. (Crisp, Tr. 3316).

945. An internal Rambus document entitled “Architectural Issues” and dated approximately one week after the December 1992 Committee meeting among other things states a plan to “get a copy of the SDRAM spec and check it for features we need to cover as well as features which violate our patents.” (CX1821 at 24).

February 1993 - Work on Rambus Patent Applications

946. In February 1993, Rambus CEO and President Geoffrey Tate sent an email to all Rambus staff noting that NEC, Toshiba, Fujitsu, Hitachi, Mitsubishi and Micron all had announced that in the second half of 1993 they would introduce samples of synchronous DRAMs that lined up with the anticipated JEDEC standard. (CX0688).

947. In early 1993 Rambus employee Fred Ware began to work with Rambus patent counsel Mr. Vincent in connection with the Rambus pending patent applications. Mr. Ware was an engineer in the “architecture group” inside Rambus and was in a reporting chain that reported to Vice-President Allen Roberts. (Crisp, Tr. 3119-20).

948. In February 1993 Mr. Ware asked Mr. Crisp for a list of claims under consideration for addition to the original Rambus patent. (CX0686). Mr. Crisp’s email response identified several items, including “DRAM with programmable access latency,” a broad concept that included programmable CAS latency as discussed earlier at JEDEC. (CX0686; Crisp, Tr. 3121-22). Mr. Crisp also identified “DRAM with multiple open rows,” a technology related to but broader than the two bank feature discussed within JEDEC. (CX0686, Crisp, Tr. 3122). Mr. Crisp also identified “DRAM using PLL/DLL circuit to reduce input buffer skews.” (CX0686; Crisp, Tr. 3122). In a follow-on communication a few days later Mr. Crisp also identified external reference voltage, a technology similar if not the same as had been discussed at JEDEC; his response to Mr. Ware indicated that adding such a claim to Rambus’s patent protection “should help confound the . . . effort” to develop industry standard technology. (CX691; Crisp, Tr. 3123-24).

949. By February 1993, Rambus was aware that major DRAM manufacturers had announced their intention to line up with the JEDEC SDRAM standard under development. CEO Tate sent an email to Rambus staff that made reference to press reports indicating that NEC, Toshiba, Fujitsu, Mitsubishi and Micron had all indicated their intention to align themselves with the JEDEC standard. (CX0688; Crisp, Tr. 3125-26).

March 1993 - JEDEC Committee Meeting

950. In March 1993 William (“Billy”) Garrett was present for Rambus at the JEDEC JC-42.3 Committee meeting in Scottsdale, Arizona. (JX0015 at 2). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list, and there was discussion by members concerning patent issues. (JX0015 at 4).

951. Among the patent matters discussed at the March 1993 Committee meeting was an inquiry made to IBM concerning whether IBM would disclose to the Committee all patents and patent applications held by the company worldwide. (G. Kelley, Tr. 2449-50; JX0015 at 6). Because of the breadth and difficulty of the company-wide search that would be required for such a listing, there was a risk that any such listing would be incomplete and misleading, and so IBM stated that it would not undertake such a listing. (G. Kelley, Tr. 2450-51). However, the IBM representative did assure the Committee that he would alert the group to any patent information known to him, and would provide a response to any patent question raised by Committee members. (G. Kelley, Tr. 2451-52).

952. At the March 1993 meeting, the Committee passed the last of the ballots that made up the SDRAM standard, and approved the issuance of a press release announcing that the Committee had approved the SDRAM standard. (JX0015 at 14, 99).

953. Notwithstanding these developments at the March 1993 meeting of the Committee, Mr. Garrett did not inform the Committee in March 1993 of the Rambus efforts to seek claims in its patent applications pertaining to SDRAM features. (CCFF 863-65).

April 1993 - Rambus Renews Its JEDEC Membership

954. In April 1993 Rambus paid its dues to renew its JEDEC membership for the 1993 calendar year. (CX602 at 11; Stipulation, Tr. 3143-44).

April-May 1993 - Consultations with Patent Counsel and Pursuit of Claims

955. In late April 1993 Lester Vincent, patent counsel for Rambus, sent to Messrs. Farmwald, Roberts and Crisp of Rambus proposed preliminary amendments to pending Rambus patent applications. (CX1957; CX1457; Crisp, Tr. 3145-48).

956. On May 4, 1993, Mr. Lester Vincent apparently sent Mr. Crisp a presentation regarding industry standards that said, “Two possible legal theories for non-enforcement [of patents]: 1) Estoppel? 2) Antitrust?” (CX1958 at 12). Mr. Vincent thought that Mr. Crisp might be interested in the presentation handout because of Mr. Vincent’s March 1992 meeting in which he discussed the issue of equitable estoppel with Mr. Crisp and Mr. Roberts of Rambus. (CX3126 at 397 (Vincent, Dep.)). The materials included as pages 2-22 of CX1958 were

produced from Mr. Vincent's files and are the only presentation relating to industry standards that were found in his files. (CX3126 at 396-97, CX3128 at 255-56 (Vincent, Dep.)).

957. The presentation summarized the Stambler v. Diebold decision as specific example of equitable estoppel as a defense to a claim of patent infringement. (CX1958 at 15, 16 (“Plaintiff could not remain silent while an entire industry implemented the proposed standard and then when the standards were adopted assert that his patents covered what manufacturers believed to be an open and available standard.” (quoting Stambler v. Diebold, 11 USPO 2d 1709, 1715 (E.D.N.Y. 1988), aff’d, 11 USPO 2d 1715 (Fed. Cir. 1989))).

958. On May 13, 1993, Mr. Vincent conferred with Messrs. Farmwald and Crisp concerning the draft amendments to Rambus pending patent applications that were sent to Rambus in April. (CX1930 at 83). On May 17, Mr. Vincent's firm filed the preliminary amendments with the Patent and Trademark Office. (CX1458; CX3129 at 412-14 (Vincent, Dep.)). One of the preliminary amendments filed on May 17 added language to the pending Rambus '651 patent application describing a claim for programmable CAS latency. (CX1458 at 5 (claim 151(D), adding claim for circuitry “for storing a value corresponding to a predetermined time period during which the interfacing circuitry must wait before transmitting reply information”). Mr. Crisp and others at Rambus understood the amendment to the '651 application to be “directed against SDRAMs.” (CX0702; CX1959; CX0703; Crisp, Tr. 3153-57).

May 1993 - JEDEC Committee Meeting

959. On May 19-20, 1993, Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Chicago, Illinois. (JX0016 at 1; Crisp, Tr. 3158). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list, and there was discussion by members concerning patent issues. (JX0016 at 5).

960. At the May 19-20, 1993, JEDEC JC42.3 Committee meeting Gordon Kelley gave a report on the status of the packet of fourteen SDRAM ballots that had been sent to the JEDEC council. Mr. Kelley announced that there was only one no vote, from AT&T, and distributed copies of the SDRAM ballots. (JX0016 at 5). Mr. Crisp informed Rambus management by email from the meeting that the SDRAM standard was likely to be adopted at the next JEDEC council meeting. (CX0700 at 1). Rambus CEO Tate responded by asking Mr. Crisp to brief him and other members of management when Mr. Crisp returned. (CX0711 at 8 (“Sounds like lots of interesting activities - please arrange to debrief me, Allen [Roberts]. Dave [Mooring] when you are back and Mike [Farmwald] if he's interested.”)).

961. At the meeting Mr. Crisp did not make any disclosure of any Rambus patent or patent application that might relate to these SDRAM ballots. (Crisp, Tr. 3160-61). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM

standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

June 1993 - Rambus Patent Activity

962. In June 1993, Fred Ware of Rambus sent an email to various Rambus employees, including Messrs. Farmwald, Roberts and Crisp, reporting on a conversation with Mr. Vincent and the “current status of the additional claims we wanted to file on the original . . . patent.” (CX1959; see also CX3130 at 129 (Vincent, Dep.)). Mr. Ware reported that a claim pertaining to “writable configuration register permitting programmable CAS latency” had been “written up and filed” and remarked that the claim was “directed against SDRAMs.” (CX1959).

963. Mr. Ware also identified several other patent claims that were being written up or considered by Mr. Vincent but had not yet been filed. These included a claim for “DRAM with PLL clock generation” that was “directed against future SDRAMs,” and a claim for “DRAM with multiple open rows” that was “directed against SDRAMs.” (CX1959). Mr. Ware also identified claims relating to DRAM, with externally supplied reference voltage and DRAMs using low-voltage-swing signal levels. He described these claims as directed against CTT technology and GTL technology respectively. (CX1959).

964. A reply email from Mr. Crisp the same day stated that the claims for low voltage swing signals already had been done. He otherwise confirmed the accuracy of Mr. Ware’s report. (CX703; Crisp, Tr. 3156-57, 3163; CX2082 at 772-74 (Crisp, Dep.); CX2092 at 189-93 (Crisp, Infineon Trial Tr.)).

965. On June 20, 1993, Mr. Vincent filed an amendment to an existing Rambus patent application seeking to add a claim for externally supplied reference voltage, another topic that had been discussed at JEDEC. (Crisp, Tr. 3164-3171; CX1959; CX1459; CX1961; CX1963 at 4).

966. On June 28, 1993, Mr. Vincent’s firm filed on behalf of Rambus an amendment that cancelled the claims in the pending Rambus patent application 07/847,692 (the ‘692 application) and inserted new claims. (CX1502 at 208, 212). The new claims contained in this amendment included claims pertaining to the use of on-chip PLL circuitry. (CX1502 at 204, 208 (claim 151); Nusbaum, Tr. 1583-85; Jacob, Tr. 5533-41; CCF 1103 et seq.).

967. Two days later, on June 30, 1993, Mr. Vincent sent Mr. Crisp a copy of the preliminary amendment to the ‘692 application. (CX1961). On July 9, 1993, Mr. Vincent met with Mr. Crisp and Mr. Ware and discussed, among other topics, claims relating to low voltage swing signals and externally supplied reference voltage. (CX1963 at 3,4; CX3126 at 447-48, 449-52 (Vincent, Dep.)).

September 1993 - JEDEC Committee Meeting & Disclosure of ‘703 Patent

968. In September 1993 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Boston, Massachusetts. (JX0017 at 1; Crisp, Tr. 3171-73). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0017 at 3). Mr. Townsend also showed a draft of portions of the revised 21-I Manual (JX0017 at 12 (“Standards that call for the use of a patented item or process may not be considered by a JEDEC committee unless all of the relevant technical information covered by the patent or pending patent is known to the committee, subcommittee or working group”) (emphasis added); *id.* at 14 (regarding discussion of “pending or existing patents” and applicability of patent policy after adoption of a standard); see also CX2092 at 63-64 (Crisp, Infineon Trial Tr.)).

969. At the September 1993 Committee meeting there was discussion concerning the discovery by Committee members that Texas Instruments (TI) had a patent covering so-called Quad CAS technology. (JX0017 at 6; Crisp, Tr. 2960-62). Mr. Crisp reported to Rambus CEO Tate and Vice-President Mooring that at the meeting “TI was chastized [sic] for not informing JEDEC that it had a 1987 patent on Quad CAS devices” and reported that the Committee had determined to remove Quad CAS technology from the pertinent JEDEC standard. (CX0711 at 1 (“The bottom line is that all Quad CAS devices will be removed from standard 21C.”)). Tempers flared at the meeting, and Mr. Crisp believed that the action was a way that the group sent a strong message to TI that they did not appreciate what TI had done. (CX2086 at 165, 168 (Crisp, Dep.)).

970. About three weeks after the September 1993 Committee meeting, Mr. Crisp requested that Mr. Vincent obtain copies of six TI patents as well as copies of the complaints in pending litigation between TI and Micron in Texas and Idaho. (CX1967; Crisp, Tr. 2963-64; CX1955 at 46; *see also* CX1971 at 1).

971. At the September 1993 meeting of the Committee Mr. Crisp disclosed to the Committee the issuance to Rambus on September 7, 1993, of United States Patent Number 5,243,703. (CX1460; Crisp, Tr. 3173; Stipulation No. 11). The ‘703 patent was the first Rambus patent and had issued shortly before the meeting. *Id.* The ‘703 patent resulted from a divisional application of an original application, Serial No. 07/510,898 (‘898 application), filed in April 1990. (First Stipulations, No. 11).

972. The ‘703 patent asserted claims over a U-shaped or reflected clock technology; neither the claims or the specification of the ‘703 patent would have alerted an engineer at the time it was issued that Rambus might seek to obtain patent rights over features contained the JEDEC SDRAM standard. (CX1460; Jacob, Tr. 5498-5501). The claims of the ‘703 patent did not read on anything other than Rambus-compatible devices. (CX2102 at 321 (Karp, Dep.)).

973. Mr. Crisp did not provide any information about the subject matter of the ‘703 patent or how, if at all, it related to JEDEC work. (CX2087 at 248-49 (Crisp, Dep.)). The ‘703 patent was unrelated to ongoing JEDEC work. (CX2092 at 197-99 (Crisp, Infineon Trial Tr.));

CX1801 at 3 (“The ‘703 patent and the WIPO application did not relate to JEDEC’s SDRAM work, but were directed to the implementation of Rambus’ RDRAM products.”)).

974. At the September 1993 meeting of the Committee, Mr. Crisp did not say anything about any of the pending patent applications of Rambus. (Crisp, Tr. 3174). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

975. David Mooring, who was Mr. Crisp's supervisor at the time, gave Mr. Crisp the impression that he was “annoyed” when he learned about the disclosure of the ‘703 patent at JEDEC. (Crisp, Tr. 3174-75; CX2054 at 189-90 (Mooring, Dep.)). In an email two years later, Mr. Crisp recalled that he had been “castigated” for disclosing the ‘703 patent to JEDEC. (CX0837 at 2; Crisp, Tr. 3175 (“chastised”)).

976. Except for the ‘703 patent, Mr. Crisp did not disclose any Rambus patent applications or patents to JEDEC during the time he was a member. (Crisp, Tr. 3316, 3176).

November 1993 - JEDEC publishes SDRAM standard

977. JEDEC published its standard for SDRAM as part of Release 4 of JEDEC Standard 21-C in November 1993. (First Stipulations, No. 19). Since 1993, JEDEC has published several revisions of the JEDEC standard governing SDRAMs, JEDEC Standard 21-C. (First Stipulations, No. 20).

December 1993 - JEDEC Committee Meeting

978. In December 1993 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in San Diego, California. (JX0018 at 1). The Chairman Mr. Townsend presented the patent policies and the patent tracking list was updated. (JX0018 at 3, 15-18).

979. At the December 1993 Committee meeting, the Committee considered and voted to adopt a ballot to rescind previously-approved portions of JEDEC standards pertaining to Quad CAS, in light of the patent issues that had been discussed at the September 1993 Committee meeting. (JX0018 at 7; G. Kelley, Tr. 2467-69). The Committee, after discussion, voted to send the ballot to rescind the previously-approved portions of the standards to the JEDEC Council. (JX0018 at 9).

980. At the December 1993 Committee meeting Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

January 1994 - Consultation With Rambus Patent Counsel

981. On January 10, 1994, Mr. Vincent met with Rambus CEO Tate, CFO Gary Harmon and Vice-President Roberts to discuss enforcement of Rambus patents against synchronous DRAM, with particular reference to low voltage swing, configurable mode register (including programmable CAS latency) and on-chip PLLs. (CX1970 at 1 (“Enforcement: Sink DRAM, . . . low swing signals . . . config registers . . . programmable latency . . . PLLs”); CX3126 at 461-62, 463-65 (Vincent, Dep.)). Mr. Vincent noted that there were five Fred Ware applications, and he needed to file all five. (CX1970 at 2).

February 1994 - Rambus Renews Its JEDEC Membership

982. In February 1994 Rambus renewed its JEDEC membership for the 1994 calendar year, increasing its dues to reflect participation in an additional JEDEC committee. (CX0602 at 7; Stipulation, Tr. 3176; Crisp, Tr. 3176).

March 1994 - JEDEC Committee Meeting

983. In March 1994 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Orlando, Florida. (JX0019 at 1). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0019 at 4).

984. Among the patent issues discussed at the March 1994 Committee meeting was the disclosure by Philips of two patents, and its statement of willingness to license on reasonable and non-discriminatory terms. (JX0019 at 25). Micron and TI also disclosed several patents at the meeting. (CX0711 at 16-17).

985. At the March 1994 Committee meeting there was extensive discussion among Committee members concerning the continuing Quad CAS controversy and the patent disclosure policy. (JX0019 at 4-5). Mr. Crisp reported to his Rambus colleagues that “the meeting opened with a lot of controversy regarding patents” having to do with the ongoing lawsuit in which TI and Micron were “embroiled.” (CX0711 at 16). Mr. Crisp reported to his colleagues that TI sought to have the Committee interpret the disclosure duty as “limited” to two scenarios. (*Id.*) He also reported Micron’s statement that the JEDEC patent policy existed “due to anti-trust concerns” so that companies could not keep out competition. (*Id.*) Mr. Crisp reported that discussion on this and other related topics “got pretty nasty and was finally squelched” by the Chairman who asked successfully for a motion to cut off discussion. (*Id.*). At the close of the discussion on this topic, those present in the room were asked to indicate by hand vote whether there was any confusion on the basic patent policy – the need and obligation to disclose patent activity. By unanimous vote, the Committee confirmed that the patent policy was clear. (Kellogg, Tr. 5028-30; JX0019 at 4-5 (“The Committee was asked if the policy is clear. The Committee felt it was clear.”)).

986. Despite the various discussions pertaining to patent disclosure at the March 1994 Committee meeting, Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

March-May 1994 - More Rambus Patent Strategy

987. On March 15, 1994, Rambus Vice President David Mooring proposed to CEO Geoff Tate, Vice-President Allen Roberts and CFO Gary Harmon that Rambus “kick-off another patenting spree.” (CX0726). Mr. Mooring noted that Rambus still had “a window of opportunity left while we still have confidential information.” (*Id.*) He suggested that it would help the Rambus scenario against competitive memories such as RamLink and SyncLink if they had patents that would be infringed by memory controllers produced by companies such as ATI. (*Id.*)

988. On April 29, 1994, Rambus Vice-President Roberts requested a meeting with Rambus employees Fred Ware, Rick Barth and John Dillon to discuss “what new claims for our existing patents we dream up which might block MOST.” (CX0730). One idea that Mr. Roberts proposed was “clocking data on moth edges of the clock on a DRAM.” (*Id.*).

989. In May 1994, Allen Roberts, Rambus Vice-President of Engineering, sent a letter to Rambus patent counsel Lester Vincent further discussing enhancements to the coverage of the original Rambus patent application and identifying various ideas to be pursued as claims in the various pending patent applications or in newly filed applications. The letter stated that “it is possible that some of these enhancements are already in the existing applications, but we would like to re-assess the strength of those claims.” (CX0734).

990. Among the enhancements described in the May 1994 letter were “[m]ultiple and independently controlled and addressed DRAM memory regions (banks).” (CX0734). Two bank design had previously been discussed on multiple occasions at JEDEC. (Crisp, Tr. 3180).

991. Among the enhancements described in the May 1994 letter was “[u]se [of] control registers to contain values which control RAS or CAS access timing.” (CX0734 at 2). Use of control registers to enable programmable CAS latency had previously been discussed on multiple occasions at JEDEC. (Crisp, Tr. 3181-82).

992. Among the enhancements described in the May 1994 letter was “[u]se of both edges of the clock for transmission of address, commands or data (or any combination) on DRAM device to increase effective bandwidth/pin.” (CX0734 at 1).

993. In July 1994 Mr. Roberts apparently informed Rambus CEO Tate that

(CX1715 at 56 (*in camera*) (

)).

May 1994 - Clarification of JEDEC Patent Policy

994. In May 1994, the secretary of the JEDEC Council distributed to all members of JC-42 Committees copies of a memorandum prepared by John Kelly, the JEDEC legal counsel. (CX0355 at 1). The memorandum had been prepared by Mr. Kelly in response to a white paper that had been submitted to the JEDEC council in March 1994 by TI in connection with the ongoing dispute concerning Quad CAS technology arising from the work of the JEDEC JC42.3 Committee. (J. Kelly, Tr. 1940-41; CX0353 at 2-5).

995. In the memorandum, Mr. Kelly, who was responsible for interpreting JEDEC rules (J. Kelly, Tr. 1821-22), clarified the JEDEC patent policy and rejected an interpretation that had been argued by TI in its white paper submitted to the JEDEC Council. (J. Kelly, Tr. 1942-47). In the memorandum, Mr. Kelly made clear that under the JEDEC patent disclosure policy written assurances with respect to patent licensing must be provided by a patent holder where a standard under consideration “may require” the use of a patented invention. (CX0355 at 2). The memorandum contradicted the position of TI, which was that no assurances were required unless it was absolutely clear that use of the patent was required to comply with the standard. (J. Kelly, Tr. 1943-44). Consistent with longstanding practice, the use of the term “patented” in the memo referred to either patents or patent applications. (J. Kelly, Tr. 1945-46).

May 1994 - JEDEC Committee Meeting

996. In May 1994 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in New York City. (JX0020 at 1; Crisp, Tr. 3188). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0020 at 4, 15-18).

997. During the course of the May 1994 meeting Mr. Crisp prepared a lengthy email to colleagues at Rambus reporting and commenting on the discussions occurring at the meeting. (Crisp, Tr. 3193-94; CX711 at 26-30). In the text of the email, Mr. Crisp noted that one of the topics addressed in the discussions was the use of externally-supplied reference voltage in later-generation SDRAM design. (CX711 at 27, 31). His comments (including one directed to Rambus Vice-President Allen Roberts) made reference to this technology as one that Rambus had been pursuing through patent filings by Rambus patent attorney at its request. (*Id.*; see also Crisp, Tr. 3193-94). Mr. Crisp commented that “we may be able to slow down or stop (or at least collect from) [devices embodying the technology] if the claim is allowed..” (CX711 at 31).

998. In fact, the topic of external reference voltage had been discussed by the Committee and noted by Rambus representative Billy Garrett as early as February 1992. (CX672 at 1; Crisp,

Tr. 3042-44). In February 1993 Richard Crisp had sent an email to other Rambus executives discussing pursuit of a patent claim relating to external reference voltage. (CX691; Crisp, Tr. 3123-24).

999. Mr. Crisp did not inform the Committee that he had worked on a patent claim relating to externally supplied reference voltage, or that Rambus might be able to slow down or stop or at least collect royalties from various devices relating to externally supplied reference voltage if the claim was allowed. (Crisp, Tr. 3194). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

June 1994 - Internal Rambus Communication

1000. On June 16, 1994, John Dillon, the head of the architecture group inside Rambus and Rambus representative at the JEDEC JC 15 Committee (CX0602 at 5), sent an email to various other Rambus executives, including CEO Geoffrey Tate, Vice-President David Mooring, Vice-President Allen Roberts and Fred Ware. (CX0738; Crisp, Tr. 3185-86). The email was entitled “an overlooked patent claim?” and discussed the “auto-precharge feature.” (CX0738).

1001. The auto-precharge feature had previously been discussed at JEDEC on at least two occasions in 1992 in connection with the SDRAM standard. (CX1708 at 5; CX0680 at 2; Crisp, Tr. 3183-85). Auto-precharge had been incorporated as a feature in the JEDEC SDRAM 21-C standard, issued in November 1993. (JX0056 at 115).

1002. The June 1994 email by Mr. Dillon stated that Rambus “may be able to make a . . . claim on auto precharge for *any* DRAM and therefore gain leverage over SDRAM” and certain DRAMs produced by the firm Mosys. (CX0738). Mr. Dillon stated that the feature was not fundamental to the performance of SDRAM, but said that “patenting this feature would have high harassment value, especially to the extent that third-party SDRAM controllers depend on it.” *Id.*

1003. The following day, CEO Geoff Tate sent an e-mail to Vice President Roberts on the subject at “sdram and most patent claims.” (CX0740). Mr. Tate wrote “this stuff is real critical,” and requested “a list of which claims we are making that read directly on current/planned sdrams” so that he could track progress from Mr. Vincent’s periodic status reports. (*Id.*)

August-September 1994 - Communication and Action by Patent Counsel

1004. On August 1, 1994, an attorney with the firm of Lester Vincent, the Rambus patent counsel, transmitted to Rambus Vice-President Allen Roberts a draft preliminary amendment to a pending Rambus patent application that included claims pertaining to dual-edge clock

technology. (CX0746 at 2; id. at 4-5 (claim 151, referring to information transmission “in response to a rising edge of the clock signal and a falling edge of the clock signal.”)).

1005. The draft application also contained claims relating to multibank design (CX0746 at 9-10 (claim 167, referring to an array of memory cells that is “subdivided into a plurality of memory sections, each of the memory sections being assigned a portion of the range of addresses”)) and to auto-precharge (CX0746 at 10 (claim 171, a dependent claim of claim 167 also referring to sense amps “for selectively pre charging the columns of the first `memory section”)).

1006. A handwritten note attached to this letter and attachment in Rambus files signed by “Allen” sought comments from others at Rambus and noted that “this is Lester’s attempt to work the claims for the MOST/SDRAM defense.” (CX0746 at 1).

1007. On August 31, 1994, Rambus employee Fred Ware responded to Allen Roberts, with copies to John Dillon and Rick Barth of Rambus, stating that the biggest omission in the claims was the lack of a normal access or a page mode access with auto-precharge. (CX0755). He added that the issue “may need some quick attention, since it’s a fairly important concept.” (Id.).

1008. On September 6, 1994, Mr. Vincent’s firm filed on behalf of Rambus an amendment to the pending Rambus patent application 08/222,646 (the ‘646 application); this application later resulted in the issuance of the Rambus ‘327 patent. (CX1493 at 1, 183). The new claims contained in the September 1994 amendment included a claim pertaining to a dual-edge clocking feature for use in DRAMs. (CX1493 at 183-201; Nusbaum, Tr. 1595-1603; Jacob, Tr. 5549-50; see CX1244 at 1).

September 1994 Committee Meeting - Presentation on PLL/DLL

1009. In September 1994 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Albuquerque, New Mexico. (JX0021 at 1; Crisp, Tr. 3199). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0021 at 4, 14-18).

1010. During the course of the September 1994 Committee meeting Mr. Crisp observed a presentation by NEC pertaining to a proposal for the use of an on-chip PLL circuit in future-generation SDRAM technology. (JX0021 at 91; Crisp, Tr. 3200-01). The proposal contrasted the potential use of PLL circuitry versus not using on-chip PLL circuitry. (JX0021 at 91; G. Kelley, Tr. 2570; Rhoden, Tr. 466; see also CX0711 at 36).

1011. In September 1994, the pending Rambus ‘692 patent application contained claims that a reasonable engineer would believe covered the on-chip PLL circuitry shown in NEC’s

proposal. (CCFF 1183 et seq.).

1012. Mr. Crisp immediately informed executive group and marketing group colleagues at Rambus, including CEO Tate, Vice-President Roberts and Vice-President Mooring. (CX711 at 36; Crisp, Tr. 3201-02). The subject line of Mr. Crisp's email read "NEC PROPOSES PLL ON SDRAM!!!" (CX0711 at 36 (emphasis in original)).

1013. In the email Mr. Crisp reported the NEC presentation and stated that "they plan on putting a PLL on board their SDRAMs." (CX0711 at 36). In the email, Mr. Crisp said that "we need to think about our position on this for potential discussion with NEC regarding patent issues." He concluded by stating: "***** I believe we have now seen that others are seriously planning inclusion of PLLs on board SDRAMs," and asking, "what is the exact status of the patent with the PLL claim?*****" (CX0711 at 36, 37 (emphasis in original)).

1014. Also on September 14, 1994, Vice-President Roberts replied to Mr. Crisp's e-mail. Although most of his e-mail apparently has been lost or destroyed, a portion remains as embedded text in an e-mail sent by Mr. Crisp. (CX0757 at 1; Crisp, Tr. 3208-11). Mr. Roberts apparently contemplated that Rambus might have to litigate to enforce patent claims covering PLL on a DRAM (CX0757 at 1 ("so if we want to fight this one (after the claim is issued), we better stock up our legal warchest.")).

1015. Still on September 14, 1994, Mr. Crisp replied to Mr. Roberts and the rest of the Rambus executive group. He agreed that litigation appeared likely not only regarding "PLL on a DRAM" and "PLL/DLL circuit implementations," but also with respect to other areas such as "programmable access latencies." (CX0757 at 1 ("It seems likely we will have to fight litigation at some point in the future.")). Mr. Crisp recognized that could involve JEDEC members. (Crisp, Tr. 3215 ("Q: Litigation might involve some of the other companies sitting in the very JEDEC room that day, wouldn't it? A: That's certainly a possibility.")). Mr. Crisp concluded by suggesting to the Rambus executive group that, if Rambus could get NEC to agree to a deal to "belly up some dollars," then Rambus could disclose the existence of its pending '651 patent application at JEDEC. (CX0757 at 1 ("I think if we can get them to agree to such a deal that the patent issue could be brought up in JEDEC ..."))).

1016. In the 1994 time frame, Mr. Mooring believed that putting a PLL on a DRAM was an invention of Rambus. (CX2098 at 397-98 (Mooring, Micron Dep.)). Gary Harmon, Rambus CFO, also testified that "I believe that we have or felt we had a patent on using PLLs on a DRAM" at the time. (CX2070 at 138-39 (Harmon, Micron Dep.)).

1017. Mr. Crisp never informed the Committee concerning his discussions with Rambus patent counsel or disclosed whether Rambus had a patent application on file pertaining to the use of on-chip PLL circuitry. (Crisp, Tr. 3207-08, 3451-52). At the September 1994 Committee meeting Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent

or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

October 1994 - Rambus Contemplates Litigation

1018. In late October 1994, Mr. Crisp and Rambus executives again discussed the possibility of suing other companies for using PLLs on SDRAMs. At that time, Rambus was negotiating a potential license agreement with Samsung. Samsung wanted a license agreement that was broader than just RDRAMs, so if they manufactured other types of DRAMs that happened to use Rambus technology, they wouldn't be sued. (Crisp, Tr. 3220-21). Although Rambus wanted to limit the agreement to "compatible uses," *i.e.*, to use in RDRAMs (Crisp, Tr. 3220-21), Samsung "made it abundantly clear" that, unless they got broader protection, "there will be no deal." (CX0767).

1019. On October 25, 1994, CEO Geoff Tate summarized the Samsung "deal details" in an e-mail to Rambus executives and Mr. Crisp. (CX0762). Mr. Tate wrote that pursuant to the negotiated terms, Rambus could not sue Samsung unless Samsung intentionally used Rambus technology in a DRAM that competed with RDRAM. (*Id.* at 1). Mr. Tate described this as "the big issue." (*Id.*) As an example, Mr. Tate explained that Rambus could not sue Samsung for putting a PLL on an SDRAM. (*Id.* ("So if they put for example a PLL on an SDRAM we can't sue them")). In a separate e-mail, Mr. Tate explained that he didn't like the terms, but they were the best that Rambus could get. (CX0765 ("we cannot get a Samsung deal without something like the If compromise we gave them. . . . I don't like the compromise but it's what we can get"))).

1020. Vice-President Allen Roberts replied to Mr. Tate in an e-mail that apparently was lost or destroyed. A portion remains, however, embedded in an e-mail from Richard Crisp. (CX0763; Crisp, Tr. 3221-22). Mr. Roberts wrote: "Is the following a mistype on your part?? Why can't we sue for using a PLL on an SDRAM if we granted [sic] that patent? This is going to be an important point." (CX0763).

1021. Mr. Crisp responded to Mr. Roberts and the entire Rambus executive group that Rambus needed to hold, and to be able to collect royalties on, its patent relating to on-chip PLLs. (CX0763 ("I've felt for some time that we need to hold this as one of or key technology patents. If it is allowed, we need to be able to collect on it."; see also Crisp, Tr. 3223-24 (Crisp wanted to collect "whatever monies [Rambus] could get" for the patent)). Mr. Crisp added that he hoped Rambus would sue other companies, particularly those that did not have a RDRAM license, and collect a royalty similar to that for RDRAM. (*Id.*)

1022. In a separate e-mail sent the same day, Mr. Crisp replied to an e-mail from Vice-President Roberts (also apparently lost or destroyed) regarding Mr. Roberts' explanation of use

of a “DLL or PLL.” (CX0764). Mr. Crisp emphasized again, “we worked hard to get the claims we did in the original patent filings (really the divisionals). I hate to see us not get the full benefit from them.” (*Id.*)

1023. In an e-mail sent the following day, on October 26, 1994, Mr. Crisp emphasized to CEO Geoff Tate and the Rambus executive group his belief that PLLs or DLLs on SDRAM could be the key to SDRAM reaching speeds of 150 MHz or 200 MHz. CX0766 at 1 (PLLs/DLLs on SDRAMs “may be the key to the 150-200 mhz clock puzzle for the SDRAM boys”). Mr. Crisp emphasized the need to keep proper perspective on “the significance of a PLL on a DRAM.” (*Id.*) Mr. Crisp added that the license agreement with Samsung might be good because, as Samsung pulled the market along in the direction of using PLLs or DLLs on SDRAMs, Rambus would “get opportunities to sue” other companies that followed Samsung’s lead. (*Id.*)

1024. CFO Gary Harmon disagreed with the assessment of CEO Geoff Tate, opining that Rambus could still sue Samsung for using PLLs on SDRAMs despite the terms of the agreement.. (CX0767 (“And I don’t agree that we can’t sue [Samsung] for infringement if they put a PLL on a SDRAM.”)). When Vice President Roberts asked whether Rambus should inform Samsung that Rambus considered the idea of clock compensation on the DRAM to correct date timing to be a Rambus invention, CFO Harmon responded that Rambus should “not rock the boat until the money is in the bank.” (CX0770).

1025. In late November 1994, Vice President Allen Roberts spoke to Mr. Lester Vincent and requested a copy of the PLL and DLL claims. (CX3126 at 495 (Vincent, Dep.)).

December 1994 - JEDEC Committee Meeting

1026. In December 1994 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Maui, Hawaii. (JX0022 at 1). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0022 at 3, 12-16).

1027. At the December 1994 Committee meeting Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

January-February 1995 - Rambus Patent Activity

1028. On January 6, 1995, Rambus filed a preliminary amendment to its pending ‘961 patent application cancelling the original claims and adding new ones. (Nusbaum, Tr. 1543-44; CX1504-216). Rambus had filed the ‘961 application in March 1992. (Nusbaum, Tr. 1542;

CX1504-019). The preliminary amendment to the '961 application contained claims that a reasonable engineer could construe to cover use of programmable burst length and programmable CAS latency in synchronous DRAMs. (Nusbaum, Tr. 1540-72; Jacob, Tr. 5507-28; see CCFF 1125 et seq.).

1029. On February 2, 1995, Rambus engineer Richard Barth met with Rambus outside patent counsel Maria Sobrino, a partner in Mr. Vincent's law firm. (CX1978; Second Stipulations, No. 1, 2). Ms. Sobrino's notes indicate that she and Mr. Barth discussed claims directed against synchronous DRAM manufacturers, including claims relating to PLLs/DLLs on DRAMs. (CX1978 at 1 ("Claims to prevent Synch DRAM mftgrs [sic]. Where do we claim using PLL/DLL on DRAMs for phase compensation for DRAMs."); Second Stipulations, No. 1, 3).

1030. In late February, 1995, Mr. Crisp informed Rambus executives and the business development group that Mr. Farhad Tabrizi of Hyundai announced at a RamLink meeting that he wanted to make a first showing of RamLink/SyncLink at the May 1995 JEDEC meeting (CX0783 at 1). Mr. Crisp suggested that one angle Rambus could take was to tell the Hyundai representatives in Korea that RamLink/SyncLink involved difficult problems and they were embarking on a very risky path, and that when they were finished they would probably have to pay Rambus higher royalties than they would pay for RDRAM. (CX0783 at 1-2 ("And then tell them that when they get finished they will probably find themselves mired in a big intellectual property trap which may result in higher royalties being paid to Rambus than if they simply license the [Rambus] technology and use it for 100% compatible [RDRAM] products.")) However, Mr. Crisp was reluctant to inform Hyundai of this intellectual property issue because of concern that it would become known at JEDEC. (CX0783 at 2 ("I certainly do not want to bring this intellectual property issue up without careful consideration. I especially do not want it all over JEDEC ..."))).

March 1995 - JEDEC Committee Meetings

1031. In March 1995, Richard Crisp was present for Rambus at a meeting of the JEDEC JC-16 Committee meeting in Las Vegas, Nevada. (CX0082 at 1).

1032. During the course of this March 1995 Committee meeting Mr. Crisp observed a presentation by Fujitsu pertaining to a proposal for a technology for high-speed bus transceiver logic known as STBUS. (CX0082 at 3, 12-16; CX0711 at 52-54). Mr. Crisp reported by email concerning the presentation to Rambus executives. (CX0711 at 52-54). In his report Mr. Crisp stated that the Fujitsu proposal relied on externally bussed reference voltage (CX0711 at 54; Crisp, Tr. 3241) and observed that because of this aspect of the technology, the proposal "may well infringe our work." (CX0711 at 54).

1033. Mr. Crisp did not tell anyone at JEDEC that he thought that the Fujitsu proposal

might well infringe Rambus patents. (Crisp, Tr. 3242).

1034. In March 1995 Richard Crisp also was present for Rambus at the JEDEC JC-42.3 Committee meeting in Las Vegas. (JX0025 at 1). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0025 at 3, 18-26).

1035. In the course of this March 1995 Committee meeting, there was continued discussion among Committee members concerning TI patent coverage of the Quad CAS technology. (JX0025 at 5). TI submitted to JEDEC a letter complying with the EIA patent policy (JX0025 at 5); this was the basis for a unanimous vote by the Committee resolving the issue. (*Id.*).

1036. In the course of this March 1995 Committee meeting, Mr. Crisp observed and later reported to Rambus executives that there was discussion during the “patent review session” of the meeting that AT&T was reported to have a patent on EDO technology, and that efforts were being made to determine what the patent covered and what position AT&T would adopt concerning licensing. (CX0711 at 57).

1037. In the course of this March 1995 Committee meeting, Mr. Crisp observed and later reported to Rambus executives that there was discussion by a Fujitsu representative concerning the use of synchronous clocking in high-speed operation. (CX0711 at 56). Mr. Crisp remarked to his Rambus colleagues that “[i]t appears they are starting to figure out that we have a very good idea with respect to synchronous source clocking. Of course they may get into patent trouble if they do this.” *Id.* at 58. Mr. Crisp had in mind patent trouble with Rambus patents. (Crisp, Tr. 3248).

1038. Mr. Crisp did not tell anyone at the Committee meeting that he thought that Fujitsu might get into trouble with Rambus patents if it went ahead with its proposal. (Crisp, Tr. 3248). Despite the various patent-related discussions that occurred at the March 1995 Committee meeting, Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

April 1995 - Rambus Renews Its JEDEC Membership

1039. In April 1995 Rambus paid its dues to renew its JEDEC membership. (CX0602 at 6).

April 1995 - Rambus Strategic Query

1040. In April 1995, Rambus CEO Geoff Tate wrote a follow-up email to John Dillon’s

June 1994 message suggesting that Rambus might be able to make a broader patent claims on auto-precharge, which would “have high harassment value” with respect to SDRAMs and third-party SDRAM controllers. (CX0791). Mr. Tate asked, “what did we end up doing about this idea?” (*Id.*). Any response to Mr. Tate’s question was apparently lost or destroyed.

May 1995 - JEDEC Committee Meeting

1041. In May 1995 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in New Orleans, Louisiana. (CX0088A at 1; Crisp, Tr. 3250). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (CX0088A at 2).

1042. During the course of the meeting there were discussions concerning a variety of patent-related issues, including: the showing of a letter from TI concerning the patent policy (CX0088A at 2, 13); the showing of a new Hitachi patent on SIMM mounting (CX0088A at 2, 13); the showing of a letter from Sun clarifying their compliance with the patent policy (CX0088A at 2, 14); and a report from Intel that the EDO patent issue was being worked internally towards a solution (CX0088A at 2).

1043. In the course of the May 1995 Committee meeting, Mr. Crisp observed three different presentations relating to SyncLink architecture. (Crisp, Tr. 3252, 3259). The SyncLink design was being developed by a group working under the auspices of the IEEE; the technology involved a packetized system and was similar to the proprietary Rambus architecture in a number of ways. (Crisp, Tr. 3254-55; see CCFF 1504). Among other things, the SyncLink technology presented at the May 1995 Committee meeting involved the use of both the rising and falling edge of the clock for data input. (CX0088A at 58 (“Reference clock, both edge for input, positive edge for output”); Crisp, Tr. 3261-63; CX0711 at 156).

1044. At the May 1995 Committee meeting, there were inquiries about possible patent issues pertaining to the SyncLink technology. Gordon Kelley of IBM asked whether or not HP, Hyundai, Mitsubishi or TI had any patents covering any of the matters being presented; all of these companies stated that they did not. (CX0711 at 72; Crisp, Tr. 3264-65). Sam Calvin of Intel and Gordon Kelley of IBM also inquired whether there were any Rambus patents covering the SyncLink technology. (CX0711 at 73; Crisp, Tr. 3266-67). When Mr. Crisp did not respond to this inquiry at the May 1995 meeting, Mr. Kelley asked Mr. Crisp to go back to Rambus and then report back to the Committee whether Rambus knew of any patents, especially Rambus patents, that may read on the SyncLink technology. (CX0711 at 73; CX0794 at 4; Crisp, Tr. 3267-68).

1045. In his e-mail informing the Rambus executives, engineering managers and business development and marketing groups of this development, Mr. Crisp listed a few ideas he had of Rambus intellectual property issues regarding SyncLink (CX0711 at 68, 73). His list

included:

- “1. DRAM on a packet oriented bus
2. DRAM with low swing signaling
- *. . . .
4. DRAM with programmable access latency”

(CX0711 at 68, 73).

1046. Mr. Crisp offered his suggestion of how to respond to the JEDEC request as well as what Rambus might want to mention to Hyundai in their attempts to restart negotiations. He suggested that Rambus “review our current issued patents and see what we have that may work against them.” (CX0711 at 68, 73). He recommended that Rambus consider “simply provid[ing] a list of patent members which have issued” and telling JEDEC members to “decide for yourselves what does and does not infringe.” (*Id.*) Mr. Crisp added, however, that if the Rambus patents were “not a really key issue . . . then it makes no sense to alert them to a potential problem they can easily work around,” and that “we may not want to make it easy for all to figure out what we have especially if nothing looks really strong.” (*Id.*)

1047. Following receipt of Mr. Crisp’s e-mail, Rambus CEO Tate wrote in his personal notebook,

(CX1723 at 138

in camera).

1048. Despite the various patent-related discussions that occurred at the May 1995 Committee meeting and the specific inquiry concerning Rambus patents on SyncLink technology, Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

June 1995 - Rambus Patent Activity

1049. On June 6, 1995, Rambus filed its patent application no. 08/469,490 (the ‘490 application). (CX1504-246; Nusbaum, Tr. 1572). The ‘490 application was a continuation of the ‘961 application. (Nusbaum, Tr. 1572). The ‘490 application contained claims covering a JEDEC-compliant SDRAM, the use of such an SDRAM, and a computer system incorporating a JEDEC-compliant SDRAM. (Nusbaum, Tr. 1573-1578; Jacob, Tr. 5528-32; see CCFF 1164 et seq.).

Summer 1995 - Rambus Patent Efforts Directed at SyncLink

1050. After the May 1995 Committee meeting, Mr. Crisp did a “general sort of read” of Rambus intellectual property. (Crisp, Tr. 3274). Mr. Crisp had access to the entire set of Rambus patent files; he doesn’t recall which of those materials he actually reviewed at the time. (CX0798; Crisp, Tr. 3585-86).

1051. Mr. Crisp focused on a particular patent application that had been earlier filed for Rambus by patent counsel Lester Vincent. (Crisp, Tr. 3274, 3274-76). A discussion between Mr. Crisp and colleagues including Vice-President Allen Roberts concluded that the particular patent application had legal problems and could only be salvaged by filing a new divisional patent application. (CX0796; Crisp, Tr. 3276-77).

1052. Mr. Crisp informed Vice-President Roberts, Vice-President Mooring, and Rick Barth that the patent application Rambus had filed in 1990 should allow Rambus to block SyncLink; Rambus just needed to “sweat through the details” of ensuring that Rambus obtained the appropriate claims. (CX0797; Crisp, Tr. 3279). Mr. Crisp stated his view that if it was necessary to do so, a new divisional application should be filed. (CX0797 (“if it is possible to salvage and get anything that helps us get a claim to shoot SyncLink in the head, we should do it”)). Mr. Crisp volunteered to take ownership of this task. (*Id.*).

1053. On July 21, 1995, Don Stark, an engineer at Rambus, circulated an e-mail to all Rambus staff calling specific attention to the SyncLink clocking scheme, and the fact that SyncLink used both edges of the clock to input data. (CX0711 at 156, 157; Crisp, Tr. 3261-62).

1054. By July 1995 Mr. Crisp reported to Vice-President Roberts and CEO Geoffrey Tate that he had done a review of Rambus intellectual property and wanted to talk with Lester Vincent about adding claims to Rambus patent applications in order to better describe Rambus inventions. (CX0824; Crisp, Tr. 3300). Mr. Roberts authorized Mr. Crisp and Rick Barth of Rambus to speak with Mr. Vincent, and they did so in early August 1995. (CX0825; CX2000 at 12 (Vincent time record entry for August 2, 1995)).

1055. During the later part of 1995, Rambus apparently provided Mr. Vincent with a copy of a SyncLink standard or data sheet, and as of December Mr. Vincent was engaged in preparing a preliminary patent application amendment based on his review of the SyncLink proposed standard. (CX2000 at 13 (Vincent time record entries for Dec. 5, 14 and 15, 1995); CX3130 at 166-68 (Vincent, Dep.)).

August-September 1995 - Renewed Estoppel Concerns

1056. In August 1995, Rambus hired Anthony Diepenbrock as Intellectual Property Manager for Rambus. (CX0827). The internal announcement by Rambus CEO Geoffrey Tate stated that a reason for hiring Mr. Diepenbrock, who was trained as an engineer and an attorney, was to have someone who would “focus[] full time on our strategy for protecting IP, analyzing

our IP position vs competitive technologies, etc.” (*Id.*). Among the competitive technologies that Mr. Tate wanted Mr. Diepenbrock to focus on were SDRAM and SyncLink. (Diepenbrock, Tr. 6111-12).

1057. On September 12, 1995, Rambus CEO Tate sent an e-mail to all Rambus executives, engineering managers, and members of the business development group reminding them that Mr. Diepenbrock’s “number 1 objective” was to “understand competitive technology” and “determine what should be done to strengthen [the Rambus] IP position relative to competition.” (CX0832). Mr. Tate requested that the recipients forward to Mr. Diepenbrock any e-mails they received talking about competitive technology developments and directions, such as “JEDEC meeting reports.” (*Id.*)

1058. Also on September 12, 1995, Rambus CEO Tate began a series of weekly one-on-one meetings with Mr. Diepenbrock. Mr. Tate’s notes from the September 12 meeting indicate that Mr. Tate instructed Mr. Diepenbrock, “cover: SDRAM -Now-Next SyncLink Mosys” and “steps: 1. Understand our IP; 2. Understand competitive Tech. And Directions; 3. Assess or current Patents - what claims/strength (?) Do we have vs. competition and what can we do?5. Plan of Action; 6. Implement.” (CX1730 at 1). Mr. Tate’s notes from his September 19, 1995 meeting with Mr. Diepenbrock indicate that they discussed, “Claims in issued patents that read on current SDRAMs/Mosys/SyncLink.” (C’S 1731 at 1).

1059. Shortly after Mr. Diepenbrock was hired at Rambus, Rambus patent counsel Lester Vincent spoke with Mr. Diepenbrock concerning the issue of equitable estoppel. (Diepenbrock, Tr. 6216-17). Mr. Vincent told Mr. Diepenbrock that he had a concern that Rambus employees attending standards bodies meetings in some capacity could raise an equitable estoppel issue regarding patents that Rambus had or was seeking. (Diepenbrock, Tr. 6217-18). After studying the issue himself, Mr. Diepenbrock came to agree with Mr. Vincent about the risk of Rambus employees, including Richard Crisp, attending such meetings. (Diepenbrock, Tr. 6218-19).

1060. Mr. Diepenbrock conveyed the shared concerns of himself and Mr. Vincent concerning equitable estoppel risks to Mr. Crisp, who at the time did not perceive the risk. (Diepenbrock, Tr. 6219; *see* Crisp, Tr. 3005-06). Mr. Vincent told Mr. Diepenbrock he had raised the issue before Mr. Diepenbrock joined Rambus. (Diepenbrock, Tr. 6219; *see* CX3127 at 114, CX3126 at 553 (Vincent, Dep.) (hallway conversation between Mr. Diepenbrock and Mr. Crisp)). Mr. Diepenbrock talked with Mr. Crisp about these concerns. (CX2082 at 804-06 (Crisp, Dep.)).

1061. In late September, Mr. Crisp wrote an email to Rambus executives that referred to “Tony’s worst case scenario regarding estoppel” and stated that “the only thing lost is the ability to enforce our rights against those that can prove estoppel applies. . . . We do not have our patent invalidated.” (CX0837 at 1; Crisp, Tr. 3005-06). Mr. Crisp reminded Rambus executives that when Rambus joined JEDEC, a group of individuals within Rambus decided that Rambus would

not talk about potential for patent infringement. (Crisp, Tr. 3325). He suggested that Rambus re-evaluate its position relative to what it decided to disclose and what to keep quiet about. He also suggested that they “redouble [their] efforts” to get the necessary amendments completed and new claims added to its pending patent applications in order to “make damn sure this ship is watertight before we get too far out to sea.” (CX0837 at 2; Crisp, Tr. 3325-26).

September 1995 - JEDEC Committee Meeting

1062. In September 1995 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Crystal City, Virginia. (JX0027 at 1; Crisp, Tr. 3305). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0027 at 4, 20-25; Crisp, Tr. 3306).

1063. Among the patent matters discussed at the September 1995 Committee meeting was the response of Rambus to the inquiry made at the May 1995 Committee meeting concerning patents on SyncLink. (Crisp, Tr. 3306-08). Mr. Crisp provided the Committee a letter from Rambus in which Rambus refused to provide any information concerning whether there were Rambus patents or patent applications that might apply to SyncLink. (CX0829; JX0027 at 26 (“Rambus elects not to make a specific comment on our intellectual property position relative to the SyncLink proposal.”)). The letter included other recitations, including the observation that it would be several years before there was a finalized SyncLink specification to analyze for possible infringement, and that SyncLink was being developed under the auspices of IEEE, which had “a less stringent patent policy than JEDEC.” (*Id.*).

1064. Rambus Vice-President Mooring, as Mr. Crisp’s supervisor, worked with Mr. Crisp and approved the language in the letter stating that “Rambus elects not to make a specific comment on our intellectual property position” on the SyncLink proposal. (CX2112 at 206-07 (Mooring, Dep.)). There is nothing in the letter informing the Committee that Rambus had pending patent applications relating to specific SDRAM technologies of programmable CAS latency, programmable burst length, on-chip PLL or DLL, and dual edge clocking. (CX2056 at 274 (Mooring, Dep.)).

1065. At the September 1995 Committee meeting Mr. Crisp read the Rambus letter to the JEDEC Committee electing to make no comment on the Rambus intellectual property position (JX0027 at 26). The letter generated discussion. (CX0711 at 66). Mr. Crisp reported to his Rambus colleagues that Gordon Kelley of IBM commented at the meeting that “he heard a lot of words but did not hear anything said.” (*Id.*).

1066. In the course of the discussion of the Rambus letter at the September 1995 Committee meeting, Mr. Crisp reminded the Committee that Rambus in the past had reported a Rambus patent to the Committee. (Crisp, Tr. 3312). This was a reference to the disclosure to the Committee of the Rambus ‘703 patent in September 1993. (*Id.*). Mr. Crisp was saying that

Rambus was in the category of JEDEC members that had disclosed patents. (Crisp, Tr. at 3313).

1067. Mr. Crisp did not tell the Committee that he was working to draft claims to shoot SyncLink in the head (Crisp, Tr. 3316) or that he believed that SyncLink would violate Rambus patents (Crisp, Tr. 3316). Mr. Crisp did not identify what particular aspects of the SyncLink technology might infringe Rambus intellectual property. (Crisp, Tr. 3317). He did not identify the SyncLink dual edge clocking feature as a feature that might violate Rambus intellectual property. (Crisp, Tr. 3317). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

1068. Mr. Crisp reported to his Rambus colleagues that there would be no second showings of the SyncLink material at the September 1995 Committee meeting. (CX0711 at 171). Mr. Crisp reported that one of the meeting participants told Mr. Crisp that he thought the reason there would be no second showings of the SyncLink technology at JEDEC was that “we [Rambus] have cast doubt over the patent issue.” (*Id.*).

Fall 1995 – Rambus Strategy Presentation

1069. In the fall of 1995, Rambus Intellectual Property Manager gave a presentation to Rambus employees on “Rambus IP strategy.” (CX1267; Diepenbrock, Tr. 6129-30). The slides included discussion of “Offensive” and “Defensive” strategies. (CX1267; Diepenbrock, Tr. 6130). The “Offensive” patent strategy, according to Mr. Diepenbrock, meant “finding key or essential areas of Rambus intellectual property and claiming them as broadly as possible.” (Diepenbrock, Tr. 6131). The first example of the “Offensive” strategy relates to DLLs, or delay locked loops. (CX1267; Diepenbrock, Tr. 6131-32). The second example given relates to dual edge clocking technology, or transmitting or receiving data on both edges of the clock. (C’S 1267; Diepenbrock, Tr. 6132-33). At the time this presentation was given, Rambus had pending patent applications relating to both these features. (Diepenbrock, Tr. 6133).

Fall 1995 - SDRAM Lite and Next Generation SDRAM Ballots

1070. Among the topics discussed at the September 1995 JC-42.3 Committee meeting was NEC’s SDRAM Lite proposal. (JX0027 at 13). NEC proposed a reduced-feature version of the SDRAM in order to reduce costs. NEC proposed to use a single CAS latency value and burst length value. (CCFF 572). The Committee decided to issue a survey ballot to its members regarding the SDRAM Lite proposal. (CCFF 573). Mr. Crisp received this ballot by e-mail. (CX0711 at 196-99).

1071. Also among the topics discussed at the September 1995 JEDEC JC-42.3 Committee meeting was the preparation and distribution of a survey ballot to obtain Committee members’ views concerning various features in connection with “next generation” SDRAM

standard technology. (JX0027 at 14; Crisp, Tr. 3323-24). In the aftermath of that meeting, a survey ballot dated October 30, 1995, was prepared and distributed to JC-42.3 Committee members including Rambus. (Crisp, Tr. 3328-29; CX0260 at 1).

1072. Among the issues inquired about in the next generation SDRAM survey ballot was whether Committee members believed that it was important to standardize CAS latency beyond the values permitted under the existing SDRAM standard. (CX0260 at 9). The ballot also asked members to state whether they believed that on-chip PLL or DLL was important to reduce the access time from the clock for future generations of SDRAM (CX0260 at 12), and whether they believed future generations of SDRAM could benefit from using both edges of the clock for sampling inputs (*id.*).

1073. The survey ballot was received by Rambus and distributed to the business development and marketing groups of Rambus. (Crisp, Tr. 3329; CX2056 at 264 (Mooring, Dep.)). Mr. Mooring summarized the reaction at Rambus: “We [Rambus] believe we invented key aspects of several of the things on this list.” (CX2056 at 268 (Mooring, Infineon Dep.)).

Fall 1995 - Rambus Patent Activity

1074. During October 1995, Anthony Diepenbrock of Rambus met with outside Rambus patent attorney Lester Vincent concerning pursuit by Rambus of patents pertaining to DLL technology. (CX1988 at 2).

1075. In October 1995, Mr. Vincent’s firm filed on behalf of Rambus an amendment to the pending Rambus ‘692 patent application. (CX1483 at 1, 8; see also CX1502 at 233, 241). This amendment modified an earlier amendment of the application, filed in June 1993, that contained claims pertaining to the use of PLL circuitry. (CX1502 at 208; Nusbaum, Tr. 1583-85). The ‘692 application as amended in October 1995 contained multiple claims addressing on-chip PLL technology. (Nusbaum, Tr. 1584; CX1502 at 233-35 (claims 151, 152, 166, 167)).

1076. The United States Patent and Trademark Office sent Mr. Vincent’s firm a Notice of Allowance of claims with respect to the ‘646 application on October 6, 1995. (CX1482; Diepenbrock, Tr. 6190). A Notice of Allowance occurs when the patent office has reason to believe that claims in a particular application should be issued. (Diepenbrock, Tr. 6151). A Notice of Allowance means that “other than the actual publication of the patent, it’s essentially a done deal.” (CX2114 at 23 (Karp, Dep.)).

1077. The ‘646 patent application, which later resulted in the issuance to Rambus of its ‘327 patent, contained claims related to moving input or output data on the rising and the falling edges of the clock. (Diepenbrock, Tr. 6144-46; Nusbaum, Tr. 1597, 1601-1603; see also Jacob, Tr. 5550-5551 (technical expert opinion that claim describes the general concept of dual edge clocking technology)). Internal Rambus documents refer to the ‘646 application, also known

internally as the P 001C2 application, as “the clocking patent.” (CX0871 at 1; Diepenbrock, Tr. 6168). Anthony Diepenbrock, the patent attorney who was employed starting in the fall of 1995 to manage Rambus’ intellectual property portfolio (Diepenbrock, Tr. 6099, 6106-6107), testified that the P 001C2 application “included claims having qualifiers that related to moving data on the rising and the falling edges of the clock.” (Diepenbrock, Tr. 6145). (See also CX2114 at 212 (Karp, Dep.)).

December 1995 - JEDEC Committee Meeting

1078. In December 1995 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Dallas, Texas. (JX0028 at 1; Crisp, Tr. 3337). The JEDEC patent policies had been the subject of a presentation in a plenary session of JEDEC prior to this Committee meeting; those presentation materials including the patent tracking list are an attachment to the minutes. (JX0028 at 3, 12-23).

1079. Among the topics discussed at the Committee meeting were the responses to the future SDRAM features survey ballots that had been distributed to Committee members in October 1995. (JX0028 at 6, 36). The Representative from Mosaid, the Committee member that had conducted the survey for the Committee, made a presentation concerning the results of the survey. (JX0028 at 6). Among the survey results was a tally showing that most responding Committee members believed that it was important to standardize CAS latency beyond the values permitted under the existing SDRAM standard. (JX0028 at 42). The tallied results showed that most responding Committee members believed that on-chip PLL or DLL was important to reduce the access time from the clock for future generations of SDRAM. (JX0028 at 45). The tallied results showed that the majority of the responding Committee members did not believe future generations of SDRAM could benefit from using both edges of the clock for sampling inputs. (JX0028 at 45).

1080. During the course of the December 1995 discussion of the survey ballot results, the representative of Mosaid disclosed that Mosaid had a patent pending on DLL technology, but stated that the patent pertained to a particular implementation and may not be required to use the standard. (JX0028 at 6; Crisp, Tr. 3342). Mr. Crisp reported to his colleagues at Rambus that Mosaid had reported the existence of a “pending patent application for PLL/DLL on SDRAMs” and repeated the characterization of the application as an implementation patent. Mr. Crisp reported that if the patent is a “concept patent,” Mosaid would comply with the JEDEC patent policy. (CX0711 at 191-92).

1081. Mr. Crisp also reported: “The momentum is building for getting a new SDRAM standard kicked off. Kelly [sic] of IBM is saying that they need to do it right, to it to stand the test of time. He admits that the current devices will not run over 100mhz. They all say that it must change.” (CX0843 at 1). This report indicates that JEDEC was looking to the future and interested in developing a more high performance or high speed product. (CX2112 at 249

(Mooring, FTC Dep.)).

1082. Despite the discussion at the December 1995 JC 42.3 Committee meeting concerning CAS latency, on-chip PLL/DLL technology and dual-edge clocking, and despite the disclosure by Mosaid of a possibly relevant patent application, Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). At the meeting Mr. Crisp did not say anything at all with respect to any Rambus patent applications that might relate to CAS latency (Crisp, Tr. 3341); did not make any statements at all with respect to any pending patent applications that might relate to the use of on-chip PLL or DLL (Crisp, Tr. 3341, -44); and made no statement at all with respect to any patent applications that might relate to the use of a dual edge clock (Crisp, Tr. 3341). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

December 1995/January 1996 - The FTC Dell Consent And Rambus Decision to Withdraw From JEDEC

1083. In December 1995, Mr. Vincent sent Mr. Diepenbrock of Rambus materials relating to a proposed FTC consent order involving Dell Computer. (CX1990 at 1; Diepenbrock, Tr. 6222; see Rambus Answer at 34, ¶ 81). Mr. Vincent described the case as involving charges that Dell restricted competition in the personal computer industry and undermined the standard-setting process by threatening to exercise undisclosed patent rights against computer companies adopting standard technology. (CX1990 at 1).

1084. Shortly after he forwarded to Rambus a copy of the Dell decision, Mr. Vincent and his partner, Maria Sobrino, had a luncheon meeting with Rambus CEO Tate at which they discussed the FTC's proposed consent order in the Dell matter and the downside risk of participating in JEDEC. (CX3124 at 190-94 (Vincent, Dep.)). The downside risk was that somebody could raise the issue of equitable estoppel and argue that Rambus patents should not be enforceable. (*Id.* at 196-98). At the time Mr. Vincent discussed this downside risk, he did not know the facts as to what was going on with respect to JEDEC, and did not know the JEDEC disclosure policy. (CX3124 at 193-94 (Vincent, Dep.)).

1085. In January 1996, Mr. Vincent and others from his firm met with Rambus executives to discuss the Dell decision and other matters. (CX3126 at 537 (Vincent, Dep.); Crisp, Tr. 3357; CX2082 at 807-10 (Crisp, Dep.)). Among those attending from Rambus were CEO Tate, David Mooring, Tony Diepenbrock and Richard Crisp. (CX3126 at 537 (Vincent, Dep.)). The discussion at the meeting addressed the downside risk of the Dell case, which included the risk that a patent might be held unenforceable. (*Id.* at 538-39). Attorneys for Rambus advised Rambus that it should no longer participate in any standards bodies, in part because the risks associated with such participation outweighed any benefits. (Rambus Answer at 34, ¶ 81).

1086. Handwritten notes of Mr. Vincent from this time period (CX3126 at 543-44 (Vincent, Dep.)) reflect among a “to do” list of Rambus-related items the following notation: “No further participation in any standards body (if there has been any) – do not even get close!!” (CX1928 (emphasis in original)).

1087. Mr. Crisp recalled that the result of the meeting was a decision that Rambus should discontinue attendance at JEDEC meetings. (CX2082 at 809 (Crisp, Dep.)). An email from Mr. Crisp to CEO Tate and others at Rambus in late January 1996 stated: “So, in the future, the current plan is to go to no more JEDEC meetings due to fear that we have exposure in some possible future litigation.” (CX0858 at 2; Crisp, Tr. 3358).

1088. The final JEDEC meeting attended by Rambus was the meeting in December 1995. (Rambus Answer at 20, ¶ 41). Thereafter Rambus continued to receive certain JEDEC mailings for some time. (*Id.*). Rambus did not pay in response to a dues invoice sent by JEDEC in January 1996. (*Id.*). Rambus responded to the dues invoice by a letter dated June 17, 1996, in which it informed JEDEC that it was not renewing its membership in the organization. (*Id.*).

1089. One of the reasons Rambus left JEDEC was because it believed the items being discussed there looked more and more like Rambus products. (CX2112 at 202 (Mooring, FTC Dep.)). One of the features that Rambus saw involved dual edge clocking, such as was seen in the SyncLink proposal and what would eventually become DDR. (CX2112 at 205, C’S 2056 at 190 (Mooring, Dep.)).

1090. Equitable estoppel was another consideration in Rambus’ decision to leave JEDEC. (CX2112 at 222 (Mooring, FTC Dep.)).

1091. Another factor in the Rambus decision to leave JEDEC was its unwillingness to license its technology on RAND terms. In responding to a letter from Cheryl Rowden of the IEEE in February 1996, Rambus in-house counsel Anthony Diepenbrock stated that Rambus “had already licensed its technology and would continue to license its technology in accordance with its existing business practices.” (CX0869 at 1, responding to CX0490; Diepenbrock, Tr. 6223-6224). Mr. Diepenbrock did not agree with Ms. Rowden’s interpretation of an earlier letter as suggesting that Rambus would be willing to license applicants on reasonable and non-discriminatory (“RAND”) terms. (Diepenbrock, Tr. 6223-6224; CX0490 at 1). Mr. Diepenbrock testified that his view was that agreeing to RAND terms was inconsistent with Rambus’ business practices. (Diepenbrock Tr. 6228) Mr. Diepenbrock also testified that one of the reasons for taking this position was because he was uncertain that every contract Rambus had signed up to that point would meet a RAND standard. (Diepenbrock, Tr. 6228). Mr. Diepenbrock also testified that, to the best of his knowledge, Rambus has never submitted a RAND letter to any standard-setting organization, including JEDEC. (Diepenbrock, Tr. 6228-6229).

Early 1996 - Rambus Obtains Its ‘327 Patent

1092. In the late 1995-early 1996 time period, the then-extant rule at the United States Patent Office was that applicants had 90 days after receiving a Notice of Allowability of Claims to pay the fees for the issuance of the patent or the patent application could be deemed abandoned. (Diepenbrock, Tr. 6191-6192). On January 5, 1996, Rambus outside patent counsel sent a check for \$1,250.00 to the United States Patent and Trademark office for payment of issue fees relating to the '646 application, also known internally as the P001C2 application. (CX1487; Diepenbrock, Tr. 6192).

1093. By December 1995, Rambus in-house attorney Mr. Diepenbrock, had put in place a protocol with Rambus' outside patent counsel that required that he be notified prior after the Notice of Allowance and before the payment of any issue fees. (Diepenbrock, Tr. 6192-6194) (witness acknowledges accuracy of prior deposition testimony used to refresh recollection). Mr. Diepenbrock also testified that he passed on information that claims had been allowed to Geoffrey Tate, the CEO of Rambus. (Diepenbrock, Tr. 6191).

1094. On April 9, 1996, Rambus' outside patent counsel prepared a tracking report noting the issue date and patent number three weeks in advance of its issuance. (CX2008 at 3; *see also* CX3127 at 75 (Vincent, Dep.)). It is not uncommon for the patent office to provide advance notice of the issue date and patent number to parties seeking patents after a Notice of Allowance had been issued. (Diepenbrock, Tr. 6150). The '327 patent issued to Rambus on April 30, 1996. (CX1494).

1095. The issuance of the '327 patent was a noteworthy event at Rambus. (Diepenbrock, Tr. 6194). Mr. Diepenbrock discussed the fact that the '327 patent had issued with others in Rambus, including CEO Tate, prior to June of 1996. (Diepenbrock, Tr. 6194-95).

January 1996 - JEDEC Committee Meeting

1096. In January of 1996, the JEDEC JC-42.3 Committee held an interim meeting in Sunnyvale, California. (JX0029 at 1; Rhoden, Tr. 484). At that meeting there was additional discussion about Future SDRAM, and Micron submitted a first presentation for the use of echo clocks on the next generation of DRAMs. (JX0029 at 17-22; Lee, Tr. 6655-66).

1097. Desi Rhoden, currently the Chairman of JEDEC, testified that the Micron presentation at the January 1996 interim meeting would trigger a disclosure obligation under the JEDEC patent disclosure policy. (Rhoden, Tr. 488-489, referencing JX0029 at 17-22).

1098. Mr. Crisp of Rambus did not attend this Committee meeting, but received the minutes and circulated copies to others at Rambus (Crisp, Tr. 3561) with the following observation:

I have put copies of the JC42.3 meeting minutes in each of your

mail slots. Notice the Micron presentation especially the part about the separate transmit and receive clocks. I think we should have a long hard look at our IP and if there is a problem, I believe we should tell JEDEC that there is a problem.

(CX0868 at 1). This email was sent to Rambus CEO Tate, Vice Presidents Mooring and Roberts, Intellectual Property Manager Diepenbrock, and others. (*Id.*) Mr. Crisp testified at trial that he suggested telling JEDEC if there was an IP problem raised by the Micron presentation. (Crisp, Tr. 3367). Mr. Crisp further testified that he had no information that Rambus ever told Micron or JEDEC that there was an IP problem. (Crisp, Tr. 3367-3368).

1099. Despite Mr. Crisp's suggestion that Rambus tell JEDEC if there was an IP problem raised by the Micron presentation (Crisp, Tr. 3367), Rambus never informed JEDEC of any problems relating to the Micron presentation in January 1996. (Crisp, Tr. 3367-3368; CX2112 at 255-56 (Mooring, FTC Dep.)) By January 1996, Mr. Mooring believed there was a general trend toward more Rambus "inventions" being incorporated into JEDEC presentations. (CX2112 at 256 (Mooring, FTC Dep.)).

June 1996 - Rambus Seeks Enforcement Readiness Opinion on '327 Patent

1100. On June 17, 1996, Rambus' Mr. Diepenbrock forwarded a request for an enforcement readiness opinion to Rambus outside patent counsel Lester Vincent with respect to the '327 patent. (CX0889; Diepenbrock, Tr. 6195-6196) (enforcement readiness means an independent review of the file wrapper to determine if it was sufficient to assert claims against a possible infringer). This was the only occasion during his tenure at Rambus where Mr. Diepenbrock could recall requesting an outside opinion on the enforcement readiness of an issued Rambus patent. (Diepenbrock, Tr. 6198-6199).

1101. In the same letter, Rambus also sought the opinion of Mr. Vincent's firm regarding whether this patent would be infringed by a device that had been described in an earlier communication with the firm. (CX0889 at 2). The prior communication sent by Mr. Diepenbrock to Mr. Vincent involved a company called Mosys, about whom Rambus was concerned with possible infringement of the '327 patent. (Diepenbrock, Tr. 6203).

1102. Rambus documents suggest that a "competitive analysis" of the Mosys device had been prepared in January of 1996 (CX1316) and again in March of 1996 (CX1319). Richard Crisp, Rambus' JEDEC representative, attended meetings in the 1996 time frame involving representatives of Rambus and Mosys where the alleged infringement of Rambus patents by Mosys was discussed. (Crisp, Tr. 3368-3369). These discussions related, in part, to a particular implementation of dual edge clocking technology contained in a Rambus patent. (*Id.*)

1103. Rambus CEO Tate was the person who directed Mr. Diepenbrock to study the

Mosys device for possible infringement, and who sought the opinion from Mr. Vincent's firm in June 1996. (Diepenbrock, Tr. 6202, 6204). At the time Mr. Diepenbrock requested the enforcement readiness opinion of outside counsel in June of 1996, Rambus had only a data sheet and no silicon from the Mosys device but considered that to be sufficient information to seek the enforcement readiness opinion. (Diepenbrock, Tr. 6204).

1104. A facsimile sent by Mr. Diepenbrock to Mike Mallie of Mr. Vincent's firm included a diagram of the Mosys device and described the device as operating on "both edges of the clock." (CX0891 at 1). Mr. Mallie met with Mr. Diepenbrock and later advised him that he saw no problem with the enforceability of the '327 patent. (Diepenbrock, Tr. at 6205).

1105. By mid-August 1996, Rambus informed Mosys about its infringement concerns with respect to the '327 patent. (CX0901) (correspondence between the CEO of Mosys and the CEO of Rambus, Mr. Tate, referencing a August 16, 1996 letter from Rambus to Mosys). Mosys and Rambus eventually entered into licensing negotiations that concluded with Mosys paying Rambus a royalty rate of one percent of sales. (CX0927) (royalty of \$56,000 based on sales of \$5.6 million).

1106. Also in August 1996, shortly after having withdrawn from JEDEC, Mr. Crisp shared with others at Rambus a presentation, based in part on confidential JEDEC material, about SDRAM using double clocked data. (CCFF 1107-08).

1107. Mr. Crisp gave a presentation on SDRAM at a lunchtime meeting at Rambus called "the Rambler." (Crisp, Tr. 3393-95; CX1320 at 1-5; CX0905 at 1). Crisp reminded his co-workers that his Rambler presentation contained confidential JEDEC material. (Crisp, Tr. 3395; CX0905 at 1 (September 1996 email from Crisp to all Rambus staff: "One more time so that all hear: the material I presented in my Rambler contained some JEDEC material which is not permitted to be shared with any company who is not a member of JEDEC."))).

1108. Mr. Crisp's presentation discussed SDRAM using double clocked data. (CX1320 at 4 ("What about double clocked Data?" with a timing diagram referencing the rising and falling edges of a clock signal); *id.* at 5 ("Double Clocked Data (read case)" and "Double Clocked Data (write case)").

June 1996 - Rambus Withdraws from JEDEC

1109. On June 17, 1996, Richard Crisp of Rambus sent a letter to JEDEC secretary Ken McGhee formally withdrawing from JEDEC. (CX0887 at 1; CX0888 at 1).

1110. The June 17, 1996, withdrawal letter signed by Mr. Crisp states in part:

To the extent that anyone is interested in the patents of Rambus, I

have enclosed a list of Rambus U.S. and foreign patents. Rambus has also applied for a number of additional patents in order to protect Rambus technology.

(CX0887 at 1; CX0888 at 1).

1111. Attached to the June 17, 1996 withdrawal letter was a list of patents issued or assigned to Rambus. (CX0887 at 2; CX0888 at 2). The list contained no references to patent applications, and was not a complete list of issued patents because the '327 patent was not on the list. (CX0888 at 2; Crisp, Tr. 3381, 3384; Diepenbrock, Tr. 6200). No one at Rambus informed JEDEC about the '327 patent, either before or after it issued on April 30, 1996. (Diepenbrock, Tr. 6201-6202; Crisp, Tr. 3316).

1112. The date of the Rambus letter withdrawing from JEDEC, which omitted the '327 patent pertaining to dual-edge clock technology (CX0887; CX0888) is the same as the Rambus letter to outside patent counsel Lester Vincent seeking an enforcement readiness opinion with respect to the '327 patent. (CX0889 at 2).

1113. Earlier drafts of the JEDEC withdrawal letter contained language suggesting that the attached list of issued Rambus patents was complete, including the following statements: "In the spirit of full disclosure, Rambus Inc would like to bring to the attention of JEDEC all issued U. S. patents held by Rambus Inc." (CX0873 at 1) and "This list [of patents] is complete as of this writing and follows below." (CX0873 at 1; CX0874 at 1; Crisp, Tr. 3382-3383). The final June 17, 1996, withdrawal letter that was actually sent to JEDEC contained no such language. (CX0887 at 1; CX0888 at 1; Crisp, Tr. 3383-3384).

1114. None of the patents listed in the attachment to the June 17, 1996, withdrawal letter (CX0888 at 2) related to JEDEC work. (CX0887 at 2; Jacob, Tr. 5365-5366, 5501-5502). The '327 patent, which was not included in the list, did relate to JEDEC work on dual-edge clocking technology. (Jacob, Tr. 5366-5367, 5545-5549, 5551-5555).

Rambus Foreign Patent Activity

1115. From the earliest days of the company, Rambus planned to pursue intellectual property claims not only in the United States but in other countries as well. (CX0535 at 1 (1990 Rambus Business Plan: file a broad patent "in all major industrial nations"); *id.* at 4 ("The base patent is being filed over the next several months in the European Patent Office, Israel, Korea, Taiwan, Japan, India and Canada.")).

1116. During the time that Rambus was a JEDEC member, part of the work by Rambus patent counsel Lester Vincent on behalf of Rambus involved work on foreign patent filings, including counseling Rambus representatives with respect to the countries in which they should

file patent applications. (Vincent, Tr. 7878-79; see CX1937 at 28). This included providing Rambus with a chart listing countries currently or in the future expected to be involved in semiconductor manufacturing, packaging and assembly and computer production, to help Rambus in making foreign patent filing decisions. (CX1972 at 1, 2).

1117. Rambus filed an International Patent Application under the Patent Cooperation Treaty (the PCT application) on April 16, 1991. (CX1454 at 1). The PCT application claimed priority based on the Rambus '898 U.S. application. (CX1454 at 1). A PCT application is a mechanism that permits an applicant to file with the World Intellectual Property Organization ("WIPO") an application based on a United States patent application, and thereafter enter the patent registration process in various foreign countries within a specified period. (Vincent, Tr. 7883; see CX1948).

1118. Rambus also filed an application with the European Patent Office ("EPO"). The EPO is administrative mechanism for centralized examination of patent applications for various European countries. (Vincent, Tr. 7885-86, 7894-97). Rambus pursued examination of patent applications in this fashion in the United Kingdom, France, Germany and Italy. (Vincent, Tr. 7897; RX335).

1119. Rambus attempted to conform certain independent claims in the EPO application to the amended claims being prosecuted in the United States. (Vincent, Tr. 7899).

1120. As of approximately 1995, there were Rambus patent applications based on the original Rambus '898 patent application pending with the EPO (Vincent, Tr. 7885-86), the WIPO (Vincent, Tr. 7883), India (Vincent, Tr. 7882), Israel (Vincent, Tr. 7885), Japan (Vincent, Tr. 7886-87) and Korea (Vincent, Tr. 7887). As of that time, Rambus had also been issued a patent in Taiwan based on the specification contained in the original Rambus '898 patent application. (Vincent, Tr. 7883-85). (See also CX1982).

1121. Complaint Counsel has limited information regarding the prosecution of Rambus's foreign patents because Respondent has asserted attorney-client privilege with respect to work involving foreign patent filings. (Vincent, Tr. 7879). There are over fifty communications regarding Rambus's foreign patent filings between 1991 and 1996 that were not produced to Complaint Counsel because Respondent asserted the attorney-client privilege. (Steinberg Motion *In Limine*, Attachment 9, Rambus Privilege Log Entries 114, 116-27, 129, 138-48, 150-51, 174-76, 187-89, 239-47, 260-64, 619, 623, 631-32, 759, 1120, 1122-24, 1126-27, 1177).

C. During the Time That It Was A JEDEC Member, Rambus Possessed United States Patents Or Patent Applications That Read On The Four Relevant JEDEC Standard Technologies At Issue In This Case.

1122. Every patent that Rambus has asserted against SDRAM and DDR SDRAM products in patent litigation resulted from continuation or divisional patent applications flowing from the original '898 application. The asserted patents claim the benefit of the '898 application's April 18, 1990 filing date. (First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

1123. Moreover, every patent that Rambus has asserted in patent litigation can trace its lineage to one of two patent applications in the '898 family: either the 08/222,646 ("646") or the 07/847,961 ("961"). (First Stipulations, No. 22; Exhibit A to First Stipulations, No. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

1124. Rambus was a member of JEDEC from December 1991 until June 1996. (CCFF 878, 1109). The '898, '646 and '961 applications were pending while Rambus was a member of JEDEC. (First Stipulations, No. 22; Exhibit A to First Stipulations, No. 22; *see also* DX0014).

1. The Rambus '961 Patent Application Contained Claims Covering Programmable CAS Latency and Programmable Burst Length.

1125. Rambus patent application 07/847,961 (the '961 application) contained claims covering, or that a reasonable engineer could interpret as covering, the programmable burst length and programmable CAS latency features of JEDEC-compliant SDRAMs. (Nusbaum, Tr. 1540-72; Jacob, Tr. 5507-28).

1126. Rambus filed the '961 application in the PTO on March 5, 1992. (Nusbaum, Tr. 1542; CX1504-019). As filed, the '961 application contained claims 95-105 of the original 150 claims submitted with the '898 parent patent application. (Nusbaum, Tr. 1542-43; CX1504-173-175).

1127. The patent examiner issued a first Office Action in the '961 application on September 6, 1994. (Nusbaum, Tr. 1544; CX1504-208). In response to that Office Action, Rambus submitted an Amendment on January 6, 1995, cancelling the original claims and adding new ones. (Nusbaum, Tr. 1543-44; CX1504-216). The January 6, 1995, Amendment was Rambus's first change to the '961 application. (Nusbaum, Tr. 1544).

(A) Claim 160 of the '961 Application

1128. Claim 160 of the '961 application recites:

[1] In a memory storage system including a bus, a semiconductor device

[2] having that [sic] is configurable by a device that is external to

the semiconductor device, comprising:

[3] at least one pin for coupling the semiconductor device to the bus; and

[4] at least one register operative to store information

[5] specifying a manner in which the semiconductor device is to respond to transaction requests received from the bus,

[6] . . .wherein the information is received by the semiconductor device from the bus when the semiconductor device is configured, the semiconductor device storing the information received from the bus lines in the register during configuration of the semiconductor device

[7] and thereafter responding to transaction requests in the manner specified by the information stored in the register.

(CX1504 at -221-22) (numbering added).

1129. An SDRAM compliant with Release 4 of the JEDEC SDRAM standard (JX0056) contains each limitation of claim 160 of the '961 application. (Nusbaum, Tr. 1550-55).

1130. A reasonable engineer could construe claim 160 to cover both the programmable CAS latency and the programable burst length features of an SDRAM compliant with Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5507-17).

1131. A JEDEC-compliant SDRAM is a semiconductor device operating in a memory storage system including a bus. Therefore, it satisfies element [1] of claim 160. (JX0056 at 1, 103, 134, 141; (Nusbaum, Tr. 1551; Jacob, Tr. 5509).

1132. A JEDEC-compliant SDRAM is configured by an external bus controller, such as a central processing unit (CPU). Therefore, it satisfies element [2] of claim 160. (JX0056 at 114-16; Nusbaum, Tr. 1552; Jacob, Tr. 5510).

1133. A JEDEC-compliant SDRAM has pins for connecting the SDRAM to the bus. Therefore, it satisfies element [3] of claim 160. (JX0056 at 106, 141; Nusbaum, Tr. 1552; Jacob, Tr. 5510).

1134. A JEDEC-compliant SDRAM contains a mode register that stores information. Therefore, it satisfies element [4] of claim 160. (JX0056 at 114; (Nusbaum, Tr. 1552-53;

Jacob, Tr. 5510-11).

1135. The information stored in a JEDEC-compliant SDRAM's mode register specifies burst length, burst type and latency mode. (JX0056 at 114). The burst length, burst type and latency mode specify the manner in which the SDRAM responds to transaction requests, i.e., read and write requests. (JX0056 at 114-16, 120, 121). Therefore, a JEDEC-compliant SDRAM satisfies element [5] of claim 160. (Nusbaum, Tr. 1553; Jacob, Tr. 5511-12).

1136. A JEDEC-compliant SDRAM receives burst length, burst type and latency information from the bus and stores it in the mode register "after power-on and before normal operation," when the SDRAM is configured. (J00X56 at 114). Therefore, it satisfies element [6] of claim 160. (Nusbaum, Tr. 1543-54; Jacob, Tr. 5512).

1137. A JEDEC-compliant SDRAM responds to transaction requests (read and write requests) in the manner specified by the burst type, burst length and latency information stored in its mode register. (JX0056 at 114, 120, 121). Therefore, it satisfies element [7] of claim 160. (JX0056 at 114; Nusbaum, Tr. 1554-55; Jacob, Tr. 5512-13).

1138. Claim 160 of the '961 application contains no language requiring a device identifier feature. (Nusbaum, Tr. 1561; Jacob, Tr. 5523).

1139. The '961 application does contain claims that recite a device identifier feature. (CX1504 at 219-223; Nusbaum, Tr. 1562). For example, claim 161 recites "an identification register" which stores "an identification number that uniquely identifies the semiconductor device." (CX1504 at 222). The fact that claim 161 contains this limitation suggests that claim 160 should not be interpreted to require a device identifier feature because proper dependant claims (i.e., claim 161) should be understood as adding limitations to their independent claims (i.e., claim 160). (Nusbaum, Tr. 1562; Fliesler, Tr. 8941).

(B) Claim 164 of the '961 Application

1140. Claim 164 of the '961 application recites:

[1] The semiconductor device of 160,

[2] wherein the register is an access-time register and the information is a value indicative of an access time for the semiconductor device, the semiconductor device being operative to wait for the access time before using the bus

[3] in response to a transaction request specifying the semiconductor device.

(CX1504-223) (numbering added).

1141. An SDRAM compliant with Release 4 of the JEDEC SDRAM standard (JX0056) contains each limitation of claim 164 of the '961 application. (Nusbaum, Tr. 1555).

1142. A reasonable engineer could construe claim 164 to cover the programmable CAS latency features of an SDRAM compliant with Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5523-25).

1143. Because claim 164 is dependant upon claim 160, it includes the limitations of claim 160. (Nusbaum, Tr. 1555). An SDRAM compliant with JEDEC release 4 satisfies the limitations of claim 160, as explained above, and therefore satisfies element [1] of claim 164. (Nusbaum, Tr. 1555).

1144. Paragraph 1144 is unused.

1145. A JEDEC-compliant SDRAM contains a mode register that specifies the CAS latency, which satisfies claim 164's requirement for an "access-time register" and "a value indicative of an access time." (JX0056 at 114). Therefore, the SDRAM satisfies element [2] of claim 164. (Nusbaum, Tr. 1555; Jacob, Tr. 5524).

1146. A JEDEC-compliant SDRAM outputs data in response to a transaction request (a read request) after waiting a time specified by the CAS latency. (JX0056 at 114, 121). A read request specifies the SDRAM through the chip select line. (JX0056 at 21, 121). Therefore, the SDRAM satisfies element [3] of claim 164. (Nusbaum, Tr. 1559-60; Jacob, Tr. 5524-25).

1147. Claim 164 of the '961 application contains no language requiring a device identifier feature. (Nusbaum, Tr. 1562; Jacob, Tr. 5525).

(C) Claim 151 of the '961 Application

1148. Claim 151 of the '961 application recites:

A computer system comprising:

a bus including bus lines for carrying data;

a bus master coupled to the bus; and

a plurality of semiconductor devices coupled to the bus, each semiconductor device comprising:

at least one register operative to store information specifying a manner in which the semiconductor device is to respond to transaction requests received from the bus,

wherein the bus master transmits the information to the semiconductor device via the bus lines of the bus when the bus is configured,

the semiconductor device storing the information received from the bus lines in the register during bus configuration and thereafter responding to transaction requests according to the information stored in the register.

(CX1504 at 218-19).

1149. A reasonable engineer could construe claim 151 of the '961 application to cover a computer system incorporating an SDRAM that complied with Release 4 of the JEDEC SDRAM standard (JX0056). (Jacob, Tr. 5526).

1150. A computer system incorporating an SDRAM that complied with Release 4 of the JEDEC SDRAM standard (JX56) would contain every limitation of claim 151 of the '961 patent. (Nusbaum, Tr. 1565-68).

1151. The limitation of claim 151 "at least one register operative to store information specifying a manner in which the semiconductor device is to respond to transaction requests ..." is similar to limitations of claim 160. A JEDEC compliant SDRAM would satisfy this limitation in claim 151 for the same reasons it satisfies the similar limitation of claim 160. (Nusbaum, Tr. 1567-68).

1152. The scope of claim 151 is similar to the scope of claim 160 of the '961 application in that claim 151 covers a computer system incorporating a memory storage system similar to that recited in claim 160. (Jacob, Tr. 5526).

1153. Claim 151 contains no language referring to a device identifier feature. (CX1504-218-19).

(D) Claim 159 of the '961 Application

1154. Claim 159 of the '961 application recites:

The computer system of 151, wherein the register is an access-time register operative to store a value indicative of an access time for the semiconductor device, the semiconductor device being operative to wait for the access time before using the bus in response to a request specifying the semiconductor device.

(CX1504 at 221).

1155. Claim 159 covers a JEDEC-compliant SDRAM used in a computer system. (Nusbaum, Tr. 1570).

1156. The limitation of claim 159 requiring “an access-time register operative to store a value indicative of an access time for the semiconductor device” is similar to a limitation in claim 164 of the ‘961 application. (Nusbaum, Tr. 1569-70). A JEDEC-compliant SDRAM having a mode register which stores CAS latency information satisfies this limitation. (Nusbaum, Tr. 1570).

1157. Claim 159 contains no language referring to a device identifier feature. (CX1504 at 221).

(E) Claim 165 of the ‘961 Application

1158. Claim 165 of the ‘961 application recites:

In computer system, a method for configuring operation of a semiconductor device coupled to the bus,

coupling a value to the bus by a bus master that it coupled to the bus, the value specifying a manner in which the semiconductor device is to respond to transaction requests after the semiconductor device is configured; and

writing the value to a register of the semiconductor device by the semiconductor device.

(CX1504 at 223).

1159. Claim 165 of the ‘961 application covers the method by which a computer system’s bus master stores information in the mode register of a JEDEC-compliant SDRAM that specifies the manner in which the SDRAM responds to transaction requests. (Nusbaum, Tr. 1570-71).

1160. A reasonable engineer could conclude that claim 165 covers the method of storing CAS latency information in the mode register of an SDRAM, as described Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5527).

1161. A reasonable engineer would conclude that claim 165 covers the method of programming burst length as described Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5527-28).

(F) Claim 168 of the '961 Application

1162. Claim 168 of the '961 Application recites:

The method of claim 165, wherein the value specifies value specifies [sic] an access time for the semiconductor device, the method comprising the further step of the semiconductor device waiting for the access time before using the bus to respond to a transaction request that specifies the semiconductor device.

(CX1504 at 224).

1163. Claim 168 covers the method used with a JEDEC-complaint SDRAM of programming the CAS latency value in the SDRAM's mode register and having the SDRAM wait the CAS latency period before using the bus. (Nusbaum, Tr. 1571-72).

2. The Rambus '490 Patent Application Contained Claims Covering JEDEC-Compliant SDRAM.

1164. Rambus patent application no. 08/469,490 (the '490 application) contained claims covering, or that a reasonable engineer could interpret as covering, a JEDEC-compliant SDRAM, the use of such an SDRAM, and a computer system incorporating a JEDEC-compliant SDRAM. (Nusbaum, Tr. 1573-1578; Jacob, Tr. 5528-32).

1165. Rambus filed the '490 application on June 6, 1995. (CX1504 at 246; Nusbaum, Tr. 1572). The '490 application is a continuation of the '961 application. (Nusbaum, Tr. 1572). Rambus filed claims 183-185 in the '490 application on June 23, 1995. (CX1504 at 258-271; Nusbaum, Tr. 1572-73).

(A) Claim 183 of the '490 Application

1166. Claim 183 of the '490 patent recites:

- [1] A computer system comprising:
a bus; a semiconductor device coupled to the bus,
- [2] the semiconductor device comprising an access-time register operative to store a value indicative of an access time for the semiconductor device;
- [3] a bus master coupled to the bus, the bus master transmitting the value to the semiconductor device via the bus, the semiconductor device storing the value in the access-time register,
- [4] the semiconductor device thereafter being operative to wait for the access time before using the bus in response to a request specifying the semiconductor device.

(CX1504 at 264-65) (numbering added).

1167. Claim 183 covers a computer system incorporating a JEDEC-compliant SDRAM having programmable CAS latency. (Nusbaum, Tr. 1580-81). A reasonable engineer could construe claim 183 of the '490 patent to cover a computer system using a JEDEC-compliant SDRAM. (Jacob, Tr. 5528-30).

1168. A JEDEC-compliant SDRAM operates in a computer system having a bus. Therefore a computer system incorporating a JEDEC-compliant SDRAM satisfies element [1] of claim 183. (JX56 at 164; Jacob, Tr. 5529).

1169. A JEDEC-compliant SDRAM has a mode register which stores CAS latency (access time) information. Therefore a computer system incorporating a JEDEC-compliant SDRAM satisfies element [2] of claim 183. (JX56 at 114; Jacob, Tr. 5529).

1170. A JEDEC-compliant SDRAM has a mode register which stores CAS latency (access time) information which it receives from a bus master over the bus. Therefore a computer system incorporating a JEDEC-compliant SDRAM satisfies element [3] of claim 183. (JX56 at 114; Jacob, Tr. 5529-30).

1171. A JEDEC-compliant SDRAM waits for the CAS latency time before using the bus in response to a read request. Therefore a computer system incorporating a JEDEC-compliant SDRAM satisfies element [4] of claim 183. (JX56 at 114; Jacob, Tr. 5530).

1172. Claim 183 contains no limitation requiring a device identification feature.

(CX1504 at 264-65; Nusbaum, Tr. 1575-77; Jacob, Tr. 5530-31).

(B) Claim 184 of the '490 Application

1173. Claim 184 of the '490 application recites:

[1] A semiconductor device having an access time that is programable, comprising:

[2] at least one pin for coupling the semiconductor device to a bus; and

[3] at least one access-time register operative to store a value indicative of the access time for the semiconductor device, wherein the value is received by the memory device from the bus, the semiconductor device storing the value in the access-time register,

[4] the semiconductor device thereafter being operative to wait for the access time before using the bus in response to a request specifying the semiconductor device.

(CX1504 at 265) (numbering added).

1174. An SDRAM compliant with Release 4 of the JEDEC SDRAM standard (JX56) contains each limitation of claim 184 of the '490 application. (Nusbaum, Tr. 1574-75). A reasonable engineer could construe claim 184 to cover the programmable CAS latency feature of an SDRAM compliant with Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5531).

1175. A JEDEC-compliant SDRAM is a semiconductor device having an access time, CAS latency, that is programable. Therefore, it satisfies element [1] of claim 184. (JX56 at 114; (Nusbaum, Tr. 1574; Jacob, Tr. 5531).

1176. A JEDEC-compliant SDRAM has pins for connecting to the bus. Therefore, it satisfies element [2] of claim 184. (JX56 at 141; Nusbaum, Tr. 1574).

1177. A JEDEC-compliant SDRAM has a mode register which stores a CAS latency value received from the bus. Therefore, it satisfies element [3] of claim 184. (JX56 at 114; Nusbaum, Tr. 1574-75).

1178. The CAS latency (access time) causes a JEDEC-compliant SDRAM to

wait a specified time before using the bus in response to a read request. Therefore, the SDRAM satisfies element [4] of claim 184. (JX56 at 114; Nusbaum, Tr. 1574-75).

1179. Claim 184 contains no limitation requiring a device identification feature. (CX1504 at 265; Nusbaum, Tr. 1577; Jacob, Tr. 5530-31).

(C) Claim 185 of the ‘490 Application

1180. Claim 185 of the ‘490 application recites:

A method for programming an access time of a semiconductor device, comprising:

coupling a value to a bus by a bus master that is coupled to the bus, the value specifying an access time for the semiconductor device;

the semiconductor device receiving the value from the bus;

writing the value to an access-time register of the semiconductor device; and

the semiconductor device thereafter responding to transaction request that specify the semiconductor device by waiting the access time before using the bus.

(CX1504 at 265-66).

1181. Claim 185 covers the method of programming the CAS latency value in the mode register of a JEDEC-compliant SDRAM that is inherent in the operation of the SDRAM. Therefore, claim 185 cover the use of an SDRAM compliant with Release 4 of the JEDEC SDRAM standard. (Nusbaum, Tr. 1576-77). A reasonable engineer could construe claim 185 to cover the use of the programmable CAS latency feature of a JEDEC-compliant SDRAM. (Jacob, Tr. 5531-32).

1182. Claim 185 contains no limitation requiring a device identification feature. (CX1504 at 265-66; Nusbaum, Tr. 1576-77; Jacob, Tr. 5530-31).

3. The Rambus ‘692 Patent Application Contained Claims Covering A Phase-Lock Loop Incorporated Into JEDEC-Compliant SDRAM.

1183. Rambus patent application 07/847,692 (the '692 application) contained claims covering, or that a reasonable engineer could interpret as covering, a phase lock loop (PLL) incorporated into a JEDEC-complaint SDRAM. (Nusbaum, Tr. 1582-95; Jacob, Tr. 5533-41).

1184. Rambus filed the '692 application in the PTO on March 5, 1992 as a divisional application of the '898 application. (CX1502-177; Nusbaum, Tr. 1582). As filed, the '692 application contained claims 73-81 of the original 150 claims submitted with the '898 parent patent application. (CX1502 at 194; Nusbaum, Tr. 1583). However, on June 28, 1993, Rambus filed a Preliminary Amendment in which it canceled claims 73-81 and added new claims 151-165. (CX1504 at 205-213; Nusbaum, Tr. 1584).

(A) Claim 151 of the '692 Application

1185. Claim 151 of the '692 application, as submitted on June 28, 1993, recited:

[1] A memory device residing on a single substrate, comprising:

[2] (A) a memory array for storing data at addresses;

[3] (B) a clock signal receiving circuit coupled to receive an external clock signal for generating a local clock signal for performing memory operations with respect to the memory array;

[4] (C) a phase locked loop (PLL) coupled to the clock signal receiving circuit and the memory array for providing a variable delay to the local clock signal such that the delayed local clock signal is synchronized with the external clock signal received by the clock signal receiving circuit.

(CX1502 at 208) (numbering added).

1186. On September 14, 1994, NEC Corporation made a proposal to JEDEC Committee 42.3 that the SDRAM standard incorporate an on-chip PLL. (JX0021 at 1, 91). The proposal demonstrates the use of a PLL on an SDRAM chip to synchronize an external clock (indicated as CLK) and the internal clock (indicated as ICLK). (JX0021 at 91; Nusbaum, Tr. 1587-88; Jacob, Tr. 5533-34).

1187. A JEDEC-compliant SDRAM that incorporated the NEC on-chip PLL proposal would contain each limitation of claim 151 of the '692 application as set forth in the June 23, 1993 amendment. (Nusbaum, Tr. 1589-93). A reasonable engineer could construe the June 1993 version of claim 151 to cover a JEDEC-compliant SDRAM including a PLL circuit as set

forth in the September 1994 NEC proposal. (Jacob, Tr. 5535).

1188. A JEDEC-compliant SDRAM is a memory device residing on a single substrate. Therefore it satisfies element [1] of claim 151. (Jacob, Tr. 5536; Nusbaum, Tr. 1590).

1189. A JEDEC-compliant SDRAM includes a memory array for storing data at addresses. Therefore, it satisfies element [2] of claim 151. (Jacob, Tr. 5536-37; Nusbaum, Tr. 1590).

1190. A JEDEC-compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal will include “a clock signal receiving circuit” as indicated by the triangle labeled “receiver” in the proposal. The receiver circuit generates a local, internal clock signal, ICLK. (JX0021 at 91; Jacob, Tr. 5537-38). The local clock signal is coupled to the memory array through the output driver that drives data onto the bus, thereby performing memory operations. (JX0021 at 91; Jacob, Tr. 5538). Therefore, a JEDEC-compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal satisfies element [3] of claim 151. (Jacob, Tr. 5538; Nusbaum, Tr. 1590-91).

1191. A JEDEC-compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal will include a PLL which is coupled to the clock signal and to the memory array through the output driver. The PLL delays the local clock signal in order to synchronize it with the external clock signal. Therefore, an SDRAM including the PLL proposal satisfies element [4] of claim 151. (JX0021 at 91; Jacob, Tr. 5538-39; Nusbaum, Tr. 1591-92).

1192. On October 23, 1995, Rambus submitted an amendment to the PTO making minor changes to claim 151, including adding a limitation to the end of claim 151 reciting “wherein the memory array, the clock signal receiving circuit and the PLL all reside on a single semiconductor substrate.” (CX1502 at 233-34; Nusbaum, Tr. 1585-86). The amendments to claim 151 did not significantly change the meaning of the claim. (Jacob, Tr. 5540-41; Nusbaum, Tr. 1593).

1193. A JEDEC-compliant SDRAM that incorporated the September 1994 NEC on-chip PLL proposal would contain each limitation of claim 151 of the ‘692 application as set forth in the October 23, 1995 amendment. (Nusbaum, Tr. 1589-92). An engineer could reasonably construe the October 1995 version of claim 151 to cover a JEDEC-compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal. (Jacob, Tr. 5540-41).

(B) Claim 152 of the ‘692 Application

1194. Rambus submitted claim 152 of the ‘692 application to the PTO on June 23,

1993. Claim 152, which is dependent on claim 151 adds the limitation that “the memory array is a dynamic random access memory (DRAM).” (CX1502 at 208).

1195. Because a JEDEC-compliant SDRAM is a DRAM, claim 152 covers an SDRAM incorporating the NEC on-chip PLL proposal. (Nusbaum, Tr. 1592).

(C) Claim 166 and 167 of the ‘692 Application

1196. In the October 23, 1995 amendment, Rambus added claims 166 and 167 to the ‘692 application. (CX1502 at 233-34). Claim 166 recites “a computer system, comprising: (A) a bus; (B) a bus master coupled to the bus” and a “memory device” having the same features as recited in claim 151 of the ‘692 application. (CX1502 at 234).

1197. Claim 167 is dependent on claim 166. Claim 167 requires that the memory array be “a dynamic random access memory (DRAM).” (CX1502 at 235).

1198. Claims 166 and 167 cover a computer system using a JEDEC-compliant SDRAM incorporating the September 1994 NEC on-chip PLL proposal. (Nusbaum, Tr. 1593-1594).

4. The Rambus ‘646 Patent Application Contained Claims Covering A JEDEC-Compliant SDRAM Incorporating A Proposed Dual-Edge Clocking Feature.

1199. Rambus patent application 08/222,646 (the ‘646 application) contained claims that covered a JEDEC-compliant SDRAM incorporating a proposed dual-edged clocking feature. (Nusbaum, Tr. 1595-1603; Jacob, Tr. 5549-50).

1200. A proposal for a dual-edged clocking scheme appears in JEDEC 42.3 Committee minutes from May 1992. (CX0034 at 32; Jacob, Tr. 5542-43).

1201. The minutes of the December 6, 1995 JEDEC 42.3 Committee meeting report the results of a “SDRAM Feature Survey Ballot.” (JX0028 at 1, 35, 45). Under the heading “Issues with Mixed Support,” the minutes list “Using both edges of the clock for sampling inputs.” (JX0028 at 35). This is a reference to dual-edged clocking. (Jacob, Tr. 5543-44). The minutes also report the results of voting on the question, “Does your company believe that future generations of SDRAM could benefit from BOTH edges of the clock for sampling input?” (JX0028 at 45).

1202. At a March 20, 1996 meeting of JEDEC Committee 42.3, Samsung Corporation made a presentation entitled “Future SDRAM.” (JX0031 at 68-72). The “Proposed Clocking Scheme” of the presentation included the feature “Data in sampled at both edge [sic] of Clock into memory.” (JX0031 at 71). This is a reference to dual-edged clocking. (Jacob, Tr. 5554-

45).

1203. The May 1992, December 1995 and March 1996 proposals for dual edge clocking require controlling memory operations (read and write operations) in an SDRAM, in response to both the rising edge and the falling edge of a clock signal. (Nusbaum, Tr. 1595-96).

1204. Rambus filed the '646 application on March 31, 1994. The '646 application is a continuation of application number 07/954,945, which is a continuation of the '898 application. (CX1493 at 002; Nusbaum, Tr. 1596).

1205. On September 6, 1994, Rambus filed a preliminary amendment in the '646 application that canceled the original claims and added new claims 151 and 152, among others. (CX1493 at 183-201; Nusbaum, Tr. 1597).

(A) Claim 151 of the '646 Application

1206. Claim 151 of the '646 application, as submitted to the PTO on September 6, 1994, recites:

[1] A dynamic random access memory (DRAM) capable of being coupled to a bus, the DRAM comprising:

[2] a first circuit for providing a clock signal;

[3] a conductor for coupling the DRAM to a bus; and

[4] a receiver circuit coupled to the conductor and the first circuit, the receiver circuit for latching information received from the conductor in response to a rising edge of the clock signal and a falling edge of the clock signal.

(CX1493 at 184-85) (numbering added).

1207. Claim 151 of the '646 application covers a JEDEC-compliant SDRAM incorporating the dual edge clocking proposals made to JEDEC in May 1992, December 1995, March 1996. (Nusbaum, Tr. 1595-1603; Jacob, Tr. 5549-50).

1208. An SDRAM is coupled to a bus. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in March 96 would satisfy element [1] of claim 151 of the '646 application. (Nusbaum, Tr. 1602; Jacob, Tr. 5550-51). A JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992 or December 1995 would also satisfy element [1]. (Nusbaum, Tr. 1598, 1602, 1617; Jacob, Tr.

5550-51).

1209. An SDRAM receives an external clock signal through a circuit that provides an internal clock signal. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in March 96 would satisfy element [2] of claim 151 of the '646 application. (Nusbaum, Tr. 1602; Jacob, Tr. 5551). A JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992 or December 1995 would also satisfy element [2]. (Nusbaum, Tr. 1598, 1602, 1617; Jacob, Tr. 5551-52).

1210. An SDRAM will have pins that couple it a bus. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in March 96 would satisfy element [3] of claim 151 of the '646 application. (Nusbaum, Tr. 1602; Jacob, Tr. 5551). A JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992 or December 1995 would also satisfy element [3]. (Nusbaum, Tr. 1598, 1602, 1617; Jacob, Tr. 5551-54).

1211. An SDRAM that samples input data in response to the rising and falling edges of a clock signal must have a receiver circuit that latches data in response to the rising and falling edges of a clock signal. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in March 96 would satisfy element [4] of claim 151 of the '646 application. (Nusbaum, Tr. 1602-03; Jacob, Tr. 5551). A JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992 or December 1995 would also satisfy element [4]. (Nusbaum, Tr. 1598, 1602-03, 1617; Jacob, Tr. 5554-55).

(B) Claim 152 of the '646 Application

1212. Claim 152 of the '646 application, as submitted on September 6, 1994, was dependant on claim 151 and added limitations to "a first input receiver" and "a second input receiver". (CX1493 at 185).

1213. On April 21, 1995, Rambus submitted to the PTO an amendment to the '646 application, which made a minor wording change to claim 151 and added the language of claim 151 to claim 152 so that it claim 152 was no longer dependant on claim 151. (CX1493 at 223-24). Rambus canceled claim 151 on September 14, 1995. (CX1493 at 243). On October 6, 1995, the examiner issued a notice of allowance for the '646 application, which indicated that he had allowed claim 152, among others. (CX1493 at 249).

1214. The '646 application issued as Patent No. 5,513,327 (the '327 patent) to Rambus on April 30, 1996. (CX1494 at 1). Claim 152 of the '646 application issued as claim 1 of the '327 patent. (CX1493 at 223-24; CX1494 at 23).

1215. Claim 152 of the of the '646 application covered the most feasible way to

implement a JEDEC-compliant SDRAM that incorporated the dual-edged clocking feature proposed in May 1992, December 1995 and March 1996. (Jacob, Tr. 5545-47).

5. The Rambus '327 Patent Contains Claims Covering Implementation of A Dual-Edge Clocking Feature in JEDEC-Compliant SDRAM .

1216. Rambus Patent No. 5,513,327 (the '327 patent) contains claims covering the most feasible way to implement the dual-edged clocking feature proposed to JEDEC in May 1992, December 1995 and March 1996 in a JEDEC-compliant SDRAM. (Jacob, Tr. 5545-49; see CX1244 at 1).

1217. The '327 patent also contains claims covering DDR SDRAM as described in JEDEC Specification JESD 79 (June 2000). (Jacob, Tr. 5550-60).

(A) Claim 1 of the '327 Patent Compared to JEDEC Dual-Edged Clocking Proposals

1218. Claim 1 of the '327 patent recites:

- [1] A dynamic random access memory (DRAM), comprising; a first circuit for providing a clock signal;
- [2] a conductor for coupling the DRAM to a bus; and a receiver circuit coupled to the conductor and the first circuit,
- [3] the receiver circuit for latching information received from the conductor in response to a rising edge of the clock signal and a falling edge of the clock signal,
- [4] wherein the receiver circuit comprises:
 - a first input receiver coupled to the conductor and the first circuit, the first input receiver for latching information provided by the bus via the conductor in response to the rising edge of the clock signal; and
 - a second input receiver coupled to the conductor and the first circuit, the second input receiver for latching information from the bus in response to the falling edge of the clock signal.

(CX1494 at 23) (numbering added).

1219. An engineer could reasonably construe claim 1 of the '327 patent to cover a JEDEC-compliant SDRAM that incorporated the dual-edged clocking feature of the May 1992 (CX0034 at 32) and March 1996 (JX0031 at 71) proposals or the December 1995 survey ballot (JX0028 at 35). (Jacob, Tr. 5545).

1220. An SDRAM uses an external clock signal for generating an internal clock signal. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [1] of claim 1 of the '327 patent. (Jacob, Tr. 5545-46; JX0056 at 124).

1221. An SDRAM uses a pin for connecting to a bus and has a clock pin coupled to a clock receiver circuit. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [2] of claim 1 of the '327 patent. (Jacob, Tr. 5545-46; JX0056 at 106).

1222. An SDRAM having a dual-edged clocking feature will latch data in response to the rising edge and falling edge of a clock. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [3] of claim 1 of the '327 patent. (Jacob, Tr. 5546).

1223. The only way for an SDRAM having a dual-edged clocking feature that latches data in response to the rising edge and the falling edge of a clock is to use two receivers, one which latches data in response to a rising edge and one which latches data in response to a falling edge. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edged clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [4] of claim 1 of the '327 patent. (Jacob, Tr. 5546-47).

(B) Claim 1 of the '327 Patent Compared to the JEDEC DDR SDRAM Standard

1224. An engineer could reasonably construe claim 1 of the '327 patent to cover a DDR SDRAM as described in the JESD 79 specification dated June 2000 (JX57). (Jacob, Tr. 5551-52).

1225. Circuits on DDR SDRAM provide clock signals. Therefore a DDR SDRAM satisfies element [1] of claim 1 of the '327 patent (Jacob, Tr. 5552-53; JX0057 at 8).

1226. A DDR SDRAM includes pins to couple the DRAM to a bus. The DDR SDRAM has a circuit including two input registers that acts as the receiver circuit for data. Therefore a DDR SDRAM satisfies element [2] of claim 1 of the '327 patent (Jacob, Tr. 5552-53; JX0057 at 8).

1227. A DDR SDRAM will latch data for inputs (writes) in response to the rising edge and falling edge of the data strobe (DQS), which is a clock signal. Therefore a DDR SDRAM satisfies element [3] of claim 1 of the '327 patent (Jacob, Tr. 5553-54; JX0057 at 32).

1228. A DDR SDRAM includes two input registers, which are input receivers, one of which latches data in response to the rising edge of DQS, and one of which latches data in response to the falling edge of (DQS, which is a clock signal. Therefore a DDR SDRAM satisfies element [4] of the '327 patent (Jacob, Tr. 5554-55; JX0057 at 8).

(C) Claim 7 of the '327 Patent Compared to JEDEC Dual-Edged Clocking Proposals

1229. Claim 7 of the '327 patent recites:

[1] A dynamic random access memory (DRAM), comprising;

a first circuit for providing a clock signal;

[2] a conductor for coupling the DRAM to a bus; and

[3] a multiplexer coupled to the first circuit, the multiplexer having an output, a first input, and a second input;

a first output line coupled to the first input of the multiplexer, wherein the multiplexer couples the first output line to the output of the multiplexer in response to a rising edge of the clock signal; and

a second output line coupled to the second input of the multiplexer, wherein the multiplexer couples to the second output line to the output of the multiplexer in response to a falling edge of the clock signal.

(CX1494 at 23) (numbering added).

1230. An engineer could reasonably construe claim 7 of the '327 patent to cover a JEDEC-compliant SDRAM that also incorporated the dual-edged clocking feature of the May 1992 (CX0034 at 32) and March 1996 (JX0031 at 71) proposals or the December 1995 survey ballot (JX0028 at 35). (Jacob, Tr. 5547-48).

1231. An SDRAM uses an external clock signal for generating an internal clock signal. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature

proposed in May 1992, December 1995 or March 1996 would satisfy element [1] of claim 7 of the '327 patent. (Jacob, Tr. 5548; JX0056 at 124)).

1232. An SDRAM uses a pin for connecting to a bus. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed to in May 1992, December 1995 or March 1996 would satisfy element [2] of claim 7 of the '327 patent. (Jacob, Tr. 5548; JX0056 at 106).

1233. The most reasonable way for an SDRAM having a dual-edged clocking feature to output data on the rising and falling edge of a clock signal is to toggle between two output drivers using a multiplexer. Therefore, a JEDEC-compliant SDRAM that used the most reasonable method to incorporate the dual-edge clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [3] of claim 7 of the '327 patent. (Jacob, Tr. 5548-49).

(D) Claim 7 of the '327 Patent Compared to the JEDEC DDR SDRAM Standard

1234. An engineer could reasonably construe claim 7 of the '327 patent to cover a DDR SDRAM as described in the JESD 79 specification dated June 2000 (JX57). (Jacob, Tr. 5556-60).

1235. Circuits on DDR SDRAMs provide clock signals. Therefore a DDR SDRAM satisfies element [1] of claim 7 of the '327 patent (Jacob, Tr. 5557; JX0057 at 8).

1236. A DDR SDRAM includes pins to couple the DRAM to a bus. Therefore a DDR SDRAM satisfies element [2] of claim 7 of the '327 patent (Jacob, Tr. 5557-58; JX0057 at 8).

1237. A DDR SDRAM has a multiplexer that is coupled to a clock. The multiplexer has two output lines which allows the DDR SDRAM to output data in response to the rising edge and the falling edge of a clock signal. Therefore a DDR SDRAM satisfies element [3] of claim 7 of the '327 patent. (Jacob, Tr. 5558-60; JX0057 at 08, 22).

D. Rambus Was Successful In Concealing Its Claim To Intellectual Property Rights To JEDEC Standard Technology.

1. During the Time It was a Member of JEDEC and Thereafter, Rambus Promoted Its Proprietary RDRAM Technology And Concealed Its Intellectual Property Claims to JEDEC Standard Technology.

1238. Throughout the period of its membership in JEDEC and thereafter, Rambus

pursued a strategy of actively promoting its proprietary RDRAM technology to companies who were in a position to manufacture memory chips or related chipsets. (See Crisp, Tr. 2931; CX0543A at 7-8).

1239. Rambus efforts to promote adoption of its proprietary RDRAM technology included making presentations concerning the proprietary technology to memory chip manufacturers and other firms. (E.g. CX2107 at 63 (Oh, Dep.); Bechtelsheim, Tr. 5818-19; G. Kelley, Tr. 2537; Kellogg, Tr. 5052-53). In connection with such efforts, Rambus commonly entered into non-disclosure agreements (“NDAs”) that prohibited the firms from disclosing information concerning the proprietary Rambus technology to others without the consent of Rambus. (E.g. Bechtelsheim, Tr. 5818-19; Rhoden, Tr. 521; Kellogg, Tr. 5052-53).

1240. The focus of these presentations was on the advantages Rambus saw of the proprietary RDRAM technology and the unique characteristics of that technology, including its unique bus architecture. (E.g., G. Kelley, Tr. 2533-34; Sussman, Tr. 1429-31). Rambus’ presentations of the RDRAM technology in the 1992-93 time frame involved a DRAM with a multiplexed bus, meaning that various signals were combined on a single line. (CX2114 at 61-62 (Karp, Dep.)). Joel Karp, who was with Samsung at the time, viewed the Rambus RDRAM as “more revolutionary than evolutionary.” (CX2114 at 63 (Karp, Dep.)). Craig Hampel, Rambus technical director who since 1993 participated in numerous meetings and presentations with DRAM manufacturers and other firms to discuss Rambus technology (Hampel, Tr. 8672, 8729-31), was not aware of any instance in which Rambus representatives told the DRAM manufacturers which aspects of RDRAM were Rambus inventions, or were protected by Rambus patents or patent applications. (Hampel, Tr. 8732-33).

1241. Rambus President David Mooring testified that the first time Rambus ever advised any SDRAM manufacturer that Rambus had claims covering features of SDRAMs was Hitachi in late 1999 or early 2000. (CX2079 at 157-58; see also CX2098 at 442-43 (Mooring, Dep.); see also CX2112 at 171-72 (Mooring, FTC Depo.)). Slides used by Rambus in presentations to Rambus customers would “definitely not have put anybody on notice” of the coverage of patents but would only have generic information about aggregate numbers of Rambus patents and/or patent applications. (CX2112 at 180 (Mooring, Dep.)).

1242. Gary Harmon, former Rambus Chief Financial Officer, was involved in negotiating RDRAM licenses for Rambus in the 1993-96 time frame. (CX2070 at 42 (Harmon, Dep.)). Mr. Harmon recalled being involved in discussions with Oki, Fujitsu, Toshiba and NEC from Japan; LG, Hyundai and Samsung from Korea; and Intel, LSI Logic, IBM, Texas Instruments, and Cirrus Logic from the United States, among others. (CX2070 at 42-43 (Harmon, Dep.)). Mr. Harmon did not recall any discussions on the scope or extent of Rambus patents during these negotiations. (CX2070 at 42 (Harmon, Dep.)).

1243. When asked, Mr. Harmon did not tell any of these companies that Rambus might

have patents extending beyond RDRAM. (CX2070 at 45-46 (Harmon, Micron Dep.)). Specifically, Mr. Harmon testified that:

I don't believe we ever specifically stated that we had intellectual property that applied to – outside of the Rambus-compatible area.

(CX2070 at 47 (Harmon, Dep.)). Mr. Harmon also was unaware from discussions with others at Rambus (excluding any privileged communications with counsel) that others had discussions with potential licensees that Rambus technologies might cover SDRAM as well as RDRAM. (CX2070 at 60-61 (Harmon, Dep.)).

1244. Howard Sussman, who participated in JEDEC since 1979 as representative for NEC and later Sanyo Semiconductor (Sussman, Tr. 1321-22), first learned about Rambus through a presentation made by a Rambus employee in 1991. (Sussman, Tr. 1429). The content of the presentation focused on what were portrayed as the key features of the Rambus RDRAM, which included the use of a low-voltage CMOS driver and packetized input/output (*Id.* at 1430-31). The presentation did not discuss PLL/DLL, programmable mode register, programmable CAS latency or burst length, or dual edge clock technology. (*Id.* at 1431, 1435-36).

1245. No one from Rambus ever suggested to Mr. Sussman that the SDRAM that he and others were standardizing at JEDEC used proprietary Rambus technology, or that Rambus intellectual property rights extended outside the RDRAM architecture. (Sussman, Tr. 1454-55). Mr. Sussman first learned that Rambus was taking the position that its technology covered products outside the RDRAM architecture in late 1999 when news of Rambus patent litigation started to show up in the trade press. (Sussman, Tr. 1455).

1246. In April 1992, Gordon Kelley of IBM attended a presentation by Rambus at IBM comparing the proprietary Rambus RDRAM technology with SDRAM. (G. Kelley, Tr. 2537). Following that presentation, Mr. Kelley believed that the Rambus RDRAM was fundamentally different from the SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM or JEDEC. (G. Kelley, Tr. 2537-38, 2546).

1247. Prior to the May 1992 JEDEC 42.3 Committee meeting, Mr. Crisp of Rambus had a conversation with Gordon Kelley of IBM about the possibility of Rambus making a presentation at a JEDEC committee meeting, in which Mr. Kelly explained the JEDEC patent disclosure and licensing policies. (See CCF 907). On the basis of that conversation, Mr. Kelly understood that there was intellectual property on the Rambus proprietary RDRAM technology that he believed Rambus wished to present to JEDEC; Mr. Kelly's understanding was that the intellectual property in issue applied only to the Rambus RDRAM technology. (G. Kelley, Tr. 2504).

1248. Through the time that he left JEDEC in 1998 (Kelley, Tr. 2383), Rambus never indicated to Gordon Kelley of IBM that it might have patent rights over on-chip PLL/DLL or dual edge clock technology. (G. Kelley, Tr. 2593).

1249. Desi Rhoden was employed at Hewlett Packard when he began to learn about the Rambus technology in the early 90's. (Rhoden, Tr. 396). Rambus came to HP to give a presentation about their new memory that they were developing. (*Id.*). The presentation was made pursuant to a non-disclosure agreement between Rambus and HP. (Rhoden, Tr. 521). Although Rambus did not say anything at that presentation about pending Rambus patent applications, though Rhoden assumed that Rambus probably did have patent applications. (Rhoden, Tr. 521). Rambus never suggested that its proprietary technology extended outside the RDRAM architecture, and did not make any statement to suggest that the SDRAM technology being standardized by JEDEC used Rambus intellectual property. (Rhoden, Tr. 521-22).

1250. Andreas Bechtelsheim, who at the time was Vice-President for technology at Sun (Bechtelsheim, Tr. 5752), participated in the development of the SDRAM standard before and during the time that Sun was a member of JEDEC. (*Id.* at 5779). At the time the SDRAM standard was developed, Mr. Bechtelsheim had no understanding that there would be a royalty associated with the programmable CAS latency or programmable burst length features. (Bechtelsheim, Tr. 5813-14). Mr. Bechtelsheim's understanding, based on presentations and discussions with Rambus, was that Rambus had patent rights that covered its proprietary RDRAM technology; Rambus did not suggest that their patents extended to SDRAM or other memory architectures. (Bechtelsheim, Tr. 5828-29; 5841-42).

1251. Andreas Bechtelsheim, who had participated in the development of the SDRAM standard as an executive of Sun, learned from press reports in 2000, when he was an employee of Cisco Systems, that Rambus had begun to enforce patents against SDRAM and DDR products. (Bechtelsheim, Tr. 5880). Mr. Bechtelsheim was surprised at the news, because the JEDEC standards had been developed in an open standards process that had a history of making choices that were not encumbered by proprietary patents or royalties. (*Id.*). Before learning of this through press reports in 2000, Mr. Bechtelsheim had not heard any rumor or suggestion that Rambus might have patents that would extend to SDRAM or DDR. (*Id.* at 5880-81).

1252. Thomas Landgraf was JEDEC representative for Hewlett Packard at the time that JEDEC was considering the JEDEC DDR standard. (Landgraf, Tr. 1708). At the time he was participating in JEDEC and considering the DDR standard, Mr. Landgraf was unaware of any patents or patent applications on the on-chip PLL or dual-edge clock features. (Landgraf, Tr. 1710-11). As Hewlett Packard's representative at JEDEC, Mr. Landgraf had an expectation that the DDR standards on which he was voting for Hewlett Packard would be free of undisclosed patents. (Landgraf, Tr. 1712). Mark Kellogg, who served as an alternate and later principal representative for IBM to the JEDEC 42.3 Committee (Kellogg, Tr. 5017), first learned about Rambus technology through a presentation by Rambus to IBM in the early 1990's. (Kellogg, Tr.

5052-53). At that time, Mr. Kellogg expected that any Rambus patent activity would be associated with the Rambus proprietary RDRAM product that they were showing to IBM, which was a narrow I/O, high-bandwidth, packetized memory device or card with a loop-back structure and a few other elements. (Kellogg, Tr. 5053). At the presentations by Rambus to IBM, no one from Rambus ever suggested that the Rambus proprietary technology extended outside the RDRAM architecture. (Kellogg, Tr. 5054).

1253. Rambus made a presentation to representatives of Micron in 1995 in connection with discussions between Micron and Rambus about licensing the RDRAM technology. (Lee, Tr. 6605). In preparation for that 1995 meeting, Micron employee Terry Lee reviewed with other Micron employees abstracts of the patents that Rambus had been granted to that time. (Lee, Tr. 6605-08). The intended scope of the review included any prior art pertaining to the patent, as well as the breadth of the patent – that is, whether the patent applied to more than just Rambus. (Lee, Tr. 6608-09; CX0629). In some instances, including the Rambus ‘703 patent, the text of the patent itself was reviewed. (Lee, Tr. 6609). Based on his review of Rambus patents in 1995, Mr. Lee and his Micron colleagues concluded that the Rambus patents applied specifically to the RDRAM bus architecture, and reported this conclusion to their supervisor at Micron. (Lee, Tr. 6610-11). Micron chose not to take a license from Rambus in 1995. (Lee, Tr. 6613).

1254. Officials of AMD only learned in 2000 that Rambus claimed patent rights in the JEDEC standard memory technology used by AMD. (Polzin, Tr. 3987; Heye, Tr. 3730).

1255. Through the 1990's, firms in the computer memory industry continued to believe that the JEDEC standards for SDRAM and DDR were open standards that could be used free of royalty payments to Rambus or anyone else. (See, e.g., CCFF 1256-58).

1256. An internal strategic document of Infineon from 1999, comparing the advantages and disadvantages of the RDRAM, SDRAM and DDR memory architectures, describes Rambus with the notation “proprietary standard of Rambus/Intel=>payment of royalties” and shows opposite that a notation for “Double Data Rate” that states “Open standard=>no royalties.” (CX2451 at 9; see also *id.* at 13 (table listing DRAM as SDRAM and DDR as “open standards” in contrast to RDRAM); Peisl, Tr. 4430-31). (See also CX2435 at 23; CX2442 at 36).

1257. An internal strategic document of Hyundai from 1997 lists as one of the “Strong Points” for DDR SDRAM that it is the “most cost effective next generation DRAM” in part because of its “open architecture without royalties or fees.” (CX2294 at 15; see also *id.* at 16 (listing a disadvantage of Rambus “cost due to proprietary design”). (See also CX2297 at 79, 80 (Hyundai, August 1997); CX2264 at 42 (Hyundai, Nov. 1997) (“open standard spec: Direct RDRAM poor, DDR good”); CX2303 at 16, 18 (Hyundai, Feb. 1998) (“Direct Rambus Royalty,” DDR SDRAM: “Open Standard (JEDEC)”); CX2334 at 10, 25, 27 (Hyundai, April 1999) (advantages of DDR SDRAM include “open industry spec”)).

1258. An internal strategic document of Micron from May 1999 compared RDRAM with SDRAM architecture and concluded “Rambus Cost Remains An Issue” in part because of “Extra royalty cost vs. SDRAM.” (CX2737 at 56).

1259. As late as December 1999, Rambus refused to state publicly whether JEDEC standard technology infringed its intellectual property. In an internal email at that time, Rambus CEO Tate noted that Rambus representatives, in a securities analyst conference call, had been asked directly “does DDR infringe your IP?” (CX1089). In response, the company had said that it was analyzing actual memory chip parts to make that determination, and expected to release the results in the first fiscal quarter. (*Id.*) Mr. Tate directed employees who were asked the same question to confine themselves to the same response, and stated “it’s important NOT to indicate/hint/wink/etc what we expect the results of our analysis to be!!!” (*Id.*).

2. Firms With Concerns About Rambus Intellectual Property Claims Came to Believe That Their Suspicions Were Unfounded.

1260. IBM and Siemens in early 1992 had concerns that Rambus might have intellectual property rights with respect to the dual-bank design that was then under consideration by JEDEC in connection with the proposed SDRAM standard. (See CCFF 903-04). However, by the time of the July 1992 meeting of the Committee, at which votes were taken on a number of ballots pertaining to the SDRAM standard, Mr. Kelly of IBM did not understand that Rambus might have any patent rights related to the ballots under consideration. (G. Kelley, Tr. 2562).

1261. Willi Meyer of Siemens was a JEDEC member who in early 1992 had concerns that Rambus might have intellectual property rights with respect to the dual-bank design that was then under consideration by JEDEC in connection with the proposed SDRAM standard. (See CCFF 903-904). However, in late 1993, after reviewing the Rambus WIPO patent application and witnessing Mr. Crisp’s disclosure of the Rambus ‘703 patent to JEDEC in September 1993, Mr. Meyer of Siemens made an internal report to colleagues at Siemens concerning the status of the JEDEC SDRAM efforts in which he stated that by adopting the SDRAM standard JEDEC had managed to define a public domain version of an improved next generation DRAM – that is, a standard in which nothing was covered by someone’s intellectual property. (CX2089 at 151-52 (Meyer, Infineon Trial Tr.)).

1262. Rambus email traffic in 1997 confirms that Siemens continued to believe that the JEDEC standards were free of patent claims. (CX0939 at 1 (Mooring: “We have not told Siemens that we think SDRAM and SDRAM-DDR infringe our patents. We think that will just irritate them.”); see also CX0939 at 1 (“We are hoping that they will either drop their competitive efforts or discover for themselves that they have violated Rambus patents ...”)).

1263. Rambus CEO Tate confirmed in sworn testimony in 2001 that at no time from 1990 until 2000 did Rambus tell Siemens or Infineon that Rambus patents covered their

SDRAM products or their DDR products. (CX2088 at 75-77 (Tate, Infineon Trial Tr.)). Rambus in June 2000 accused Infineon of patent infringement in connection with its production of SDRAM and DDR products. (CX1127).

1264. Hyundai entered into a license agreement with Rambus in December 1995. (CX1589 (letter of intent); CX1599, CX1600 (license agreement); CX2107 at 65-66 (Oh, Dep.)). At the time that Hyundai negotiated its license with Rambus in 1995, Hyundai did not believe that Rambus might have patents or patent applications that extended outside the scope of RDRAM. (CX2107 at 69 (Oh, Dep.)). However, Hyundai negotiated a provision in its 1995 license agreement with Rambus that would have permitted Hyundai to use the licensed Rambus intellectual property rights in connection with “Other DRAM,” that is, DRAM chips other than Rambus proprietary RDRAM. (CX1599 at 3, 12). The reason for this provision was to provide an “insurance program” for concerns by Hyundai that Rambus might have intellectual property claims pertaining to the SyncLink technology, which was being developed by a group in which Hyundai was participating. (CX2107 at 75-77, 94-96, 99, CX2108 at 274-78 (Oh, Dep.)). At the time, Hyundai did not know what patent rights Rambus might have, and the general terms of the provision were acceptable to Hyundai as a way of providing for the possibility that Rambus might assert intellectual property claims against SyncLink. (CX2107 at 75-77 (Oh, Dep.)).

1265. Despite the existence of a provision in its Rambus license agreement that would have given it the general right to use Rambus technology for a specified royalty rate in connection with non-RDRAM compatible products, Hyundai’s strategic documents continuing until at least 1999 show that Hyundai believed that JEDEC standard SDRAM and DDR technologies were open and not subject to royalty payment. (CX2294 at 15, 16; CX2297 at 79, 80; CX2264 at 2; CX2303 at 16, 18; CX2334 at 10, 25, 27). Rambus in June 2000 accused Hyundai of patent infringement in connection with its production of SDRAM and DDR products. (CX1129).

3. Review Of Public Patent Documents Known to JEDEC Members Would Not Have Placed A Reasonable Practitioner on Notice of Claims by Rambus to JEDEC Standard Technology.

(A) The Original Rambus ‘898 Patent Application, Which Described The Basic Rambus Invention, Was the Basis for Several Rambus Patents or Applications That Became Matters of Public Record.

1266. The description of the basic Rambus invention contained in the specification portion of the original ‘898 patent application was the basis for several documents that were publicly available and known to JEDEC members during the time that Rambus was a JEDEC member. (See CCF 1267). However, JEDEC members who reviewed these documents did not conclude that Rambus claimed or could claim intellectual property rights to the JEDEC

standards. (CCFF 1273-76). Moreover, a reasonable engineer reviewing public patent documents in the early to mid-1990's would not have understood that Rambus claimed or could claim rights to the JEDEC Standards. (CCFF 1266 et seq.).

1267. Rambus filed an International Patent Application under the Patent Cooperation Treaty (the PCT application) on April 16, 1991. (CX1454 at 1). The PCT application claimed priority based on Rambus' '898 U.S. application. (CX1454 at 1). The PCT application has the legal effective filing date of the '898 application, April 18, 1990. (CX1454 at 1; Fliesler, Tr. 8884). The PCT application was published on about October 31, 1991, and thereafter available to the public. (CX1454 at 1). It contains the original text, drawings and 150 original claims of the '898 U.S. application. (CX1454; CX1451).

1268. The PCT application would not have alerted a reasonable engineer that Rambus claimed or could claim patent rights over features in JEDEC-compliant SDRAMs and DDR SDRAMs because language in that application, deriving from the Rambus United States '898 application, described a bus architecture that is narrow, multiplexed, packetized and lacking a chip-select network. The bus architecture of a JEDEC-compliant SDRAM does not meet any of these criteria. (Jacob, Tr. 5460-5501; see CCFF 1283 et. seq.).

1269. Rambus patent 5,243,703 (the '703 patent) issued September 7, 1993. (CX1460 at 1). The '703 patent claims priority to the '898 application. The '703 patent issued from a divisional application of the '898 application. (CX1460 at 1). The specification and drawings of the '703 patent are substantially the same as the specification and drawings of the '898 specification and drawings. (CX1460; CX1451; Jacob, Tr. 5500-01). In September 1993, Rambus JEDEC representative Richard Crisp notified the JEDEC JC 42.3 Committee that the '703 patent had issued to Rambus. (CCFF 971-73).

1270. The '703 patent would not have alerted a reasonable engineer that Rambus claimed or could claim patent rights over features in JEDEC-compliant SDRAMs and DDR SDRAM because language in that issued patent, deriving from the Rambus United States '898 application, described a bus architecture that is narrow, multiplexed, packetized and lacking a chip-select network. The bus architecture of a JEDEC-compliant SDRAM does not meet any of these criteria. (Jacob, Tr. 5460-5501). Moreover, the claims contained in the '703 patent recite particular features that are not contained in the JEDEC standards. (Jacob, Tr. 5492-93, 5497, 5498-99; see CCFF 1351-55).

1271. At the time that Rambus withdrew from membership from JEDEC, it submitted with its withdrawal letter dated June 17, 1996, a list of issued patents. (CX0887 at 2; CCFF 1109-14). The list was not a complete list of issued patents because the '327 patent was not on the list. (CX0888 at 2; Crisp, Tr. 3381, 3384; Diepenbrock, Tr. 6200).

1272. None of the patents listed in the Rambus JEDEC withdrawal letter would have

alerted a reasonable engineer in the 1990s that Rambus might be able to obtain patent rights over features incorporated in the JEDEC SDRAM or DDR SDRAM standards. (Jacob, Tr. 5502). Each patent on the list is either restricted to a narrow, packetized, multiplexed bus architecture, addresses topics outside the scope of the JEDEC 42.3 committee, or relates to only minor implementation details of material that could have been within the scope of the 42.3 committee. (Jacob, Tr. 5502; see CCF 1356-57).

(B) JEDEC Members Who Reviewed Publicly Available Rambus Patent Documents Did Not Conclude That Rambus Claimed Rights To the SDRAM or DDR Technologies Under Discussion at JEDEC.

1273. Howard Sussman, who participated in JEDEC since 1979 as representative for NEC and later Sanyo Semiconductor (Sussman, Tr. 1321-22), reviewed the European patent application of Rambus in 1992 or 1993. (Sussman, Tr. 1445). His review, which consisted in large part of flipping through the document and looking over the diagrams, led him to conclude that the application resembled the presentation that he had earlier received from Rambus concerning proprietary RDRAM technology. (Sussman, Tr. 1450-51). At the time of his review in 1992 or 1993, Mr. Sussman did not see anything that he believed put him on notice that Rambus might have intellectual property claims on programmable burst length, programmable CAS latency, on-chip PLL or DLL, or dual edge clock technology. (Sussman, Tr. 1451-54).

1274. According to the Rambus JEDEC representative Richard Crisp, at the May 1992 JC 42.3 Committee meeting, Howard Sussman of NEC commented to the group that he had seen a copy of a Rambus international patent application. (CX2092 at 128 (Crisp, Infineon Trial Tr.)). The essence of the comment was that Mr. Sussman had obtained a copy of the application from the foreign patent office, had read it, and said it should not be a concern for the JEDEC standardization effort. (CX2092 at 129 (Crisp, Infineon Trial Tr.)). Mr. Crisp was there, heard the comment, and didn't say anything different. (CX2092 at 130 (Crisp, Infineon Trial Tr.)).

1275. Willi Meyer of Siemens was a JEDEC member who in early 1992 had concerns that Rambus might have intellectual property rights with respect to the dual-bank design that was then under consideration by JEDEC in connection with the proposed SDRAM standard. (See CCF 903-04). However, in late 1993, after reviewing the Rambus international patent application and witnessing Mr. Crisp's disclosure of the Rambus '703 patent to JEDEC in September 1993, Mr. Meyer of Siemens made an internal report to colleagues at Siemens concerning the status of the JEDEC SDRAM efforts in which he stated that by adopting the SDRAM standard JEDEC had managed to define a public domain version of an improved next generation DRAM – that is, a standard in which nothing was covered by someone's intellectual property. (CX2089 at 151-52 (Meyer, Infineon Trial Tr.)).

1276. In connection with discussions between Micron and Rambus about licensing the

RDRAM technology in 1995 (Lee, Tr. 6605-05), Micron employees reviewed abstracts of the patents that Rambus had been granted to that time. (Lee, Tr. 6606-08). The intended scope of the review included any prior art pertaining to the patent, as well as the breadth of the patent – that is, whether the patent applied to more than just Rambus. (Lee, Tr. 6609; CX0629). In some instances, including the Rambus ‘703 patent, the text of the patent itself was reviewed. (Lee, Tr. 6609). Based on this review of Rambus patents, the Micron employees concluded that the Rambus patents applied specifically to the RDRAM bus architecture, and reported this conclusion to their supervisor at Micron. (Lee, Tr. 6610-11).

(C) A Reasonable Engineer Reviewing Public Patent Documents in the Early to Mid-1990's Would Not Have Understood that Rambus Claimed Rights to JEDEC-Standard Technology.

1277. The main parts of a patent or patent application are the specification, which is the written description of the claimed invention, and the claims, which are statements that define the boundaries of an applicant's right to exclude others from making, using or selling. (Nusbaum, Tr. 1496-97).

1278. The content of claims in a pending patent application can provide information beyond that provided by the application’s specification. (Fliesler, Tr. 8894-96, 8900-01). There can be a gap between all the claims that a patent application could support, on the one hand, and the claims that the patent applicant actually files, on the other hand. (Fliesler, Tr. 8897-90). There are many reasons that a patent applicant might not pursue all the claims that a patent specification hypothetically could support. (Fliesler, Tr. 8901). Moreover, information as to how a patent applicant interprets its claims in pending applications is valuable information to a competitor that is not available from the application’s specification or the claims themselves. (Fliesler, Tr. 8901-02).

1279. Rambus filed patent application serial no. 07/510,898 (the ‘898 application) in the U.S. Patent and Trademark Office (PTO) on April 18, 1990. (CX1451 at 001-02; Nusbaum, Tr. 1507; see DX0014). Various patents or patent applications, some known to JEDEC members during the time Rambus was a JEDEC member or at the time Rambus withdrew from its membership in JEDEC, contained the specification of the original ‘898 application. (CCFF 730-31, 1342-43, 1351-52). However, as discussed below, the claims in each of these patents or patent applications differed from each other.

1280. An engineer or patent lawyer could not have known for certain what claims Rambus would pursue in the ‘898 family from reading the ‘898 application, or the identical PCT application. (Fliesler, Tr. 8902).

1281. For the reasons set forth below, the description of the inventions contained in the specification set forth in the basis ‘898 application and reproduced in substance as the

specification in each of the patents or patent applications deriving from the '898 application would not have alerted a reasonable engineer that Rambus claimed patent rights over features in JEDEC-compliant SDRAMs and DDR SDRAMs. (CCFF 1283 et seq.).

1282. For the reasons set forth below, the claims contained in each of the Rambus patents or patent applications known to JEDEC members during and immediately after Rambus was a member of JEDEC would not have alerted a reasonable engineer that Rambus claimed patent rights over features in JEDEC-compliant SDRAMs and DDR SDRAMs. (CCFF 1341 et seq.).

(1) The Patent Specification Describing the Basic Rambus Inventions.

1283. The '898 patent application included a descriptive portion, called the "specification," that was 62 pages long and included 15 original drawings. (CX1451 at 3-63, 140-150; Nusbaum, Tr. 1496-97).

The Narrow, Multiplexed Bus of the '898 Specification

1284. The '898 specification describes a narrow, multiplexed bus structure having no chip-select line as the "present invention." (CX1451 at 9-10, 14; Jacob, Tr. 5461-63; Nusbaum, Tr. 1642-43).

1285. The first paragraph of the "Summary of Invention" section of the '898 specification characterizes the "present invention" as having a bus that includes:

a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

(CX1451 at 9).

1286. The "Summary of Invention" section also describes the bus: "[i]n the system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data over the same bus." (CX1451 at 10).

1287. The specification describes Figure 2 (CX1451 at 130) in the "Summary of Invention" section and states, "[t]he new bus includes clock signals, power and multiplexed

address, data and control signals.” (CX1451 at 9-10). Figure 2 of the ‘898 specification depicts the bus organization described in the specification. (Jacob, Tr. 5470).

1288. Figure 2 (CX1451 at 130) shows eight multiplexed bus lines that each carry address, control and data information. (Jacob, Tr. 5471). Figure 2 shows that all components in the system share the bus lines. There are no point-to-point connections traveling from the bus master to only one component. (Jacob, Tr. 5471). Figure 2 does not show a chip-select line. (Jacob, Tr. 5472).

1289. The “Summary of Invention” section of the ‘898 specification states, “[p]ersons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention. (CX1451 at 10). The specification does not state that a bus having more bus lines than the number of bits in an address may be used to implement the teaching of the invention. (CX1451). The specification does not state that a bus having dedicated address, control and data lines may be used to implement the teaching of the invention. (CX1451).

1290. The first paragraph of the “Detailed Description” section of the ‘898 specification states:

The present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system. . . . The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus. In many systems using the present invention, the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines. Using the organization described herein, very large addresses (40 bits in the preferred implementation) and large data blocks (1024) bytes) can be sent over a small number of bus lines (8 plus one control line in the preferred implementation).

(CX1451 at 13-14).

1291. The description of the bus in the ‘898 specification as having “substantially fewer bus lines than the number of bits in a single address” indicates that the bus will have relatively few lines and be narrow. For instance, if an address requires 24 bits, the bus will have substantially fewer lines than 24. (Jacob, Tr. 5463-64).

1292. The bus used with a JEDEC-compliant SDRAM does not have “substantially fewer bus lines than the bits in a single address.” A typical SDRAM bus has over 100 lines and is wider than the number of bits in the address. (Rhoden, Tr. 401; Jacob, Tr. 5464).

1293. The term “multiplexed” means that at different times different classes of information are transmitted over the same wires. The bus lines described in the ‘898 specification are multiplexed because each can carry address, data and control signals at different times. (Jacob, Tr. 5464-65).

1294. The subsection of the “Detailed Description” section of the ‘898 specification entitled “Bus” describes a bus architecture having eight “BusData” lines that are multiplexed to carry address, control and data information. This subsection describes no other bus architecture. (CX1451 at 20-21).

1295. The bus used with a JEDEC-compliant SDRAM has dedicated address lines, dedicated data lines and dedicated control lines. The dedicated lines carry only one type of information. The bus lines used with a JEDEC-compliant SDRAM are not multiplexed to carry address, data and control information. (Rhoden, Tr. 401; Jacob, Tr. 5465).

1296. The invention described in the ‘898 specification has “no need for separate device-select lines since device-select information for each device on the bus is carried over the bus.” (CX1451 at 14). This indicates that the bus system described in the ‘898 specification does not have a chip select network for indicating which chips should respond to commands. (Jacob, Tr. 5495-96).

1297. A JEDEC-compliant SDRAM uses a separate chip-select network. (Jacob, Tr. 5465). A chip-select line is a wire in JEDEC architecture that is used to identify a “rank” or module of DRAMs for responding to commands. (Jacob, Tr. 5471-72).

The Packetized System of the ‘898 Specification

1298. The ‘898 specification describes a packetized system. (Jacob, Tr. 5466). A packet is a bundle of information that is sent over a bus in multiple cycles of time. (Jacob, Tr. 5466).

1299. Because the system described in the ‘898 specification sends addresses, control signals and data blocks over a small number of bus lines (relative to the number of bits in the address), that information is sent over the bus in multiple cycles of time, which together are a packet. (CX1451 at 17; Jacob, Tr. 5466).

1300. The “Detailed Description” section of the ‘898 specification contains a subsection entitled “Protocol and Bus Operation” at pages 19-28. (CX1451 at 21-30). That subsection

includes a description of Figure 4 (CX1451 at 131) starting on page 21. (CX1451 at 23).

1301. Figure 4 of the '898 specification illustrates a preferred implementation of the invention in which a request packet is transmitted over nine bus lines over six bus cycles. (CX1451 at 23-24, 131; Jacob, Tr. 5474-75). Each of the bus lines in Figure 4 is multiplexed to carry data, address or control information. (Fliesler, Tr. 8911-12).

1302. The first bus cycle of the packet shown in Figure 4 indicates four bits to specify "access type." (CX1451 at 131; Jacob, Tr. 5475; Fliesler, Tr. 8912). The access type information indicates whether the memory should perform a read or write, the type of access, and the timing (access time) of the response. (CX1451 at 24-25, 27; Jacob, Tr. 5475; Fliesler, Tr. 8912-13).

1303. The last four bits of information transmitted in the sixth bus cycle shown in the packet of Figure 4 give block size information. The block size information specifies the size of the data block to be transferred. (CX1451 at 29-30, 131; Jacob, Tr. 5475-76).

1304. The '898 specification does not describe the implementation of a request packet, other than that of Figure 4. (CX1451 at 23-24). The specification does not describe transmission of a read or write request in a non-packetized system. (CX1451; Jacob, Tr. 5476-77).

1305. The specification does not describe transmission of a read or write request over any bus other than one having substantially fewer bus lines than bits in a single address and having multiplexed lines for carrying address, control and data information. (CX1451; Jacob, Tr. 5476-77).

1306. JEDEC-compliant SDRAM does not operate as a packetized system such as that described in the '898 specification. (Jacob, Tr. 5467). The JEDEC SDRAM architecture does not transmit request information over a small number of multiplexed bus wires over multiple bus cycles. (Jacob, Tr. 5476). The JEDEC SDRAM architecture transmits request information over dedicated bus wires over one bus cycle for the column address and one bus cycle for the row address. (Rhoden, Tr. 402-04; Jacob, Tr. 5477).

1307. Because the system described in the '898 specification does not include a chip-select line, it encodes information for designating a particular DRAM to respond to a request in a packet. (Jacob, Tr. 5472). When the bus master sends a packet to the memory system, every DRAM in the system must decode that packet and determine from the identification information in the packet if the packet is designated for that particular DRAM, or some other DRAM in the system. (CX1451 at 22-23; Jacob, Tr. 5472).

1308. JEDEC-compliant SDRAM use a separate chip-select network. They do not

receive identification information in request packets. (Jacob, Tr., 5465, 5471-72).

Description of Block Size in the ‘898 Specification

1309. The ‘898 specification describes the operation of the block size feature at pages 27 and 28. (CX1451 at 29-30). This portion of the specification includes a table illustrating that the block size can be varied from 0 to 1024 bytes. (CX1451 at 30; Jacob, Tr. 5477-78).

1310. The last four bits of information transmitted in the sixth bus cycle shown in the packet of Figure 4 (CX1451 at 131) in the ‘898 specification give block size information. The block size information specifies the size of the data block to be transferred. (CX1451 at 29-30, 131; Jacob, Tr. 5475-77; Fliesler, Tr. 8918).

1311. Because, in the system described in the ‘898 specification, the block size information is transmitted with each request packet, the block size information can be easily and efficiently changed with each new request. (Jacob, Tr. 5479; Fliesler, Tr. 8919).

1312. In a JEDEC-compliant SDRAM, the burst length feature is programmed during initialization. (JX0056 at 114; Fliesler, Tr. 8920). The burst length is typically set once at system start-up and never changed again. The burst length cannot be easily and efficiently changed with each new request. (Jacob, Tr. 5479).

1313. The JEDEC SDRAM standard requires only two possible values for the burst length, four and eight. (JX0056 at 114).

1314. The variable block size feature described in the ‘898 specification addresses a scheduling problem inherent in the narrow, multiplexed, packetized bus system of the ‘898 specification. An inefficiency results from the data and address information sharing relatively few bus lines. The variable block size feature increases efficiency by maximizing the amount of data that can be transferred in response to a request as needed. (Jacob, Tr. 5479-80). The description and use of the variable block size feature described in the ‘898 specification is inherently tied to the narrow, multiplexed bus architecture and packetized system. (Jacob, Tr. 5479-81).

1315. The ‘898 specification explains, “[t]ransfers of long blocks of data use the bus efficiently even without overlap because the overhead due to bus address, control and access times is small compared to the total time to request and transfer the block. (CX1451 at 18).

1316. The ‘898 specification describes the use of a variable block size feature only in the context of a narrow, multiplexed bus architecture and a packetized system. (Jacob, Tr. 5478). The ‘898 specification does not describe the use of a variable block size feature in any other context, including in the context of a DRAM generally. (Jacob, Tr. 5478).

1317. In a JEDEC-compliant SDRAM, the programmable burst length feature is present as a convenience. It is not needed to address the bus scheduling and inefficiency concerns generated by the use of a narrow, multiplexed bus. (Jacob, Tr. 5480).

1318. An engineer reading the '898 specification in the early to mid-1990s would not have thought that Rambus could obtain patent rights over the programmable burst length feature as it is used in JEDEC SDRAM due to the difference between the JEDEC system and the system described in the '898 specification. (Jacob, Tr. 5480-81).

Description of Access Time in the '898 Specification

1319. In the system described in the '898 specification, the memory device responds to a read request packet or a write request after waiting the specified access time. (CX1451 at 17; Jacob, Tr. 5481).

1320. As described in the '898 specification, each request packet contains information that specifies the access time. (CX1451 at 23, 25, 29; Jacob, Tr. 5482). This allows the bus master to efficiently change the access time with each new request packet. (CX1451 at 29, Jacob, Tr. 5483).

1321. In a JEDEC SDRAM, the CAS latency is programed at system start-up. The CAS latency is not changed during operation. The CAS latency cannot be changed with each request. (JX0056 at 114; Jacob, Tr. 5483; Fliesler, Tr. 8920).

1322. The implementation of the access time feature described in the '898 specification is inherently tied to narrow, multiplexed bus and packetized system described in the specification. (Jacob, Tr. 5483-84). By allowing changes to the access time on a request-by-request basis, the system described in the '898 specification resolves inefficiencies that result from the use of a narrow, multiplexed, packetized bus in which address and control information must share lines with data. (Jacob, Tr. 5484).

1323. The specification explains that the access time allows the shared bus to be used for other requests during the access time: "The bus to be used in the intervening bus cycles [between request and response] by the same or other masters for additional requests or brief bus accesses. Thus, multiple, independent accesses are permitted, allowing maximum utilization of the bus for transfer of short blocks of data." (CX1451 at 17-18).

1324. The '898 specification does not describe the use of access time in any context other than the context of a narrow, multiplexed bus operating in a packetized system. (Jacob, Tr. 5476-77).

1325. In a JEDEC SDRAM, programmable CAS latency is used as a convenience to

allow parts that have different performance to exist in the same system. (Jacob, Tr. 5484).

1326. Because of the difference between the implementation and function of access time in the '898 specification and programmable CAS latency as used in the JEDEC SDRAM standard, an engineer reading the '898 application in the early to mid-1990s would not have understood that Rambus might obtain patent rights over programmable CAS latency as that feature was used in the JEDEC SDRAM standard. (Jacob, Tr. 5484-85).

Description of the Clocking Scheme in the '898 Specification

1327. In the "Background of the Invention" section, the '898 specification states "The clocking scheme used in this invention has not been used before . . .". (CX1451 at 7).

1328. According to the "Brief Description of the Drawings" section of the '898 specification, "Figures 8a and 8b show the connection and timing between bus clocks and devices on the bus." (CX1451 at 12). Figure 8a (CX1451 at 145) depicts the U-shaped clock organization described in the specification at pages 46-48. (CX1451 at 47-49, 145; Jacob, Tr. 5485).

1329. In Figure 8a (CX1451 at 145), the clock (labeled CLK) sends a clock signal, clock 1, along a wire. Each chip in the system connects to the wire and receives an "early bus clock signal." At the end of the system, the clock wire turns, and returns to the clock. On the return, the wire transmits the clock 2 signal to each chip, which receives a "late clock signal. (CX1451 at 47-48; Jacob, Tr. 5485-86).

1330. In the clocking system described in the '898 specification, each DRAM has circuitry that synthesizes an internal, midpoint clock signal from the early clock and the late clock signals. (CX1451 at 48-49; Jacob, Tr. 5467-69; see DX0096). Figure 13 of the '898 specification is a timing diagram showing the early clock, late clock and internal clock signal that represents the time average, or midpoint, between the early and late clock. The internal midpoint clock is not in synch with either of the external clocks (early and late clock). (CX1451 at 149; Jacob, Tr. 5491; Fliesler, Tr. 8922).

1331. In the clocking scheme described in the '898 specification, a DRAM latches data in sync with the internal, time average, midpoint, clock and not any external clock. (CX1451 at 149; Jacob, Tr. 5492).

1332. A JEDEC-compliant DDR SDRAM does not generate an internal, time average, midpoint clock from external clock signals. (Jacob, Tr. 5492-93).

1333. A JEDEC-compliant DDR SDRAM latches (inputs) data in sync with an external clock, DQS. (Jacob, Tr. 5493; JX0057 at 32). A JEDEC-compliant DDR SDRAM outputs data

in sync with the external clock signals, CLK and CLK bar. (Jacob, Tr. 5557-60; 5493, JX0057 at 32).

1334. The clocking scheme described in the '898 application differs from the clocking scheme used in the JEDEC DDR SDRAM standard because the application's clocking scheme uses one wire to transmit two clock signals (the early and late signals) whereas the standard uses two wires (clock and clock bar) to transmit one, differential clock signal. (Jacob, Tr. 5492-93; JX0057 at). (A differential clock signal, consisting of the signal and its inverse, is, by definition, one clock signal. (Jacob, Tr. 5493). An engineer reading the '898 patent application during the 1990s would not have thought that Rambus could obtain patent rights over the dual-edged clocking feature as it was proposed for and used in the JEDEC DDR SDRAM standard because of the difference between the two clocking schemes. (Jacob, Tr. 5493).

Description of Figure 12 in the '898 Specification

1335. According to the "Brief Description of the Drawings" Section of the '898 specification, "Figure 12 is a block diagram showing how the internal device clock is generated from two bus clock signals using a set of adjustable delay lines." (CX1451 at 13). The specification describes Figure 12 (CX1451 at 148) at pages 57-58 (CX1451 at 58-59).

1336. Figure 12 of the '898 specification depicts the circuit located on each chip in the described system generates the time averaged, midpoint internal clock signal. (CX1451 at 13). The circuit of figure 12 uses the early clock signal (56) and late clock signal (57) shown in Figure 8a as inputs and generates the mid-point clock signal (73) as its output. (CX1451 at 58-59; Jacob, Tr. 5487; Fliesler, Tr. 8926-27). The only output of the circuit in Figure 12 is the time averaged, mid-point internal clock signal (73). (Fliesler, Tr. at 8927).

1337. Figure 12 does not show a phase lock loop (PLL). (Jacob, Tr. 5487-88). The '898 application never refers to a phase-locked loop or a PLL. (Jacob, Tr. 5489-90).

1338. Figure 12 does not show a delay lock loop (DLL). (Jacob, Tr. 5488). A comparison of a DLL circuit and the circuit of Figure 12 indicates that they have different structures. (Jacob, Tr. 5488-89, see DX0097). The '898 application never refers to a delay-locked loop or DLL. (Jacob, Tr. 5489-90; Geilhufe, Tr. 9663).

1339. The circuit of Figure 12 performs a different function than a DLL. The circuit of Figure 12 uses two clock signals to generate a third signal that is the midpoint, time-average of the two original clock signals. A DLL delays one input signal so that it will be synchronized with a second signal. (Jacob, Tr. 5488-89).

1340. An engineer reading the '898 application in the mid to late 1990s would not have thought that Rambus might obtain patent rights to on-chip DLL as it was used in the JEDEC

DDR SDRAM standard due to differences between the implementation, circuit structure and function of the circuit in Figure 12 compared to a DLL circuit. (Jacob, Tr. 5490).

(2) The Claims Contained in the Publicly Available Patent Application and Patents Known to JEDEC Members.

1341. In addition to the limited language of the specification, discussed above, each of the publicly available patent application or patents known to JEDEC members during and immediately following the withdrawal of Rambus as a JEDEC member contained limitations in its respective patent claims that would not have placed a reasonable engineer on notice of claims by Rambus to JEDEC-standard technology. (CCFF 1342-57).

The Rambus International Patent Application

1342. Rambus filed its International Patent Application under the Patent Cooperation Treaty (the PCT application) on April 16, 1991. (CX1454 at 1). The PCT application was published on about October 31, 1991, and contains the original text, drawings and 150 original claims of the '898 U.S. application. (CX1454; CX1451)

1343. The '898 patent application, as first filed in the PTO, contained 150 original claims. (Nusbaum, Tr. 1515). None of the original 150 claims cover JEDEC-compliant SDRAM. (Nusbaum, Tr. 1526). None of the original 150 claims would have alerted an engineer in the 1990s that Rambus might seek to obtain patent rights over features proposed for use or used in the JEDEC SDRAM or DDR SDRAM standards. (Jacob, Tr. 5494-98).

1344. Two limitations of the '898 application, "said bus containing substantially fewer bus lines than the number of bits in a single address," and "said bus carrying device-select information without the need for separate device-select lines connected directly to individual memory devices" can be characterized as multiplexed bus limitations. (Nusbaum, Tr. 1527; Jacob, Tr. 5494-96). Of twenty independent claims in the original group of 150, only two, claims 73 and 91, lack both of these limitations. (Nusbaum, Tr. 1520).

1345. A majority of the 150 original claims contain the limitation "said bus containing substantially fewer bus lines than the number of bits in a single address." (CX1451 at 64-125; Nusbaum, Tr. 1519; Jacob, Tr. 5495). A JEDEC-compliant SDRAM does not satisfy this limitation because it uses more bus lines than the number of bits in a single address. (Nusbaum, Tr. 1527-28; Jacob, Tr. 5495; see Rhoden, Tr. 401).

1346. A majority of the 150 original claims also contain the limitation "said bus carrying device-select information without the need for separate device-select lines connected directly to individual memory devices." (CX1451 at 64-125; Nusbaum, Tr. 1519; Jacob, Tr. 5495). A JEDEC-compliant SDRAM system does not satisfy this limitation because it includes

a chip-select line that is directly connected to individual memory devices. (Nusbaum, Tr. 1528; Jacob, Tr. 5465, 5495-96).

1347. Claim 73 is directed to a “loop clocking system,” also called the U-shaped clocking scheme, having an “early bus clock” and a “late bus clock.” (CX1451 at 089-90; Nusbaum, Tr. 1523-24; Jacob, Tr. 5497). A JEDEC-compliant SDRAM does not use the clocking scheme recited in claim 73 (Nusbaum, Tr. 1528; Jacob, Tr. 5492-93, 5497).

1348. Claim 91 requires “bus connection means” (i.e., pins) that are “positioned along a single side of the package.” (CX1451 at 099; Nusbaum, Tr. 1524). The narrow bus described in the ‘898 specification allows for a small number of connecting pins that can be positioned along a single side of the chip’s package. (Nusbaum, Tr. 1528-29). JEDEC-compliant SDRAM do not use connection means along only one side of a package. The pins are along at least two sides of chip’s package. (Nusbaum, Tr. 1529; Jacob, Tr. 5497-98).

1349. A reasonable patent practitioner reviewing the ‘898 application would not have assumed that the original 150 claims contained limitations that were unnecessary to distinguish the prior art because of the massive effort that he would have presumed to have gone into drafting the relatively large number of claims and the relatively lengthy specification. (Nusbaum, Tr. 1537-40).

1350. A reasonable patent practitioner would have presumed that the multiplexed bus limitations, which appear in the majority of the 150 claims, were necessary to define the invention because the first paragraph of the Summary of the Invention section of the application characterizes the two limitations as features of the “present invention.” (Nusbaum, Tr.1539-40).

The ‘703 Patent

1351. Rambus patent 5,243,703 (the ‘703 patent) issued September 7, 1993. (CX1460 at 1). The ‘703 patent claims priority to the ‘898 application. The ‘703 patent issued from a divisional application of the ‘898 application. (CX1460 at 1).

1352. The specification and drawings of the ‘703 patent are substantially the same as the specification and drawings of the ‘898 specification and drawings. (CX1460; CX1451; Jacob, Tr. 5500-01).

1353. The claims of the ‘703 patent recite a “U-shaped clocking scheme” having an early clock and a late clock signal and generating the time average of those two clock signals. (CX1460 at 24; Jacob, Tr. at 5499-5500). The JEDEC SDRAM and DDR SDRAM standards do not use the “U-shaped clocking scheme.” (Jacob, Tr. 5492-93, 5497).

1354. The ‘703 patent would not have alerted an engineer during the 1990s that Rambus

might seek to obtain patent rights over features contained in the JEDEC SDRAM or DDR SDRAM standards because the claims of the '703 patent recite the U-shaped clocking scheme. (Jacob, Tr. 5498-99).

1355. The '703 patent would not have alerted an engineer during the 1990s that Rambus might seek to obtain patent rights over features contained in the JEDEC SDRAM or DDR SDRAM standards because its specification and drawings, which are substantially the same as those of the '898 application, do not relate to the standard. (Jacob, Tr. 5460-5501).

The Patents Identified in the Rambus Withdrawal Letter

1356. At the time that Rambus withdrew from membership from JEDEC, it submitted with its withdrawal letter dated June 17, 1996, a list of issued patents. (CX0887 at 2). The list was not a complete list of issued patents because the '327 patent was not on the list. (CX0888 at 2; Crisp, Tr. 3381, 3384; Diepenbrock, Tr. 6200).

1357. None of the listed patents would have alerted an engineer in the 1990s that Rambus might be able to obtain patent rights over features incorporated in the JEDEC SDRAM or DDR SDRAM standards. (Jacob, Tr. 5502). Each patent on the list dated June 17, 1996 (CX0887 at 2) is either restricted to a narrow, packetized, multiplexed bus architecture, addresses topics outside the scope of the JEDEC 42.3 committee, or relates to only minor implementation details of material that could have been within the scope of the 42.3 committee. (Jacob, Tr. 5502).

1358. Paragraphs 1358 - 1499 are unused.

VII. RamLink, Synclink and the SyncLink Consortium.

1500. In addition to the Rambus and JEDEC efforts to develop standards for next-generation DRAM technology, there were other similar efforts during the 1990's. Among these were the Ramlink, Synclink and SyncLink Consortium efforts, which did not result in commercially viable DRAM standards. (CCFF following).

A. The IEEE RamLink and SyncLink Working Groups.

1. The IEEE Had Rules Substantially Different From Those of JEDEC.

1501. The IEEE was a professional organization that engaged in various activities, including standard-setting activities. (Tabrizi, Tr. 9116; *see also* Prince, Tr. 8972-73).

1502. Membership in the IEEE was not by company; rather, individuals belonged to IEEE in their individual capacity. (Tabrizi, Tr. 9117; *see also* RX0579 (“ . . . [M]embership and participation is by the individual person, as a professional, rather than by a company with the person being merely the company’s representative, as is the case for ANSI and JEDEC projects.”)).

1503. The IEEE procedures, unlike those of JEDEC, did not impose any obligation on companies with respect to patent disclosure. (Tabrizi, Tr. 9122 (“Again, the IEEE policy, since the individual participants were representing themselves, they were not representing any company, they had no obligation to, in terms of patent disclosure. It was kind of vague enough. It wasn’t like JEDEC, very solid patent disclosure.”); Crisp, Tr. 3283-84; CX0711 at 128, 129-30 (“The talk moved temporarily to patents, and Walther was adamant in pointing out that the bylaws permit the member companies to retain their own intellectual property.”); JX0027 at 26 (“Additionally, SyncLink is being sponsored by an organization with a less stringent patent policy than JEDEC. Under the bylaws of the IEEE working groups, attendees represent themselves only, not their employers. Furthermore, they are free to patent whatever they desire, and are not bound to relinquish any of their rights to their patents by presenting their ideas for standardization.”)).

2. RamLink Was Developed By Supercomputer Scientists to Standardize a New Future Memory Bus.

1504. RamLink was a specification for a packet-based memory. (Tabrizi, Tr. 9116). RamLink was being developed by the 1596.4 working group within the IEEE. (Gustavson, Tr. 9280).

1505. RamLink developed as an effort to standardize a new future bus. (Tabrizi, Tr. 9117 (“RamLink was a generic bus that you could connect any kind of memory to it.”); Prince,

9018 (“ . . . [T]he IEEE had been engaged for a considerable period of time in standardizing the scalable coherent interface as a replacement for the future bus backplane. . . . The future bus was getting old.”)).

1506. RamLink developed from work of supercomputer scientists on the so-called scalable coherent interface, an effort to develop an entire backplane, or an entire set of components for a high-speed system. (Prince, 9018-19 (“ . . . [T]he IEEE had been engaged for a considerable period of time in standardizing the scalable coherent interface as a replacement for the future bus backplane. . . . [T]he people involved in the scalable coherent interface were the supercomputer scientists of the industry from IBM, Hewlett-Packard, CDC, Apple. . . . [T]hey were defining an entire backplane, an entire set of components . . .”)).

1507. RamLink consisted of a high speed bus protocol that permitted access, based on scheduling of events, to the bandwidth that already existed inside DRAMs. (JX0026 at 95 (“What is RamLink? – High performance protocol that permits access to the large bandwidth already available inside DRAM chips – The basic protocol concepts are based on the scheduling of events”)).

1508. The RamLink bus was fully multiplexed; command, address and data information were all sent on a single bus. (Tabrizi, Tr, 9119).

1509. RamLink members sought to cooperate with Rambus in order to come up with a better standard. Wiggers, Tr. 10,596-97; CX0681 at 1 (“Wigger[s] says Ramlink wants to cooperate with us.”)).

1510. Rambus regarded RamLink as a source of potential competition. (Farmwald, Tr. 8369; CX0681 (“ . . . [O]ur decision options [with respect to RamLink] are (1) Decide they are the enemy and do one or more of: (a) Kill them ourselves (b) Convince them to kill themselves (c) Convince their management to kill them . . .”)).

1511. Richard Crisp attended meetings of the IEEE P1596.4 RamLink/SyncLink working group in early to mid-1995. (Crisp, Tr. 3528; RX-0579 at 6 (“Attendees . . . Richard D. Crisp”); CX0711 at 81-82 (“As a regular attendee of the Ramlink working group you contributed to the standard and by IEEE rules you were and are a voting member of the working group.”)).

1512. IEEE was balloting the RamLink proposal for standardization as of June 1995. (Gustavson, Tr. 9282; Gustavson, Tr. 9283).

3. The IEEE SyncLink Project Grew Out of, and Modified, the Proposed RamLink Standard.

1513. SyncLink developed as a subset of RamLink (Tabrizi, Tr. 9117 (“SyncLink was a subset of RamLink.”); Gustavson, Tr. 9280 (SyncLink was “an off-shoot of Ramlink”); Gustavson, Tr. 9282 (SyncLink was “something that grew out of RamLink”); JX0026 at 98 (“– RamLink supports a rich set of transactions and features – SyncLink uses a subset of those features . . . – Uses existing DRAM technology”). Whereas Ramlink was intended to be a generic bus to which one could connect any kind of memory, SyncLink was intended to be specific to synchronous DRAMs. (Tabrizi, Tr. 9117).

1514. The purpose of SyncLink was to create an open standard for the next generation memory system, in which everybody would be able to develop products compatible with the standard free of blocking patents. (Tabrizi, Tr. 9117-18; *see also* JX0026 at 10 (“It was intended to be an open standard.”)).

1515. SyncLink was the subject of development within the IEEE P1596.7 working group. (RX0940 at 7, 9).

1516. As with RamLink, SyncLink focused on the bus and system protocol; it consisted of an entire system. (JX0026 at 96 (What is a SyncLink? – Implementation of a subset of the RamLink Protocol for high-performance memory systems . . . – Typically a SyncLink memory system consists of a Link Controller, a number of memory devices or modules called SLDRAMs, and the interconnect, all on a single board.”); Tabrizi, Tr. 9118 (“JEDEC was working on the core DRAM project and the SyncLink was working on the kind of overall – the component plus the bus that link them together.”)).

1517. The SyncLink project modified the RamLink protocol. (Gustavson, Tr. 9284; *see also* RX0589 at 1 (“The main question was how much to modify the RamLink protocol to optimize for SyncLink.”)). The resulting SyncLink architecture was partially multiplexed; command and address information were sent on a single bus, but data was sent on a separate bus. (Tabrizi, Tr. 9119).

1518. The SyncLink project had just begun as of May-June 1995. (Gustavson, Tr. 9283).

1519. Richard Crisp attended meetings of the IEEE RamLink and SyncLink working groups. (Crisp, Tr. 3528; Tabrizi, Tr. 9033; RX-0579 at 6 (“Attendees . . . Richard D. Crisp”); RX-0590 at 3 (“Attendees . . . Richard D. Crisp”)).

1520. Rambus regarded SyncLink as a potential threat to Rambus. Crisp, Tr. 3255 (SyncLink could potentially be a threat to Rambus); Crisp, Tr. 3528-29 (Crisp viewed SyncLink

as a potential competitor to RDRAM); *see also* Farmwald, Tr. 8369-70 (RamLink or SyncLink was a marketing concern to Rambus); CX0911 (“Competitive Alternatives . . . SyncLink; is it real or is it memorex?”).

4. The IEEE RamLink/SyncLink Project Was Presented At the JEDEC JC-42.3 Committee, But Rambus Refused to Disclose Whether It Had Any Patents or Patent Applications Relating To It.

1521. In May 1995, Hyundai, Texas Instruments and Mitsubishi presented the RamLink and SyncLink architectures at JEDEC. (JX0026 at 10-11, 95-113). The Mitsubishi presentation of SyncLink included a description of dual edge clocking. (JX0026 at 112 (“Strobe In Reference Clock both edge for input, positive edge for output”; *see also* timing diagram at bottom of page 112); Rhoden, Tr. 471-72; Kelley, Tr. 2574-75; Sussman, Tr. 1408-09).

1522. Gordon Kelley asked whether any companies had patent issues regarding SyncLink. (CX0711 at 72 (“Gordon Kelley asked whether or not any companies have patent issues with the material.”)). Hyundai, Texas Instruments, Mitsubishi and Hewlett Packard all stated that they did not have patents covering SyncLink, and Farhad Tabrizi stated that SyncLink was intended to be an open system. (CX0711 at 72; JX0026 at 10 (“It was stated that no known patents exist on this proposal. It was intended to be an open standard.”); Rhoden, Tr. 474). When Mr. Crisp, the Rambus JEDEC representative, did not respond to this inquiry at the May 1995 meeting, Mr. Kelley asked Mr. Crisp to go back to Rambus and then report back to the Committee whether Rambus knew of any patents, especially Rambus patents, that may read on the SyncLink technology. (CX0711 at 73; CX0794 at 4; Crisp, Tr. 3267-68).

1523. After substantial internal discussion and efforts at Rambus over several months (CCFF 1050-55), at the September 1995 meeting of the JEDEC Committee, Mr. Crisp provided a response of Rambus to the inquiry made at the May 1995 Committee meeting concerning patents on SyncLink. (Crisp, Tr. 3306-08). Mr. Crisp provided the Committee a letter from Rambus in which Rambus refused to provide any information concerning whether there were Rambus patents or patent applications that might apply to SyncLink. (CX0829; JX0027 at 26 (“Rambus elects not to make a specific comment on our intellectual property position relative to the SyncLink proposal.”)). The letter included other recitations, including the observation that it would be several years before there was a finalized SyncLink specification to analyze for possible infringement, and that SyncLink was being developed under the auspices of IEEE, which had “a less stringent patent policy than JEDEC.” (*Id.*). (See CCFF 1062-68).

1524. Mr. Crisp reported to his Rambus colleagues that there would be no second showings of the SyncLink material at the September 1995 Committee meeting. (CX0711 at 171). Mr. Crisp reported that one of the meeting participants told Mr. Crisp that he thought the reason there would be no second showings of the SyncLink technology at JEDEC was that “we [Rambus] have cast doubt over the patent issue.” (*Id.*).

5. Although Mr. Crisp of Rambus Inadvertently Disclosed Limited Information to the IEEE Working Group Regarding the Potential Coverage of Rambus Patents, Rambus Refused to Provide a RAND Letter and No Product Implementing the RamLink Standard Ever Came to Market.

1525. In June 1995, Reese Brown posted a copy of the ballot for the proposed IEEE RamLink standard on the JEDEC reflector. (CX0711 at 76-77 (“I am posting this notice at the request of Ken McGhee: The JEDEC Office has received a copy of a ballot of a proposed IEEE Standard . . . (RAMLINK).”); Crisp, Tr. 3280-82).

1526. Richard Crisp took exception to the posting of RamLink information on the JEDEC reflector. (Crisp, Tr. 3282). Without planning to do so beforehand, Mr. Crisp wrote in an e-mail to Mr. Brown stating in part that the proposed IEEE standard was not real and had patent issues associated with it. (CX0711 at 79-80; Crisp, Tr. 3282-83). Mr. Brown forwarded Mr. Crisp’s e-mail to Mr. Hans Wiggers. (Crisp, Tr. 3283).

1527. Hans Wiggers was the Chairman of the RamLink working group as of mid-1995. (Gustavson, Tr. 9282).

1528. Mr. Wiggers wrote to Mr. Crisp because, as Chairman of the RamLink working group, he took Mr. Crisp’s comment about patent issues “very seriously.” (CX0711 at 90-91; Wiggers, Tr. 10,595 (“ . . . because I was the chair, I had to take serious any claims of patents by anybody.”)). Mr. Wiggers stated that he assumed Mr. Crisp had attended the IEEE working group meetings in “good faith,” and if Mr. Crisp knew of any way in which the proposed RamLink standard violated patents held by Rambus or others, he thought Mr. Crisp had a “moral obligation” to bring to his attention information about which patents were being violated. (CX0711 at 90-91; Crisp, Tr. 3284-86).

1529. Mr. Crisp replied to Mr. Wiggers that his personal opinion was that the RamLink/SyncLink proposals will have a number of problems with Rambus intellectual property. He stated that he planned to make an official statement at the September 1995 JEDEC meeting, and in the meantime he had nothing else to say about Rambus’s patent position. He further stated that Rambus would not make any comment with respect to pending material until it issued. (CX0711 at 103, 104-05; Crisp, Tr. 3287-89).

1530. Mr. Crisp sought to prevent Mr. Wiggers from passing this information on to others. He stated in his e-mail that he claimed and withheld all copyrights for the material in his e-mail, and asked Mr. Wiggers to respect his request not to copy and distribute his e-mail to others. (CX0711 at 103, 107; Crisp, Tr. 3289-90). Mr. Wiggers agreed. *Id.*

1531. Mr. Wiggers wrote to Mr. Crisp again in July 1995, stating that as part of

submitting the RamLink standard to the IEEE Standards Board, he had to certify that there were no patent issues outstanding. He stated that he had to report his previous communications with Mr. Crisp. (CX0711 at 130, 131; Crisp, Tr. At 3291-92). Mr. Crisp responded that he had nothing to say to the IEEE working group regarding Rambus's patent position, and that anything he had said in private correspondence was not to be construed as an official position of the company. (CX0711 at 136-37; Crisp, Tr. 3293-94).

1532. Mr. Wiggers offered to summarize in his words the earlier correspondence with Mr. Crisp. Crisp, Tr. 3294. Mr. Crisp responded, "Not acceptable!", and asserted that he had "no obligation under any agreements [he had] made with anyone to report anything to anyone relative to the Rambus intellectual property . . ." (CX0711 at 142, 145; *see also* Crisp, Tr. 3294-96). Mr. Wiggers then agreed to pass on only a short statement to the effect that Mr. Crisp expressed a personal opinion that the SyncLink proposal may infringe Rambus patents. (CX0711 at 146; *see also* Crisp, Tr. 3296-97).

1533. At the next meeting of the IEEE working group, it was announced that Mr. Crisp informed the group that, in Rambus's opinion, both RamLink and SyncLink "may" violate Rambus patents that date back as far as 1989. (RX0590 at 2). The statement did not provide any details about Rambus's issued patents or pending patent applications, or about what aspects of the RamLink or SyncLink work might infringe Rambus patent rights. (RX0590 at 2; Crisp, Tr. 3299). The working group concluded that resolution of the issues of whether early public work might invalidate such patents or whether the patents appear to be violated was not a feasible task for the working group, so it decided to continue with the technical work at hand. (RX0590 at 2).

1534. Despite Mr. Crisp's statement to the IEEE working group, Rambus declined to comment at JEDEC with respect to its intellectual property position relative to the SyncLink proposal at JEDEC. (JX0027 at 26).

1535. In December 1995, Ms. Cheryl Rowden, Administrator - Intellectual Property of the IEEE, wrote to Rambus asking Rambus to advise the IEEE whether Rambus's patent or patents applied to information contained in the IEEE P1596.4 working group's draft RamLink standard and, if so, whether Rambus would issue a letter of assurance that it would make a non-discriminatory license to its technology available under reasonable rates, terms and conditions. (CX0487).

1536. On Rambus's behalf, Lester Vincent prepared draft responses to the IEEE indicating that Rambus had patent rights that covered the draft RamLink standard and that Rambus would not agree to be bound by the IEEE's licensing terms. Mr. Vincent prepared a draft dated January 11, 1996 stating that Rambus patent rights "do cover information found in the draft IEEE P1596.4 document." (CX0853 at 2). The draft letter further stated, however, that Rambus was under "no obligation" to any standards body "to license its intellectual

property” or “to disclose its intellectual property in order to retain the right to enforce” it, that Rambus reserved the sole right to decide whether and at what rate or rates to license intellectual property, that Rambus’s intellectual property rights were “not limited by the policy of any standards body,” and that Rambus “will not . . . issue the letter of assurance that you have requested regarding a non-discriminatory license.” (*Id.* at 1-2). Mr. Vincent prepared a draft dated January 15, 1996 stating that Rambus wished to continue to license its technology on terms that are “consistent with Rambus’s own business plan and that are not set by any standards body,” and that Rambus therefore was “unable” to provide the IEEE with the letter of assurance that the IEEE sought. (CX0856 at 1). The draft letter further stated that Rambus had applied for a number of additional patents, but that those patent applications remained confidential. (*Id.* at 2).

1537. On January 15, 1996, Mr. Anthony Diepenbrock sent a letter to Ms. Rowden of the IEEE omitting many of the statements from Mr. Vincent’s drafts. (CX0855). Mr. Diepenbrock’s letter stated that Rambus “cannot comment” on the proposed RamLink standard, containing a list of issued Rambus patents, and stating that Rambus would continue to license its technology “in accordance with its existing business practices.” (CX0855 at 2).

1538. On February 16, 1996, Ms. Rowden wrote to Mr. Diepenbrock stating that, from Mr. Diepenbrock’s letter of January 15, 1996, it was the understanding of the IEEE that Rambus was willing to license applicants “on a nondiscriminatory basis under reasonable terms and conditions” for the purpose of implementing the IEEE RamLink standard. (CX0490).

1539. Mr. Diepenbrock disagreed with Ms. Rowden’s interpretation of his January 15, 1996 letter because he found that agreeing to reasonable and non-discriminatory terms to be inconsistent with Rambus’s existing business practices. (Diepenbrock, Tr. 6223-24, 6228). On February 21, 1996, he wrote a reply letter to Ms. Rowden repeating his earlier statement that Rambus would continue to license its technology “in accordance with its existing business practices.” (CX0869).

1540. The IEEE requested that the 1596.4 working group redesign the RamLink standard so that it wouldn’t violate any Rambus patent claims. (Gustavson, Tr. 9296-97).

1541. Mr. Gustavson reviewed the claims of certain of Rambus’s pending patent applications. (Gustavson, Tr. 9286). His background was that of a system architect; he was interested in the bus and the system architecture, not the DRAMs. (Gustavson, Tr. 9313-14). He concluded that there was no way to work around the claims that he saw, since they related to things that the working group had been doing for ten years or so. (Gustavson, Tr. 9287). Mr. Gustavson thought the Rambus patent claims should not block the balloting of the proposed RamLink standard. (Gustavson, Tr. 9294).

1542. Also in February 1996, Mr. Crisp called Mr. Gustavson because he believed that

Mr. Gustavson “was misinterpreting Rambus’s position relative to Ramlink etc.” (RX0593 at 1.) Mr. Crisp reported that Rambus was “not able to determine at this time” whether there was a conflict between the RamLink standard and Rambus’s patents. (*Id.* at 1-2). Mr. Gustavson concluded, “I expect they won’t try to interfere with the standardization process.” (*Id.* At 2.)

1543. Although the IEEE later issued the proposed RamLink standard, no product implementing the RamLink standard ever came to market. (Prince, Tr. 9012).

6. In Response to the Possibility That Rambus Patents Might Cover SyncLink, Hyundai Negotiated an “Other DRAM” Provision As Part of Its RDRAM License To Provide Rights To Use Rambus Technology In Non-Rambus DRAMs.

1544. After Hyundai became aware that Rambus might have patents covering aspects of SyncLink, it negotiated an “Other DRAM” provision in its license agreement with Rambus as a kind of “insurance program.” This “Other DRAM” provision permitted Hyundai to use Rambus technology in DRAMs other than RDRAMs. (CCFF 1264-65).

1545. During the course of 1995, Hyundai was in negotiations with Rambus for a license permitting use of Rambus technology in connection with RDRAMs. (CX0783; CX0711 at 61; CX0711 at 64).

1546. In 1995, Dr. Oh was the Senior Vice President in charge of Hyundai’s Sales and Marketing Division. (CX2107 at 11 (Oh, Dep.)).

1547. At the time that Hyundai began license negotiations with Rambus, Dr. Oh was unaware that Rambus might have patents that extended outside the scope of RDRAM. (CX2107 at 69 (Oh, Dep.)).

1548. By the latter half of 1995, Dr. Oh and others at Hyundai were aware of the possibility that some aspect of SyncLink interface technology might be covered by Rambus patents. (CX2290 at 13; CX2107 at 72 (Oh, Dep.)). However, Hyundai representatives did not have sufficient information to determine whether Rambus patents would cover SyncLink. (CX2107 at 72-73, 75-76 (Oh, Dep.)).

1549. In order to protect against the possibility that Rambus might have patents relating to SyncLink, Hyundai sought to include a statement in the Hyundai-Rambus license agreement covering SyncLink. (CX2107 at 73 (Oh, Dep.)). Hyundai viewed this as “an anticipatory move” or an “insurance program” in case it turned out that Rambus had patents relating to SyncLink. (CX2290 at 4 (“This is an anticipatory move, in view of the possibility that a patent dispute could potentially arise concerning the SyncLink Consortium, which the Company is actively working on right now.”); CX2107 at 75, 99 (Oh, Dep.)).

1550. Hyundai and Rambus signed a license agreement in December 1995. Hyundai succeeded in having included in the Hyundai-Rambus license agreement an “Other DRAM” provision that granted Hyundai the right to use Rambus technology in DRAMs other than RDRAMs, subject to payment of a 2.5% royalty. (CX1599 at 3 (Paragraph 1.5, “Other DRAM”), 12 (Paragraph 5.3(a)(ii)); *see also* CX2107 at 84-85, 91-92 (Oh, Dep.); Crisp, Tr. at 3320-22).

1551. Although the “Other DRAM” provision in the Hyundai-Rambus license agreement permitted Hyundai to use Rambus technology in all DRAMs other than RDRAMs, Hyundai was only thinking in terms of SyncLink at the time. (CX2107 at 94-96 (Oh, Dep.)).

1552. Dr. Oh regarded 2.5% as a high royalty rate, but he did not think that Hyundai would actually have to pay that rate. He regarded it as an “insurance program” in case it turned out that SyncLink violated Rambus patents and Hyundai had no alternatives. (CX2107 at 99 (Oh, Dep.)).

1553. Certain Rambus executives stated internally within Rambus that Hyundai would owe Rambus royalties under the Rambus Hyundai license agreement on sales of synchronous DRAMs. (CX1074 at 1.) Rambus never informed Dr. Oh that Hyundai owed Rambus royalties pursuant to this agreement for sales of synchronous DRAMs. (CX2108 at 229 (Oh, Dep.) (Dr. Oh first learned in 2002 that Rambus was asserting that SDRAM and DDR SDRAM produced by Hyundai infringed Rambus’s patents).

B. The SyncLink Consortium.

1. The SyncLink Consortium Was Formed To Permit Joint Funding and Sharing of Various Development Tasks In Order to Create the Next Generation Open Standard.

1554. The SyncLink architecture was first developed within the IEEE working group as an off-shoot of RamLink. (Gustavson, Tr. 9280 (SyncLink was “an off-shoot of Ramlink”); Gustavson, Tr. 9282 (SyncLink was “something that grew out of RamLink”). The SyncLink working group modified the RamLink protocol. (Gustavson, Tr. 9284; *see also* RX0589 at 1 (“The main question was how much to modify the RamLink protocol to optimize for SyncLink.”)). The resulting SyncLink architecture was partially multiplexed; command and address information were sent on a single bus, but data was sent on a separate bus. (Tabrizi, Tr. 9119).

1555. In August 1995, Hyundai, Mitsubishi, Mosaid and Texas Instruments formed the SyncLink Consortium. (RX0591 at 1). Companies joining later or sending attendees included Micron, Hitachi, Samsung, Fujitsu, NEC, Hewlett-Packard, IBM, Panasonic, Molex, VIS, AMP and Vanguard International. (RX2090 at 7-8). Members included not only DRAM suppliers,

but also customers and other companies. (CX2303 at 21 (identifying “users” and “others”); Tabrizi, Tr. 9177-78).

1556. The purpose of the SyncLink Consortium was to develop the next generation open standard, royalty-free standard that could meet customer requirements. (Tabrizi, Tr. 9121; *see also* RX0849 at 5 (“Consortium Mission Provide an Open Industry Standard Solutions That Meets Performance Requirements of Future Memory Systems”); RX0940 at 3 (same)). The SyncLink Consortium was intending to develop the next-generation main memory architecture that could be used in various applications, including personal computers, servers, workstations and various other segments of the market. (Tabrizi, Tr. 9126-27; *see also* RX0591 at 2 (“We all agreed that we are optimizing for PCs, the high volume market, though we want to perform well for multiple-processor systems and for graphics too.”)).

1557. The SyncLink Consortium was formed as a consortium outside of the IEEE in part to fund development of an actual prototype test chip and to work with users to develop and test a board. (Tabrizi, Tr. 9122; *see also* RX0591 at 1 (“The Consortium intends to contract with Mosaid to provide the circuit-level feasibility analysis and design support for SyncLink development.”)).

1558. The SyncLink Consortium was formed as a consortium outside of the IEEE in part because the Consortium members did not consider the IEEE rules regarding disclosure of patents to be satisfactory. Because individual members in the IEEE represented only themselves and not any company, there was no obligation of patent disclosure. (Tabrizi, Tr. 9120, 9122).

1559. The SyncLink Consortium was formed as a consortium outside of the IEEE in part to permit cross-licensing among members with respect to any technology utilized in the standard. (Tabrizi, Tr. 9122).

1560. The SyncLink Consortium was open to any company that wanted to join. (Gustavson, Tr. 9316; RX0591 at 1 (“The Consortium will be open to additional Founding Members that declare their intention to join by September 21, 1995, and complete the financial transaction by October 21, 1995. Other companies can join later, but at a price determined at that time by negotiation.”); CX0488 at 4 (“The chair actively encourages all members to actively solicit memberships from any and all companies that may be interested in this work.”)).

1561. Rambus was invited to join the SyncLink Consortium, but did not. (Gustavson, Tr. 9316; *see also* CX0488 at 4 (“SyncLink secretary should write Rambus, HP, IBM, etc. to specifically invite them to join, and keep copies.”)).

1562. The SyncLink Consortium formed a corporation known as SLDRAM Inc. (Tabrizi, Tr. 9124).

1563. The SyncLink Consortium divided the various infrastructure tasks necessary for the development of the standard among member companies. Hyundai and Mitsubishi developed an initial test chip. IBM developed a motherboard. Micron performed simulation analysis. Hewlett Packard performed an environmental analysis. IBM and Teradyne performed testing. A packaging company worked on defining the next generation package. (Tabrizi, Tr. 9127-30).

1564. The SyncLink Consortium members shared know-how and design experience relating to the SyncLink architecture. (Tabrizi, Tr. 9128-29).

1565. The SyncLink Consortium members shared the cost of development of the first chip and the expenses associated with other projects. SLDRAM Inc. levied special assessments of its members as needed for different projects. (Tabrizi, Tr. 9128).

1566. SLDRAM Inc. contracted with Mosaid to develop a 64-meg prototype chip on behalf of the Consortium. (RX0785 at 1 (“MOSAID is prepared to begin development of a 64M SL-DRAM beginning as soon as we can formalize a business relationship with the SyncLink Consortium.”)). The design work cost between \$2 million and \$3 million. (Tabrizi, Tr. 9129-30; RX0882 at 2 (“MOSAID agrees to our offered \$2.5M total, if Consortium provides 4 experienced engineers for the duration, to be under direction of MOSAID project leader, and members of the core design team.”)). The Mosaid contract was paid for by means of a special assessment in the amount of approximately \$170,000 per member company. (Tabrizi, Tr. 9178).

2. The SyncLink Consortium Sought To Avoid Patented Technologies, Including Technologies that Members Thought Might Be Covered By Rambus Patents.

1567. Members of the SyncLink Consortium were concerned about patents of non-members that might cover the work of SyncLink. The SyncLink Consortium applied for and held patents in its own name. (Tabrizi, 9124-25; Gustavson, Tr. 9314).

1568. The SyncLink Consortium’s purpose in applying for and holding patents was defensive, to prevent other individuals or companies from obtaining patents that would block the SyncLink work. (Tabrizi, Tr. 9125 (“Our patent policy was fully defensive. We just didn’t want other people to file patents on our technology.”); Gustavson, Tr. 9315-16 (“We had discovered . . . that one had to have patents so that you could be protected so that no one could block you from using your own technology, basically. And the term I heard applied to this was ‘defensive patents’.”); RX0849 at 6 (“The consortium have filed six patents for members protection against others.”); Lee, Tr. 6848-49, 7048 (“ . . . [W]e were concerned that later on some company might try to assert patents on as far as our innovations, and so the only way to protect ourselves was to file patents.”)).

1569. Members of the SyncLink Consortium were particularly concerned about Rambus's patents. (CX0488 at 2 ("Micron is particularly concerned to avoid the Rambus patents, though all of us share this concern."); *see also* Gustavson, Tr. 9303-04).

1570. The SyncLink Consortium lacked specific information about Rambus's intellectual property rights. Mr. Crisp had informed the IEEE RamLink working group that RamLink and SyncLink "may" violate Rambus patents. (RX0590 at 2). Although Mr. Vincent's draft letter of January 11, 1996 stated that Rambus patent rights "do cover information found in the draft IEEE P1596.4 document," (CX0853 at 2), Mr. Diepenbrock's final letter of January 15, 1996 to Ms. Rowden of the IEEE stated that Rambus "cannot comment" on the proposed RamLink standard, (CX0855 at 2), and Mr. Crisp subsequently told Mr. Gustavson that Rambus was not able to determine whether there was a conflict between the RamLink standard and Rambus's patents. (RX0593 at 1-2). Mr. Wiggers testified that he never received any clarification of Rambus's patent claims relating to RamLink. (Wiggers, Tr. 10,595-96; *see also* CX2107 at 76 (Oh, Dep.) ("We did not know exactly what Rambus has – had at that time. If we knew what they had, then it [the Other DRAM provision in the Hyundai-Rambus license agreement] would be more specific than this."); CX2107 at 72-73 (Oh, Dep.) ("No way – no way we can speculate [as to the possibility that Rambus's patents might cover SyncLink] because we don't know what it is.")). Neither Mr. Crisp's statement to the IEEE working group nor Mr. Diepenbrock's letters to the IEEE provided any details about Rambus's issued patents or pending patent applications, or about what aspects of the RamLink or SyncLink work might infringe Rambus patent rights. (RX0590 at 2; CX0855 at 2; Crisp, Tr. 3299).

1571. Certain members of the SyncLink Consortium thought that the SyncLink architecture (as opposed to the RamLink architecture) avoided Rambus patents because the SyncLink architecture did not use a triply multiplexed bus structure and did not use other key features of the Rambus architecture. (Lee, Tr. 6623-24 (Rambus used a loop-back clock, whereas SyncLink used a source synchronous design with data strobes; Rambus used an open drain driver, whereas SyncLink used a push/pull driver scheme; "the SyncLink bus structure just had command/address multiplexed. Data was a separate bus."); Lee, Tr. 6610-11 ("The [Rambus] patents – at least the abstracts that I had reviewed seemed to apply kind of specifically to this bus architecture, to this RDRAM product. . . . [By 'this bus' I meant] the narrow bus with the command/address/data multiplexed with this Rambus architecture and Rambus signaling scheme."); *see also* Tabrizi, Tr. 9118-19 ("At IEEE RamLink, the bus was fully multiplexed. That means address, data, command all on one bus. But the SyncLink was somewhere between the two [RamLink and the JEDEC architecture]. We made the address and command on one bus and data on a separate bus.")).

1572. SyncLink Consortium members nevertheless shared a concern to avoid Rambus patents in any future consortium work. (CX0488 at 2 ("Micron is particularly concerned to avoid the Rambus patents, though all of us share this concern.")).

3. After Intel Announced That It Would Support Exclusively RDRAM For Future PC Main Memory, The Role Of The SyncLink Consortium Changed to Supporting a Possible Future Memory Standard For Limited Applications Alongside RDRAM and DDR SDRAM.

1573. After Intel announced in late 1996 that it would support exclusively the RDRAM architecture for main memory in future personal computer architectures, the role of the SyncLink Consortium changed from developing a future generation main memory product to developing a future product for certain specific applications, particularly servers. (CCFF following).

1574. At the time it was formed, the SyncLink Consortium was intending to develop the next-generation main memory architecture that could be used in personal computers as well as servers, workstations and various other segments of the market. (Tabrizi, Tr. 9126-27; *see also* RX0591 at 2 (“We all agreed that we are optimizing for PCs, the high volume market, though we want to perform well for multiple-processor systems and for graphics too.”)).

1575. As of the latter half of 1996, DRAM manufacturers supported three different architectures for the next generation: Rambus’s Direct RDRAM, SyncLink (or SLDRAM), and DDR SDRAM. (Tabrizi, Tr. 9131-32; Peisl, Tr. 4533; Appleton, Tr. 6341; CX0711 at 183, 184-85 (Intel “will say internally that they are pushing forward two if not three different potential technologies (R2 [Direct RDRAM], SyncLink, and 200+mhz SDRAM? [DDR SDRAM], are keeping the players ‘honest’ by playing one off the other . . .”). DRAM manufacturers understood that customers would decide which architecture to buy. (Tabrizi, Tr. 9133-34; Peisl, Tr. 4417 (“Q: Did you ever express any preference to customers toward either SDRAM or RDRAM? A: No. And essentially it’s the customer’s decision which controller is being designed into a particular motherboard and that dictates the usage of the memory.”); *see also* Appleton, Tr. 6317-18 (discussing Micron’s support of burst EDO, RamLink and SDRAMs in the early 1990’s, “The customer is going to decide what they want to buy, and we needed to make sure that whatever became the customer’s choice of product, that we were in a position to be able to supply it.”)).

1576. Intel played a significant role in selecting among the future architectures. Intel built both microprocessors and chipsets that connected the microprocessors to the system main memory. (Tabrizi, Tr. 9134). At that time, Intel controlled about 80% of the market for microprocessors used in personal computers. (Tabrizi, Tr. 9138-39).

1577. In late 1996, Intel announced that its future chipsets for main system memory in personal computers would support exclusively RDRAM. (Tabrizi, Tr. 9134-35). As a result of that decision, DRAM manufacturers expected SyncLink to be relegated to non-PC applications, including servers, Apple-based computers and systems using UNIX-based processors. (Tabrizi,

Tr. 9134-35, 9137).

1578. Following Intel's announcement of its decision to support only RDRAMs for main memory in future PC systems, Mr. Tabrizi had to decide whether to stop the SyncLink Consortium work or to get some level of support from DRAM manufacturers to continue the SyncLink Consortium work. (Tabrizi, Tr. 9138-39; *see also* Appleton, Tr. 6382 (with respect to RX0801, his letter to Mr. Tabrizi, ". . . they wanted me to send this letter to Mr. Tabrizi because he was having difficulty even within Hyundai on maintaining support for SyncLink."); Lee, Tr. 6893-94 (" . . . the triggering issue is what do we do with the consortium, do we keep going forward or not.")).

1579. Mr. Tabrizi organized a meeting of executives representing the SyncLink Consortium members in January 1997 to determine the future of the SyncLink Consortium. (Tabrizi, Tr. 9138-39; RX0808 at 2 ("Propose executive meeting Friday Jan 10, 1997, in Tokyo . . . Goals: exchange ideas on future of SynchLink. Present SynchLink, ask execs for support.")). At the meeting, the level of support for the SyncLink Consortium varied from company to company; the participants agreed to continue at least to support the SyncLink Consortium's development work, but not to commit major resources to it. (Tabrizi, Tr. 9139-40).

1580. Following the meeting in January 1997, the SyncLink Consortium continued with its development work. By June 1997, the SyncLink Consortium had contracted with Mosaid to design a prototype chip. The SyncLink Consortium agreed to pay \$2.5 million for the Mosaid work; members contributed \$175,000 each. Hyundai also contributed two engineers and Siemens and Vanguard contributed one engineer each to the design effort. (Tabrizi, Tr. 9178; RX0938 at 1-2).

1581. Throughout 1997, 1998 and into 1999, most DRAM manufacturers continued to support three future generation architectures: Direct RDRAM, SyncLink, and DDR SDRAM. (CX2294 at 5, 7, 9 (Hyundai roadmaps for SDRAM, DDR SDRAM, SLDRAM and RDRAM); CX2297 at 3, 25 (Hyundai tables showing RDRAM for PC application, DDR/SLDRAM for server application, and DDR for graphic application); Tabrizi, Tr. 9144-52; CX2718 at 26, 44, 45 (Micron roadmap and tables showing projected availability and positioning of DDR, RDRAM and SLDRAM); CX2728 at 2-3 (Micron table showing projected availability and comparison of SDRAM, DDR, RDRAM and SLDRAM); CX2735 at 24-25 (Micron roadmap for SDRAM, DDR, SLDRAM and RDRAM); Lee, Tr. 6719-29, 6740-44).

4. After Rambus Pressured Hyundai Into Withdrawing From the SyncLink Consortium, the SyncLink Consortium Was Disbanded.

1582. In late 1998, Rambus CEO Geoff Tate suggested to Hyundai executive Dr. Oh that Hyundai stop participating in the SyncLink Consortium. (CX2107 at 109-110 (Oh, Dep.)

(“Rambus claimed that SyncLink is hurting them, and so suggest me to stop SyncLink, ask me to stop, suggest me.”); *see also* Tabrizi, Tr. 9183 (“My executives were continuously getting complaint from both Rambus and Intel that Farhad is pushing SLDRAM and they want us to – they want Hyundai to ask Farhad to resign.”)). Mr. Tate explained to Dr. Oh that, by playing an active role in the SyncLink Consortium, Hyundai hurt Rambus’s business. (CX2107 at 115-16 (Oh, Dep.)).

1583. Because Intel supported Rambus at that time, Dr. Oh believed he had no choice but to produce RDRAM. (CX2107 at 117 (Oh, Dep.) (“Intel supported Rambus, so at that time no choice. As a – one of the large manufacturer of DRAM, I had to produce Rambus DRAM . . .”)). In order to produce RDRAMs, Dr. Oh believed that Hyundai needed to have support from Rambus. (CX2107 at 118-19 (Oh, Dep.)).

1584. Dr. Oh believed that he would not get full support from Rambus unless Hyundai withdrew from the SyncLink Consortium. (CX2107 at 119 (Oh, Dep.)).

1585. In order to satisfy Rambus, Dr. Oh instructed Mr. Tabrizi to resign from the SyncLink Consortium. (CX2107 at 117 (Oh, Dep.) (“ . . . in order to satisfy Mr. Tate and satisfy rambus request, I asked Mr. Tabrizi to resign.”); Tabrizi, Tr. 9183-84 (“Q: And did Dr. Oh instruct you to resign from SyncLink? A: Yes, he did.”)).

1586. In 1999, after Mr. Tabrizi resigned, the SyncLink Consortium was disbanded. (Tabrizi, Tr. 9183).

1587. The SyncLink architecture was not accepted within the industry and never went into volume production. (Appleton, Tr. 6319; Tabrizi, Tr. 9184 (“Q: Now, did Hyundai ever produce SyncLink in commercial quantities? A: Never.”); Peisl, Tr. 4492 (“Q: Did SyncLink ever result in the production of a product? A: Not to my knowledge.”)).

1588. Paragraphs 1588 - 1599 are unused.

UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION

In the Matter of

RAMBUS INCORPORATED,

a corporation.

Docket No. 9302

COMPLAINT COUNSEL'S
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FINDINGS OF FACT,
CONCLUSIONS OF LAW
AND ORDER

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**COMPLAINT COUNSEL’S
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**UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION**

In the Matter of

RAMBUS INCORPORATED,

a corporation.

Docket No. 9302

**COMPLAINT COUNSEL'S
PROPOSED FINDINGS OF FACT**

Volume II

VIII. After Rambus Withdrew from JEDEC, It Continued to Promote Its Proprietary Technology, While Secretly Preparing to Assert Patent Claims Against JEDEC Standard Technology.

A. Intel's Endorsement of RDRAM in Late 1996 Placed DRAM Manufacturers Under Economic Pressure to Sign Licenses with Rambus and Support RDRAM Technology.

1600. In late 1995, Intel decided it would support the proprietary Rambus RDRAM technology with the next generation of Intel microprocessors. (RX1532 at 1 (Intel timeline: "December '95: chose RDRAM as the direction we would pursue")).

1601. In order to pacify companies that were unhappy with Rambus's exclusive control over the RDRAM architecture, Rambus considered forming a Rambus "standards committee" called REDEC. (Crisp, Tr. 2939-2940; CX0902 at 1 (Garrett August 1996 email: "I have put a strawman proposal in you mailboxes, "High Performance Memory Open Standards Committee"); CX0903 at 1 (Crisp August 1996 email: "This is about pacification of our partners, pure and simple . . . there is a lot of resentment within our DRAM partners")).

1602. Richard Crisp, Rambus's primary JEDEC representative, argued against REDEC

because if “REDEC was modeled at all like JEDEC, then there would be an expectation” that the organization was developing “standards which steer clear of patents.” (CX0903 at 2; Crisp, Tr. 2942). Crisp believed REDEC would be in direct conflict with Rambus’s goal of collecting licensing fees and royalties on its intellectual property. (CX0903 at 2-3 (Crisp August 1996 email: REDEC “sounds pretty good on the surface but I see several problems: 1) Open standards seem at odds with our business model . . . I just cannot visualize how it could be turned into anything resembling JEDEC, do meaningful work, and not be in direct conflict with our business model.”)). Mr. Crisp acknowledged that “[t]he most valuable patents are ones that must be used in order to be in compliance with a standard.” (*Id.* at 2; Crisp, Tr. 2939).

1603. In late 1996, Intel announced that its future desktop PC chipsets would only work with RDRAM. (RX1532 at 2 (Intel timeline: “December ‘96: Communicated that we had chosen RDRAM and signed a license with RamBus to memory vendors”); Hampel, Tr. 8677-78; Tabrizi, Tr. 9135; Crisp, Tr. 3432-33; CX2634 at 1 (Microprocessor Report article from April 1997 noting “Intel’s adoption of Rambus’s Direct RDRAM as its next-generation main-memory technology for PC’s”)).

1604. During the beginning of the Rambus-Intel partnership, Intel hoped that Rambus would have a good relationship with the DRAM industry. (MacWilliams, Tr. 4871 (“what we had hoped for and what we had worked for actually in the first few years of this deal was to try and make Rambus a value-added part of this whole industry infrastructure”)). Intel envisioned an industry infrastructure where DRAM vendors built DRAMs, Intel built chipsets, and “Rambus provide[d] all of the glue to make the enabling pieces work and therefore [] would be perceived as valuable.” (MacWilliams, Tr. 4871).

1605. Projected demand for RDRAM increased sharply after Intel announced it would produce chipsets that used RDRAM. (Hampel, Tr. 8677-78 (Rambus saw an increase in customer interest after Intel endorsed RDRAM: “There were more customers interested. We did increase kind of the workload . . . to support the effort”); CCF 1607, 1802, 1806-08)).

1606. Because RDRAM was expensive to produce and Rambus demanded high royalty rates, some members of the DRAM industry were surprised and concerned about Intel’s decision to endorse Rambus. (Appleton, Tr. 6344 (Micron’s Chairman of the Board and CEO Steven Appleton was surprised to learn that Intel had endorsed Rambus’s Direct RDRAM technology because “there were better alternatives to pursue” and “it would be a relatively high cost to the DRAM industry to do it.”); Tabrizi, Tr. 9044, 9135 (Hynix Vice President Farhad Tabrizi was very concerned about Intel’s decision to support RDRAM because he believed in open standards and felt the industry would be stuck with a very costly device to manufacture)).

1607. Despite concerns, Intel’s support of RDRAM forced Micron to engage in licensing negotiations with Rambus. (Appleton, Tr. 6345-46 (“once Intel endorsed [] RDRAM, then the probabilities of customers in the marketplace actually using it increased quite a bit, and

as a result, we also then believed that some customers would use RDRAM and that we needed to then engage to negotiate for a license.”)).

1608. In February 1997, Rambus and Samsung narrowed the scope of their prior RDRAM license agreement by eliminating the “other use clause.” (CX0914 at 1 (Tate December 1996 email: reporting an “agreement on a much narrow[er] deal,” pursuant to which Samsung was forbidden to use Rambus IP for any “competitive DRAMs”); CX0918 at 1 (Tate February 1997 email discussing a meeting with Samsung: “we both signed the contract (finally)”); CCF 741)).

1609. One by one, DRAM manufacturers signed Direct RDRAM license agreements with Rambus. (CCFF 1611-15).

1610.
(CX2699 at 1, *in camera*).

1611. In February 1997, Mitsubishi signed a license agreement with Rambus covering Direct RDRAM. (CX1609 at 1-19). The subject matter of the Mitsubishi agreement was limited to Rambus-compatible DRAMs and interfaces. (*Id.* at 1-2).

1612. In March 1997, Hyundai amended its RDRAM license agreement with Rambus to include Direct RDRAM. (CX1612 at 1-7; CX1599 at 1-23; CX1600 at 1-22 (original RDRAM license agreement between Hyundai and Rambus dated December 1995)). Hyundai’s new agreement included royalties on Direct RDRAM ranging from 1.5% to 2.0% depending on the sale date. (CX1612 at 5).

1613. In March 1997, Micron signed a license agreement with Rambus covering Direct RDRAM. (CX1646 at 1-20). Micron agreed to pay royalty rate up to 2% on next generation RDRAM. (CX1646 at 11).

1614. Micron was forced to sign a license agreement for Direct RDRAM under “economic pressure.” (Appleton, Tr. 6346-47 (“We felt that with Intel’s endorsement, that there would be a customer base that would use the product, and we needed to be in a position to make whatever product that the customer decided that they were going to use for their platforms.”); Lee, Tr. 6870, 6615 (Micron was forced to sign a license agreement with Rambus in keep up with Intel’s projection of using RDRAM across its product lines)).

1615. In July 1997, Siemens AG signed a license agreement with Rambus covering RDRAM. (CX1617 at 1-22; CX2088 at 62 (Tate, Infineon Trial Tr.)).

B. Rambus Attempted to Persuade Companies to Stop Developing Alternative Technologies That Competed with RDRAM.

1616. From 1996 through 1998, Rambus attempted to get DRAM manufacturers to agree not to support alternatives to RDRAM. (CCFF 1617-18, 1620, 1623).

1617. Rambus considered offering Samsung warrants for 250,000 shares of Rambus stock in exchange for working exclusively on RDRAM. (CX0981 at 4 (Tate December 1997 email: “we should offer [Samsung] 250K warrants in return for their commitment NOW to drop ddr”); CX0983 at 1 (Tate December 1997 email: “we give [Samsung] warrants for 250K shares at the market price . . . as long as they have not developed or worked on any competitive memory interface technology”)).

1618. Rambus offered Micron, Samsung, and Lucky Goldstar (“LG”) preferential RDRAM license terms in exchange for “dropping” development work on other DRAMs. (Appleton, Tr. 6342-43; RX0828 at 1 (December 1996 letter from Rambus to Micron: “if Micron wants to increase the commitment a step further to put ‘all your wood behind one arrow’ with Rambus as your sole effort for high-bandwidth DRAMs . . . then in return we can slash our fee for our license”); CX0956 at 2-3 (Tate September 1997 email: “if samsung was willing to consider dropping ddr, synlink and announcing that after sdram-100 that rambus is their only dram strategy then we could talk about . . . rewards to samsung”); CX0957 at 1-2 (Rambus proposed to Korean DRAM maker LG that if it were to “cancel ddr” and commit to fully support RDRAM, then Rambus “could consider some [RDRAM] royalty breaks for 98 in return.”); CX0966 at 1 (Tate November 1997 email considering LG’s request to lower RDRAM royalty rates: “tie to agreement to NOT do ddr/sldram and public announcement of this NOW”)).

1619. Micron “responded negatively” to Rambus’s request to stop developing non-Rambus DRAM because Micron CEO Steve Appleton did not want to limit the company to one path. (Appleton, Tr. 6343).

1620. In early 1998, Rambus CEO Geoffrey Tate met with Hyundai senior executive vice president Dr. Oh and suggested that Hyundai stop participating in the SyncLink Consortium. (CX2107 at 110-111 (Oh, Dep.)).

1621. Dr. Oh wanted to maintain good relations with Rambus because Intel supported Rambus. (CX2107 at 117 (Oh, Dep.) (“Intel supported Rambus, so . . . [as] one of the large manufacturers of DRAM, I had to produce Rambus DRAM”)). In order to produce RDRAMs, Hyundai needed support from Rambus. (CX2107 at 119 (Oh, Dep.)).

1622. Dr. Oh feared that he would not get full technical support from Rambus unless Hyundai withdrew from the SyncLink Consortium. (CX2107 at 119 (Oh, Dep.)).

1623. In 1998, Hyundai stopped participating in the SyncLink Consortium. (CX2107 at 109 (Oh, Dep.)). Dr. Oh instructed Farhad Tabrizi to resign from SyncLink “in order to satisfy

Mr. Tate and satisfy Rambus[’s] request.” (CX2107 at 117 (Oh, Dep.); Tabrizi, Tr. 9183-84).

1624. Hyundai never commercially produced SyncLink and, after Hyundai withdrew its support, SyncLink “kind of died.” (Tabrizi, Tr. 9183-84).

C. After its Withdrawal from JEDEC, Rambus Secretly Monitored the Activities at JEDEC and Synlink Even As It Continued To Amend and Prosecute its Patent Applications.

1625. Rambus continued to follow JEDEC’s activities after it submitted its withdrawal letter in June 1996. (Crisp, Tr. 3388; CX0888?at 1).

1626. Several sources leaked information to Rambus about JEDEC meetings after Rambus withdrew from JEDEC. (Crisp, Tr. 3413). In 1997 Richard Crisp, Rambus’s principal JEDEC representative, received information about JEDEC’s activities from a source called “deep throat.” (Crisp, Tr. 3414; CX0929 at 1; CX0932 at 1 (Crisp June 1997 email: “My ‘deep throat’ (DT) source told me that the DDR bandwagon is moving fast within JEDEC with all companies participating.”)). Crisp also received information relating to proceedings at JEDEC from an anonymous source called “Mixmaster,” a reporter Crisp called the “Carroll contact,” and a source known as “Secret Squirrel.” (Crisp, Tr. 3414-3417; CX0953 at 1; CX0935 at 1 (“More stuff from the Carroll contact”)).

1627. Mr. Crisp shared JEDEC-related information he received from Deep Throat, the Carroll Contact, Mixmaster, and other sources with Rambus executives and engineers. (Crisp, Tr. 3413-3417; CX0935 at 1 (Crisp email regarding “more stuff on taipei jedec meeting”); CX0929 at 001; CX0932 at 1 (June 1997 email from Crisp to Rambus’s entire executive group and others within Rambus entitled “JEDEC G2,” referring to a type of intelligence); CX0973 at 1 (“some JEDEC G2”); CX0979 at 1 (“jedec G2 . . . no discussion of any Rambus patents that my source heard either officially or unofficially”); CX1014 at 1 (“other G2 regarding JEDEC . . . I had lunch with a JEDEC guy (frequent source of information)”)).

1628. After its withdrawal from JEDEC, Rambus used the information that Mr. Crisp gathered in the process of amending the scope of its patent claims. (Crisp, Tr. 3417-18).

1629. After June 1996, Rambus continued to follow SyncLink’s activities. (Crisp, Tr. 3388-89; Crisp, Tr. 3395-3396; CX0711 at 183).

1630. After June 1996, Rambus continued its efforts to secure patent rights over SyncLink. In August 1996, Mr. Crisp again urged upon Rambus management “the importance that we have our issued patents and any pending claims looked at long and hard” to anticipate the SyncLink standard. (CX0711 at 185). Mr. Crisp stated that it probably would not matter if SyncLink was successful “[a]s long as we collect big royalty checks every quarter.” (*Id.*)

D. Rambus Continued Efforts to Obtain Patents Covering the Technologies Presented at JEDEC.

1631. After withdrawing from JEDEC in June 1996, Rambus continued its efforts to perfect patent rights over the programmable CAS latency, programmable burst length, dual edge clock and on-chip PLL/DLL technologies. (CCFF 1632-1667).

1632. At the time Rambus withdrew from JEDEC, it already had an issued patent containing claims covering uses of dual edge clock technology in synchronous DRAMs. After withdrawing from JEDEC, Rambus filed additional applications in order to obtain additional patents with claims relating to use of dual edge clock technology. (CCFF 1216-37, 1634-40).

1633. Rambus filed the '646 application on March 31, 1994. The '646 application is a continuation of application number 07/954,945, which is a continuation of the '898 application. (CX1493 at 2; Nusbaum, Tr. 1596).

1634. Rambus patent application 08/222,646 (the '646 application) issued as Rambus patent no. 5,513,327 (the '327 patent) on April 30, 1996. It claims priority based on the original '898 application and can trace its lineage through the '646 application. (CX1494 at 1; First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

1635. Rambus's '327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature proposed to JEDEC in May 1992, December 1995 and March 1996 in a JEDEC-compliant SDRAM. (Jacob, Tr. 5545-49; CCFF 1216-23, 1229-33).

1636. The '327 patent also contains claims covering DDR SDRAM as described in JEDEC Specification JESD 79 (June 2000). (Jacob, Tr. 5550-60; CCFF 1224-28, 1234-37).

1637. On February 19, 1999, Rambus filed application no. 09/252,998 ("the '998 application"), which traced back to the '646 application. The '327 patent was listed under related U.S. application data. (CX1523 at 1).

1638. On February 29, 2000, the '998 application issued as patent no. 6,032,214 ("the '214 patent"). (CX1523).

1639. Independent claims 1 and 15 of the '214 patent relate to outputting data with respect to a first and a second clock signal. (CX1523 at 29 (Claim 15 recites: "A method of operation of a synchronous memory device . . . wherein a first portion of the first amount of data is output synchronously with respect to the first external clock signal and a second portion of the first amount of data is output synchronously with respect to the second external clock signal.")).

1640. Rambus has taken the position that claims 1 and 15 of the '214 patent cover use of double data rate in combination with variable block or burst size. (CX1371 at 64-70 (comparing claim 1 of the '214 patent to the mode register and timing diagrams of a JEDEC DDR SDRAM data sheet); CX1383 at 60, 63-66 (same); *see also* Rambus Brief, *Rambus Inc. v. Infineon Technologies AG*, (Feb. 1, 2001), at 7-8 (Judicial Notice taken, Tr. 1581-82, marked by not admitted as CX1877) (the "double data rate" invention "allow[ed] data to be sent out on both the tick and the tock (the rising and falling edges) of the clock"; "Claim 15 of the '214 is a representative claim covering the double data rate invention in combination with the variable block size (burst) described above.")).

1641. After Rambus withdrew from JEDEC, it continued to prosecute a pending patent application containing claims covering uses of an on-chip phase lock loop circuit in synchronous DRAMs. Rambus also filed additional patent applications containing claims relating to on-chip PLL/DLL technology after it withdrew from JEDEC. (CCFF 1642-48).

1642. Beginning in June 1993 and continuing throughout the time that Rambus was a member of JEDEC, Rambus patent application 07/847,692 (the '692 application) contained claim 151 that a reasonable engineer could interpret as covering, a phase lock loop (PLL) incorporated into a JEDEC-complaint synchronous DRAM. (Nusbaum, Tr. 1582-95; Jacob, Tr. 5533-41).

1643. Rambus filed application no. 08/749,729 (the '729 application) as a continuation of the '692 application on November 15, 1996. Rambus included claim 151 of the '692 application as claim 151 in the new '729 application. (CX1502 at 305-13, 319; CX1459).

1644. The '729 application issued as the 5,657,481 (the '481) patent on August 12, 1997. (CX1503 at 1). Claim 151 of the '729 application became claim 1 of the '481 patent. (CX1503 at 26; CX1502 at 306).

1645. At the time the '481 patent issued, Rambus described the patent in internal documents as containing an independent claim covering a memory device that includes phase lock loop circuitry. (CX0948 ("The 5 independent claims cover the following: (a) A memory device that . . . includes phase locked loop circuitry which varies the delay of the local clock signal to create an internal, synchronized clock to operate the interface circuitry on the memory device."); *see also* CX1244 at 1 ("pll-on-a-memory-device patents/'481"))).

1646. On February 10, 1997, Rambus filed patent application no. 08/798,525 (the '525 application). This application issued as Rambus patent no. 5,954,804 (the '804 patent) on September 21, 1999. The '804 patent claims a priority date of April 18, 1990 based on the original '898 application and traces its history through the '961 and '490 applications, which it lists as related applications. (CX1518 at 1; First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

1647. Claim 26 of the '804 patent relates to delay lock loop circuitry. (CX1518 at 31 (Claim 26 recites, "An integrated circuit device . . . [that] comprises: . . . delay locked loop circuitry to generate an internal clock signal using the first and second external clock signals")).

1648. Rambus has taken the position that the '804 patent covers use of delay lock loop technology in combination with programmable CAS latency. (Rambus Brief, *Rambus Inc. v. Infineon Technologies AG*, (Feb. 1, 2001), at 9 (Judicial Notice taken, Tr. 1581-82, marked but not admitted as CX1877) ("Claim 26 of the '804 patent is a representative claim covering the delay locked loop invention in combination with [programmable CAS] latency")).

1649. From January 1995 until February 1996, Rambus had claims in pending patent applications, the 07/847,961 (the '961 application) and the 08/469,490 (the '490 application), that contained claims covering the programmable CAS latency feature of a JEDEC compliant SDRAM or its use. (CCFF 1127-82).

1650. Not long after Rambus withdrew from JEDEC, Rambus renewed its attempts to obtain a patent containing claims covering programmable CAS latency in synchronous DRAMs. (CCFF 1651-61).

1651. Claims 183-185 of the '490 application covered a JEDEC-compliant SDRAM having programmable CAS latency, a computer system using that SDRAM, or a method of programming it. (Nusbaum, Tr. 1574-81; Jacob, Tr. 5528-32).

1652. Rambus cancelled claims 183-185 of the '490 application on February 26, 1996 in response to a restriction requirement by the patent examiner. (CX1504 at 279) ("Please cancel claims . . . 183-185 without prejudice to the filing of continuations or divisionals"). However, Rambus resubmitted those claims to the PTO in application 08/798,520, which also claims priority to the '898 application. (CX1509 at 187-89; CX1504 at 264-266; First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; *see also* DX0014).

1653. On February 10, 1997, Rambus filed its 08/798,520 patent application (the '520 application). The '520 application was divisional of the 08/448,657 patent application ("the '657 application"), which in turn was a divisional application of the '646 application. (CX1509 at 184). The '520 application claims priority based on the '898 application. (First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

1654. On February 10, 1997, Rambus submitted to the PTO a Preliminary Amendment to the '520 application adding claims 156-158. (CX1509 at 184). The text of claims 156-158 in the '520 application is identical to the text of claims 183-185 in the '490 application. (CX1504 at 264-266; CX1509 at 187-88, 189 ("This divisional application includes claims 156-158 which correspond to claims 183-185, respectively, from related application Serial No. 08/469,

490 filed June 6, 1995 . . .’)).

1655. On January 20, 1998, Rambus amended claim 156 of the ‘520 application. (CX1509 at 227). Rambus did not represent that the amendment changed the scope of claim 156. (CX1509 at 231-35, and specifically at 232 (the purpose of the amendment was “to further prosecution of the claimed invention.”)).

1656. The patent examiner allowed claim 156 of the ‘520 application in this form. It became claim 1 of Rambus patent 5,841,580, (the ‘580 patent), which issued on November 24, 1998. (CX1510 at 1, 29).

1657. On November 20, 1998, Rambus filed application no. 09/196,200 (“the ‘200 application”), which was a continuation of the ‘520 application. (CX1507 at 96).

1658. The patent examiner rejected claim 151 of the ‘200 application because it was not patentably distinct from claim 1 of the ‘580 patent and thus constituted double patenting. (CX1507 at 88 (“Claim 151 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 5,841,540 [5,841,580]. Although the conflicting claims are not identical, they are not patentably distinct from each other because the bus transaction request would include the read request.”)).

1659. In order to overcome the patent examiner’s double patenting objection, Rambus submitted a terminal disclaimer for the ‘200 application that disclaimed the term of any patent beyond the expiration date of the ‘580 patent. (CX1507 at 76).

1660. Following the terminal disclaimer, the examiner allowed the ‘200 application, which issued as Rambus patent 5,953,263 (“the ‘263 patent”) on September 14, 1999. (CX1517 at 1; CX1507 at 32). Claim 151 of the ‘200 application issued as claim 1 of the ‘263 patent. (CX1507 at 98; CX1517 at 29).

1661. Rambus has taken the position that claims contained in the ‘263 patent cover use of programmable CAS latency. (CX1383 at 13 (applying elements of claim 18 of the ‘263 patent to the CAS latency portion of a mode register diagram); CX1371 at 16-18, 21-22, 24 (stating that a programmable mode register that includes bits specifying the read latency infringes the ‘263 patent); *see also* Rambus Brief, *Rambus Inc. v. Infineon Technologies AG*, (Feb. 1, 2003), at 5-6 (Judicial Notice taken, Tr. 1581-82, marked but not admitted as CX1877) (the ‘263 patent applies to use of programmable CAS latency because “a programmable register can be added to a DRAM chip to establish a known delay time or latency” and that “Claim 1 of the ‘263 patent is a representative claim covering this invention.”)).

1662. While a member of JEDEC, Rambus had claims in the ‘961 patent application that covered the programmable burst length feature of a JEDEC compliant SDRAM or its use.

(CCFF 1125-39, 1148-53, 1158-61).

1663. After withdrawing from JEDEC, Rambus renewed its attempts to obtain a patent containing claims covering programmable burst length in synchronous DRAMs. (CCFF 1664-67).

1664. On February 19, 1999, Rambus filed patent application no. 09/252/997 (“the ‘997 application”). The ‘997 application traced its lineage through the ‘646 application back to the ‘898 application. The ‘327 was listed as related U.S. application data. (CX1525 at 1; *see also* First Stipulation, No. 22; Exhibit A to First Stipulations, No. 22; Nusbaum Tr. 1506-1508; *see also* DX0014)).

1665. On March 7, 2000, the ‘997 application issued a U.S. patent no. 6,034,918 (the ‘918 patent). (CX1525).

1666. Claims 1 and 18 of the ‘918 patent relate to programmable block size. (CX1525 at 30 (Claim 18 recites: “A method of operation of a synchronous memory device, wherein . . . the method of operation of the memory device comprises: . . . receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request . . .”).

1667. Rambus has taken the position that claims of the ‘918 patent cover use of programmable burst length. (CX1383 at 36, 43 (applying elements of claims 1 and 8 (a dependent claim of claim 1) of the ‘918 patent to the burst length portion of a mode register diagram); CX1371 at 91-94, 97 (stating that a programmable mode register that includes bits specifying the burst length infringes the ‘918 patent); *see also* Rambus Brief, *Rambus Inc. v. Infineon Technologies AG*, (Feb. 1, 2001), at 5-6 (Judicial Notice taken, Tr. 1581-82, marked but not admitted as CX1877) (stating that claims of the ‘918 patent cover programmable burst length because “additional circuitry (allowing for a programmable block or burst size) can be added to the prior art DRAM chip so as to allow for the output of a variably sized block of data (or burst of data) . . .” and that “Claim 18 of the ‘918 patent is a representative claim covering this invention.”)).

1668. Complaint Counsel lacks information about Rambus’s understanding of any of the above-listed patents and applications, or other patents in the ‘898 family that Rambus has asserted against SDRAM and DDR SDRAM, because Rambus has asserted attorney-client and work product privileges with respect to all correspondence to, from or among attorneys (other than correspondence to or from the PTO) relating to the prosecution of these patents. (Steinberg Motion *In Limine*, Attachment 9, Rambus Privilege Log Entries).

1669. After leaving JEDEC in June 1996, Rambus continued to prosecute patents at foreign patent offices. (CX1496 at 1; CX1499 at 1; CX1506 at 1; CX1511 at 1; CX1515 at 1;

CX1519 at 1; CX1527 at 1; CX1529 at 1; CX1533 at 1; CX1535 at 3; CX1536 at 1; Crisp, Tr. 3405).

1670. A Korean Patent No. titled, “Integrated Circuit I/O Using a High Performance Bus Interface,” was granted in 1999. (CX1515 at 1). That patent claims priority based on Rambus’s original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

1671. German Patent No. 9117296.9 was granted on April 6, 2000. (CX1527 at 1). That patent claims priority based on Rambus’s original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

1672. European Patent No. EP 0525068 B1, entitled “Semiconductor Memory Device,” was granted April 19, 2000. (CX1529 at 1). That patent claims priority based on Rambus’s original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

1673. European Patent No. EP 1004956B1, entitled “Method of operating a synchronous memory having a variable data output length,” was granted on January 3, 2001. (CX1533 at 2). That patent claims priority based on Rambus’s original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

1674. European Patent No. EP 1022642B1, entitled “Integrated circuit I/O using a high performance bus interface,” was granted on September 5, 2001. (CX1536 at 1). That patent claims priority based on Rambus’s original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

1675. Complaint Counsel has limited information regarding the prosecution of all foreign patents because Respondent has asserted attorney-client privilege with respect to work involving foreign filings. (Vincent, Tr. 7879). There are well over one hundred communications regarding Rambus’s foreign patent filings between July 1996 and early 2000 that were not produced to Complaint Counsel because Respondent asserted the attorney-client privilege. (Steinberg Motion *In Limine*, Attachment 9, Rambus Privilege Log Entries: 52-100, 105-113, 115, 132-137, 154-156, 158-164, 166-173, 177-180, 206-227, 248-259).

E. Rambus Continued to Conceal Its JEDEC-Related Intellectual Property after its Withdrawal from JEDEC.

1676. After its withdrawal from JEDEC, Rambus continued to conceal from the DRAM industry that it believed SyncLink and DDR SDRAM infringed Rambus patents. (CX0939 at 1 (Davidow July 1997 email: “One of the things we have avoided discussing with our partners is intellectual property problem discussed in the fourth paragraph [referring to Rambus’s thinking

that SLDRAM and SDRAM DDR infringed Rambus's patents]"; CX2109 at 149-50 (Davidow, Dep.); CX0936 at 1 (Davidow July 1997 email: "We have not discussed [possible infringement] with the DRAM manufacturers. We hope we never have to."); CX2109 at 136-138 (Davidow, Dep.); CX0942 at 1 (Tate August 1997 email: "our policy so far has been NOT to publicize our patents and i think we should continue with this.")).

1677. In early 1997, Rambus held a DDR threat assessment meeting. (CX0919 at 1; Crisp, Tr. 3403-3404). In an email summarizing the meeting, Rambus CEO Geoffrey Tate stated, "There are many issued and in-process patents that DDR SDRAMs/SGRAMs *might* infringe." (CX0919 at 1 (asterisks in original)).

1678. In response to the DDR threat assessment meeting, Mr. Tate instructed his staff "NOT" to tell people that Rambus felt DDR may infringe its patents. (CX0919 at 1 ("1. keep pushing our patents through the patent office 2. do *NOT* tell customers/partners that we feel DDR may infringe – our leverage is better to wait"); Crisp, Tr. 3408 ("Mr. Tate had explained to people . . . that he didn't want us to make any allegations that there might be some infringement. . . . we were basically told to not be telling customers and partners that we think DDR might infringe our patents.")).

1679. During Rambus's licensing negotiations with Micron in early 1997, Rambus never told Micron that its patent rights extended or might extend beyond direct RDRAM. (Appleton, Tr. 6350 ("Never during the discussion that we had with Rambus on the license for RDRAM did they ever indicate, ever say that somehow [] the patents that were part of RDRAM had any application to anything else besides RDRAM"))).

1680. During Rambus's licensing negotiations with Micron in early 1997, Rambus never told Micron that Rambus believed it possessed, or would be able to obtain patent rights extending to any aspect of SDRAM. (Appleton, Tr. 6348; Lee, Tr. 6619). In early 1997, Rambus knew that Micron was working on SDRAM. (Appleton, Tr. 6351). During this time period, Micron would have considered it important to know if Rambus believed it possessed patent rights over an aspect of SDRAM. (Appleton, Tr. 6352).

1681. During Rambus's licensing negotiations with Micron in early 1997, Rambus never told Micron that Rambus believed it possessed, or would be able to obtain patent rights extending to SyncLink DRAM technology. (Appleton, Tr. 6353).

1682. During Rambus's negotiations with Siemens in 1997, Rambus never told Siemens that it thought DDR SDRAM and SyncLink would infringe Rambus patents. (CX0937 at 1; CX0939 at 1 (Mooring July 1997 email: "We have not yet told Siemens that we think SLDRAM and SDRAM-DDR infringe our patents. We think that will just irritate them. Hopefully, SLDRAM and DDR will die due to their technical/infrastructure faults so we don't have to play that card."); CX2109 at 144 (Davidow, Dep.); CX2088 at 75-77 (Tate, Infineon Trial Tr.)).

1683. During a 1997 meeting between Rambus and Korean DRAM maker LG, an LG executive explained to Mr. Tate that LG's reason for favoring DDR was that it understood DDR to be a "royalty-free . . . open, jedec standard." (CX0957 at 1). It appears that Mr. Tate did nothing to disabuse LG's beliefs regarding the "open" and "royalty-free" nature of JEDEC's DDR SDRAM standard. (*Id.* at 1-2).

1684. In August 1997, Rambus believed that people did not understand the significance of the 5,513,327 patent, which included claims related to moving data on the rising and the falling edges of the clock. (CX1494; CX0942 at 1 (Tate August 1997 email: "we already have the 327 patent but few people are aware of what it means."); Diepenbrock, Tr. 6145-46; Hampel, Tr. 8732-33 (Mr. Hampel could not recall any instance in which Rambus representatives told the DRAM manufacturers which features of RDRAM were protected by Rambus patents or patent applications)). Rambus had omitted the '327 patent from its June 1996 JEDEC withdrawal letter. (CX0888 at 1-2).

1685. Rambus believed that "competitive solutions" such as DDR SDRAMs and SLDRAMs would likely infringe its '327 and new '481, PLL/DLL on DRAM patent. (CX1503 (Rambus's 5,657,481 patent issued on August 12, 1997); Diepenbrock, Tr. 6183; CX0942 at 1 (Tate August 1997 email: "ddr/sldram are likely to infringe" these two patents)).

1686. Eight days before the 5,657,481 patent issued, Mr. Tate reminded his staff that Rambus's policy had been "NOT to publicize our patents" and suggested that staff continue this approach. (CX0942 at 1). Mr. Tate further instructed his staff to prepare a position statement in case Rambus received calls from the press when the new patent issued. (*Id.*)

1687. Rambus employees created a "party line" to help address any inquiries about the newly issued 5,657,481 patent, which avoided comment directly on whether SDRAMs or DDR SDRAMs infringed the patent. (CX0948 at 1; CX0947 at 1 ("Q3: Do Double Data Rate (DDR) SDRAMs use this patent? A: We don't know yet. No DDR products exist for us to evaluate.")).

1688. During the same timeframe that Rambus was concealing its JEDEC-related intellectual property from the DRAM industry, Rambus made limited, private disclosures to its partner, Intel. (CCFF 1694-95).

1689. In August 1996, Rambus was concerned that Intel might support 200 Mhz SDRAMs. (CX0898 at 1 (Barth August 1996 email discussing concern with Intel supporting 200MHz SDRAMs)). At the time, Rambus CEO Geoffrey Tate suggested that one way to deal with this threat might be to alert Intel that, among other "potential problems," these devices might infringe upon Rambus patents. (CX0897 at 1 (Tate August 1996 email: "my gut-level inclinations on an action plan . . . send intel a rambus assessment on 200mhz sdram raising the potential problems we see with feasibility, risk and compatability; *AND* point out that we

have issued patents that this proposal could very well infringe”)).

1690. In the second half of 1997, Rambus was concerned that Intel was considering supporting DDR through a DDR-compatible chipset. (CX0942 at 1). Rambus believed that Intel could be scared into a DDR program because Intel’s principal chipset rival – VIA – was itself “aggressively promoting DDR.” (CX0968 at 1 (Crisp November 1997 email suggesting that VIA’s support for DDR, along with the support of other companies, had Intel worried and could cause Intel to “be scared into doing a DDR program.”); *see also* CX0655 at 1 (“certain groups within Intel are supposedly talking about DDR for main memory”)).

1691. Rambus planned to persuade Intel not to develop a chipset that would support DDR SDRAM memory. Rambus CEO Geoffrey Tate suggested that Rambus “meet with intel . . . to get them aware that IF they were to consider a DDR chipset that there is a minefield of 60+ rambus patents that would have to be avoided – we convince them 2 of the mines are real but not give them a map to the whole minefield.” (CX0942 at 1).

1692. In August 1997, Rambus CEO Geoffrey Tate wrote to his colleague David Mooring laying out strategies for convincing Intel not to develop a DDR chipset. (CX0946 at 1; CX1244 at 1 (Tate August 1997 email titled “parker/gelsinger; ddr crush plan”: “i think we need to make it clear to them that we aren’t going to make any significant further changes in our business deal with them without their decision they are not doing a ddr backup chipset period.”)). Mr. Tate stated, “they need to know that a ddr backup chipset is first real bad for their objectives and second one that we cannot accept under our original make-us-king deal.” (*Id.*) Mr. Tate also suggested that Tony Diepenbrock was ready, willing, and able to “educate” Mooring on Rambus’s “double-data-rate/327 and pll-on-a-memory-device patents/481.” (*Id.*)

1693. In January 1998, Rambus executives considered telling Intel that they believed DDR and SLDRAM infringed Rambus patents in order to discourage Intel from developing non-Rambus technologies. (CX0984 at 3 (Tate January 1998 email: “should we also disclose our position on patents and that we believe ddr’s/sldram/etc will likely infringe our patents? this is to show that whatever path the market takes it infringes our IP. should we tell intel this?”)).

1694. In late 1997 or early 1998, Rambus informed Intel in general terms that Rambus might have patent applications that would cover DDR SDRAMs, but did not provide any specific details. (MacWilliams, Tr. 4905 (“We were related this notion that [Rambus] might have something, but we were given nothing concrete. We had no specifics on what they had patents applications on. We had no patent applications in-house to look at. So it was kind of a piece of information with no immediate relevance.”)).

1695. Intel had non-disclosure agreements with Rambus that prevented it from sharing Rambus confidential information with third parties. (Calvin, Tr. 1018; CX0993 at 1 (Tate

January 1998 email: our rdram partners “CANNOT disclose our confidential information to 3rd parties . . . Our partners’ employees working on competitive products, e.g. DDR, might have access to our confidential information. they might even go to committees like jedec to discuss DDR. BUT they are obligated as employees of our partners’ to keep our confidential information secret”).

1696. In early 1998, Rambus considered, but rejected, making public statements about DDR infringing Rambus patents. (CX0987 at 4 (Tate January 1998 email: “ddr infringes our patents (question: do we start saying this publicly?)”).

1697. Rambus was still concealing its JEDEC-related intellectual property in 1999. (CX1075 at 2 (interview with Rambus CEO Geoffrey Tate: “We’ve made no comment on whether DDR infringes our patents. . . . Our position is there is insufficient data.”); CX1089 at 1 (in December 1999, Mr. Tate advised his colleagues that, if asked questions about the potential for DDR to infringe Rambus patents, “it’s important NOT to indicate/hint/wink/etc what we expect the results of our [infringement] analysis to be!!!”).

1698. Most people in the DRAM industry believed that RDRAM and DDR SDRAM were very different technologies. (CX2749 at 1-3 (October 1999 article describing the difference between the clocking of DDR SDRAM and the clocking of RDRAM); CCFF 748, 751-53, 1281)).

1699. Before late 1999, most people in the DRAM industry did not believe that Rambus’s patents applied to SDRAMs or DDR SDRAMs. (CX2107 at 69 (Oh, Dep.); Bechtelsheim, Tr. 5841-42, 5880-81; Sussman, Tr. 1455; Kellogg, Tr. 5060; CCFF 1698)).

1700. Rambus Vice President of Intellectual Property Joel Karp even acknowledged that most of the DRAM industry did not think Rambus’s patents applied to SDRAMs and DDR SDRAMs. (CX1069 at 1) (Karp May 1999 email: “They probably think they avoid our IP if they don’t go ‘packetbased’”).

F. Rambus Prepared to Enforce its Strategic Patent Portfolio.

1701. In late May 1997, Rambus CEO Geoffrey Tate considered hiring Joel Karp to coordinate Rambus’s strategies for enforcing patent claims against non-Rambus technologies. (CX0928 at 1).

1702. Mr. Tate understood that Mr. Karp was “NOT a technologist” and thus would not be in a position “to determine who infringes [Rambus patents] and how.” (CX0928 at 1). Tate expected that Karp’s “real strength” would be in “negotiating deals with infringers.” (CX0928 at 1).

1703. In June 1997, Mr. Tate briefly reconsidered whether Rambus should hire Mr. Karp in light of the fact that DDR devices were not likely to be available until early to mid-1998. (CX0931 at 1 (Tate June 1997 email: “i’ve decided to NOT make joel an offer and NOT make him a consultant. reasons: . . . DDR is not coming 2H/97 but more like 1H/98, mid-98 . . . if we get surprised and DDR happens sooner we can always . . . try to hire joel later”)).

1704. In October 1997, Mr. Karp became Vice President of Intellectual Property at Rambus. (CX0960 at 1; CX0963 at 1; Crisp, Tr. 3410; CX2059 at 33 (Karp, Dep.)).

1705. Mr. Karp knew from the day he was hired at Rambus that there was a good chance Rambus would end up in litigation with DRAM manufacturers. (CX2102 at 429 (Karp, Dep.)).

1706. Rambus hired Mr. Karp to negotiate licensing agreements with manufacturers of non-Rambus DRAMs. (CX2114 at 105 (Karp, Dep.) (“they really hired me to do noncompatible licensing”); CX2059 at 33 (Karp, Dep.) (“I was hired specifically for the noncompatible licensing”); CX0960 at 1 (Karp’s role “is to prepare and then to negotiate to license our patents for infringing drams (and potentially other infringing ic’s”)); CX2067 at 48-50 (Davidow, Dep.); CX0963 at 1 (Tate October 1997 email announcing that Karp “joined rambus . . . as vice president responsible for assessing our patent portfolio, determining when chips infringe our patent portfolio, setting licensing strategies for infringing chips, and for negotiations with companies that build and sell infringing chips.”)).

1707. Rambus was careful not to make it known externally what Mr. Karp was hired to do. (CX0960 at 1 (Tate October 1997 email: “when joel starts we have to have our spin control ready for partners/etc as to why we are hiring him and what he will be doing. my thought is we say externally that joel is coming on board to help us with contracts and ip licensing.”); CX0963 at 1 (Tate October 1997 email to Rambus staff: “joel karp joins rambus ****NOTE****: message to outside is only that ‘joel is going to help us with contract negotiations’”)).

1708. Rambus wanted to keep Mr. Karp’s job responsibilities quiet as part of its “strategy” to “downplay the whole infringement/IP issue.” (CX0963 at 1 (Tate October 1997 email to Rambus staff: “currently we expect based on datasheets that both ddr sdram/sgram and sldram will infringe our patents. . . . ****NOTE**** - we are not making any public statement outside of rambus about joel joining. . . . Our strategy is to downplay the whole infringement/IP issue until there is actual infringement.”)).

1709. Mr. Karp contemplated suing unlicensed companies that used RDRAM. (CX0982 at 1) (Karp December 1997 email: “If unlicensed folks use our IP, we are well protected with patents and must use whatever legal remedies we deem necessary to shut them down or have them take a license from us.”).

1710. Shortly after joining Rambus, Mr. Karp began planning a campaign to collect royalties from DDR SDRAM and other non-RDRAM products. (Crisp, Tr. 3418).

1711. Rambus CEO Geoffrey Tate instructed Mr. Karp not to agree to any “non-compatible” DRAM license unless the royalty rate was greater than the rates Rambus charged for its proprietary RDRAM technology. (CX0960 at 1 (Tate October 1997 email: “i advised clearly that if a chip co wants to license all of our present and future patents for use for any infringing dram, then the only acceptable deal is the royalty on infringing drams must be greater than the royalty on rambus drams.”)).

1712. Rambus’s strategic objective in charging higher royalties for SDRAM than RDRAM was to promote the adoption of RDRAM by raising the costs of competing technologies. (CX0550 at 1 (January 1998 document setting out Rambus’s “Goals for 2002”: “Develop and enforce IP, A. Get access time register patent issued that reads on existing SDRAM . . . C. Get all infringers to license our IP with royalties > RDRAM (if it is a broad license) OR sue”); CX1744A at 150 (Karp’s October 1998 handwritten notes regarding a one-on-one meeting with Tate: “SDRAM Royalties – royalty rate dependent on . . . RDRAM -- idea - how to prevent a new competitive device”); CX2114 at 149-150 (Karp, Dep.); CCF 1977-80)).

1713. Mr. Karp thought it best that Rambus not make any public disclosure regarding its belief that DDR infringed Rambus patents. Karp was concerned that a public disclosure would cause DRAM manufacturers to band together to find ways to avoid paying royalties to Rambus. Mr. Karp suggested that the better strategy was to “approach companies individually and without any publicity.” (CX0988 at 1 (“I am very uncomfortable with any public statements regarding who or what infringes our patents. . . . Once one or two sign up to strategic licenses it will be much easier to license the others but public pronouncements only stimulate a lot of negative emotions towards Rambus.”)).

1714. In 1997, Rambus implemented the strategic patent portfolio project. (CX2067 at 103 (Davidow, Dep.)). The term “strategic patent portfolio” “referred to the 1990 patent or continuances to the 1990 patent.” (CX2109 at 198-99 (Davidow, Dep.)).

1715. In February 1998, Mr. Karp produced a draft document entitled “Strategic Patent Licensing Program” in which he identified target royalty rates for DDR SDRAM (3.0-4.0%) and SDRAM (3.5-5.0%). (CX0551 at 1).

1716. In April 1998, Mr. Karp formed an internal “Rambus Patent Council,” which was to “meet once a month with the intent of discussing [Rambus’s] overall patent strategy/directions from a strategic perspective.” (CX1017 at 1).

1717. One of Rambus’s “key results” for 1998 was securing its strategic patent

portfolio. (CX1744A at 161 (“Key result . . . IP rights secure strategy portfolio, convince industry that paying royalties to Rambus is a fact of life”); CX2114 at 152-154 (Karp, Dep.)).

G. Rambus Destroyed Documents in Anticipation of Patent Enforcement Litigation.

1718. In March 1998, there was “growing worry” within Rambus about “email back-ups as being discoverable information” in future litigation. (CX1005 at 1).

1719. In April 1998, Rambus planned to purchase several high volume shredders. (CX1744A at 92 (“Buy shredders for all floors.”); CX2114 at 134-35, 123-124 (Karp, Dep.) (“the idea was to put shredders at more convenient locations”)).

1720. Rambus executives decided to destroy emails archived on the company’s backup system after three months. (CX1744A at 94 (“3 months might be ok”); CX1744A at 104 (May 1998 management staff meeting: “Backups kept for three months); CX2114 at 136-39 (Karp, Dep.) (“the backups would be kept three months”)).

1721. Rambus did not preserve emails from the early 1990’s that were stored on macintosh backup tapes. (CX2114 at 139-140 (Karp, Dep.) (“those were the first tapes that were destroyed”)).

1722. Rambus CEO Geoffrey Tate and Mr. Karp had a one-on-one meeting at which they discussed reviewing pre-June 1996 backup tapes. (CX1744A at 136 (“Review backup tapes for pre-June 1996, Check for files”); CX2114 at 144-145 (Karp, Dep.)).

1723. On May 14, 1998, Mr. Karp sent an e-mail to all Rambus engineers and senior managers regarding “Backup Strategy/Document Retention Policy.” (CX1031 at 1). He informed them that “[e]very Rambus employee will be involved” in Rambus’s document retention policy. (*Id.*) Karp announced that he expected to have “a company meeting in early June to kick off the program.” (*Id.*) He invited questions in face-to-face discussions, but preferred that senders of any emails “keep the distribution narrow.” (*Id.*)

1724. In June 1998, Mr. Karp was finalizing Rambus’s document retention policy and preparing slides to explain the policy to Rambus employees. (CX1744A at 122 (“Doc retention teaching slide next week”); CX2114 at 140-141 (Karp, Dep.) (“we were finalizing the document retention policy . . . I was working on a set of slides that were going to be used as part of the meetings that would be held.”)).

1725. In June 1998, Mr. Karp outlined a plan to implement Rambus’s document retention policy. (CX1744A at 126 (“Exec approval of doc. ret. policy, Presentation of details to exec, Presentation to managers and key individuals with outside counsel, Presentation to staff

via division meetings, Implementation mid-August”); CX2114 at 141-142 (Karp, Dep.)).

1726. Rambus CEO Geoffrey Tate made the final decision to implement the document retention policy at Rambus. (CX2102 at 362 (Karp, Dep.))

1727. In July 1998, Karp disseminated Rambus’s two-page written document retention policy to all Rambus employees. (CX1040 at 1-2; Diepenbrock, Tr. 6230; CX2114 at 155-56 (Karp, Dep.)).

1728. Rambus provided inadequate guidance to its employees as to what documents should be retained and which documents could be purged as part of its corporate document retention program. (February 26, 2003 Order on Complaint Counsel’s Motions for Default Judgment and for Oral Argument at 9; CX1040 at 1-2 (policy itself provided little guidance to employees)).

1729. Rambus’s corporate document retention program specifically failed to direct its employees to retain documents that could be relevant to any foreseeable litigation. (February 26, 2003, Order on Complaint Counsel’s Motions for Default Judgment and for Oral Argument at 9; CX1040 at 1-2; CX1264 at 1; CX2102 at 354 (Karp, Dep.) (Mr. Karp did not recall anyone at Rambus saying documents should be retained because they might be relevant to some future litigation.)).

1730. Rambus’s corporate document retention program specifically failed to require employees to create and maintain a log of the documents purged pursuant to the program. (February 26, 2003, Order on Complaint Counsel’s Motions for Default Judgment and for Oral Argument at 9; CX1040 at 1-2; CX2102 at 371 (Karp, Dep.) (Mr. Karp did not recall Rambus keeping any inventory of the items that were destroyed)).

1731. After distributing the written policy, Karp and an attorney from Cooley Godward held a meeting with all Rambus employees to “kick off” the document retention policy. (Diepenbrock, Tr. 6230; Crisp, Tr. 3419; CX2102 at 361-62 (Karp, Dep.); CX2114 at 156 (Karp, Dep.)).

1732. While explaining the document retention policy to Rambus employees, Mr. Karp told staff to destroy emails because they could be discoverable in litigation. (Diepenbrock, Tr. 6230-32; CX1264 at 1 (“EMAIL – THROW IT AWAY • Email Is Discoverable In Litigation Or Pursuant To A Subpoena • Elimination of email is an integral part of document control • In General, Email Messages Should Be Deleted As Soon As They Are Read”)); CX2114 at 161 (Karp, Dep.) (“We know all e-mail is discoverable; there’s no question about that. So the real question becomes what are you required to save and what should you not save.”)).

1733. Rambus’s former in-house counsel Anthony Diepenbrock was told that Rambus

did not want to keep documents around because they were “[d]iscoverable in a lawsuit.” (Diepenbrock, Tr. 6234-35 (“Q. And when you say you were told Rambus didn’t want to keep these documents around because they were discoverable, when you say ‘discoverable,’ you are talking about in a subsequent litigation like we are in right here, right? . . . A. Discoverable in a lawsuit, right”)).

1734. In the weeks following the initial meeting, Karp held several training sessions regarding the document retention plan. (CX2102 at 361 (Karp, Dep.)).

1735. Mr. Karp explained Rambus’s document retention policy to all Rambus employees. (CX2102 at 367 (Karp, Dep.)).

1736. From 1998 through 2000, Rambus employees destroyed massive amounts of material as part of Rambus’s document retention policy. (CX1052 at 1; CX2114 at 165 (Karp, Dep.) (“Q. You testified previously there were a large number of documents discarded or purged or destroyed after this policy was implemented at Rambus? A. Yes.”); CCF 1737-40)).

1737. As a result of directives from Mr. Karp, Mr. Diepenbrock, Rambus’s in-house counsel, purged his documents and files in the summer on 1998. (Diepenbrock, Tr. 6235-36).

1738. In response to Joel Karp’s directives regarding the document retention policy, Richard Crisp, Rambus’s primary JEDEC representative, cleaned out his files. (Crisp, Tr. 3425; CX2082 at 841-43 (Crisp, Dep.)). Because Crisp was leaving on a business trip to Asia, he did not have a lot of time to sort through all the material in his office. (Crisp, Tr. 3427). As a result, Crisp simply dumped most of the paper in his office, including JEDEC-related material and any paper documents regarding patent prosecution work, into a burlap bag to be shredded. (Crisp, Tr. 3427-30; CX2082 at 841-43 (Crisp, Dep.) (“anything that I had on paper, I basically threw away”)).

1739. In September 1998, Rambus celebrated a corporate-wide “Shred Day.” (CX1044 at 1; CX1051 at 1 (“Thursday is Shred Day 1998 . . . Please leave your burlap bags in the hallway . . . We will have a Shred Day Celebration in the new 1st floor open area . . . If you have any questions regarding our Document Retention Policy, please see Joel [Karp]”); Crisp, Tr. 3422; CX2102 at 369-370 (Karp, Dep.) (“we had one day where we had kind of a spring cleaning . . . one of the many Valley shredding companies [came] in with their kind of industrial shredders”)).

1740. In one day alone, in the space of five hours, Rambus destroyed as much as 20,000 pounds of business records. (CX2102 at 371 (Karp, Dep.) (Rambus delivered “a lot of stuff” to the shredding company; the “stuff [was] being basically piled pretty high on carts.”); CX1052 at 1 (Karp September 1998 email: “Shred Day: Status Report . . . It took about 5 hours to completely fill the shredding truck (capacity is 20,000 lbs)”)).

1741. Mr. Karp testified that he “did a little bit of spot checking” with Rambus employees and “sat and watched over their shoulder” to insure compliance with the document retention policy. (CX2102 at 360-61 (Karp, Micron Dep.))

1742. In September 1998, Mr. Karp had a one-on-one meeting with Rambus CEO Geoffrey Tate during which Karp inquired whether Tate and other board members had cleaned out their files. (CX1744A at 141 (“Doc. Retent, Geoff files?, Board members?”); CX2114 at 146-47 (Karp, Dep.) (“Q. You were checking up on Mr. Tate? A. Yes”)).

1743. Mr. Karp deleted all his Rambus-related files from his computer when he left Rambus in summer 2000. (CX2059 at 62 (Karp, Dep.); CX2102 at 378 (Karp, Dep.)).

1744. From 1998 through 2000, Rambus’s outside counsel destroyed massive amounts of material as part of Rambus’s document retention policy. (CCFF 1745-48, 1752).

1745. Rambus instructed Lester Vincent, an attorney with its outside patent law firm Blakely, Sokoloff, Taylor & Zafman, to destroy Rambus-related files. (CX3129 at 530 (Vincent, Dep.) (“[Karp] discussed the Rambus document retention policy that he wanted me to implement.”); CX3126 at 410 (Vincent, Dep.); CX2114 at 182-83 (Karp, Dep.)).

1746. At Rambus’s request, Mr. Vincent destroyed a variety of documents from the left hand side of his files, including various “prosecution documents” such as “patent prosecution files for issued patents . . . claiming priority to the 1990 Farmwald, Horowitz application.” (CX3126 at 408 (Vincent, Dep.); CX3129 at 530-33, 536, 539-40 (Vincent, Dep.)).

1747. Mr. Vincent also destroyed various “drafts, handwritten notes, letters or faxes, and maybe drawings,” including correspondence from Rambus to Blakely, Sokoloff and vice versa, Vincent’s own handwritten notes and those of other lawyers from his firm, drafts of patent applications and amendments, draft handwritten drawings or informal drawings, electronic versions of such documents, and audio tapes of meetings with inventors. (CX3129 at 531-533 (Vincent, Dep.); CX3126 at 425-26 (Vincent, Dep.) (“drafts or handwritten notes or correspondence in the file . . . would be destroyed.”)).

1748. Some of the copies Mr. Vincent destroyed were the “only documents in existence.” (CX3129 at 539-40 (Vincent, Dep.)).

1749. Mr. Vincent carried out the document destruction at various points in time, beginning several months after the initial instructions he received from Rambus in 1997 and early 1998. (CX3126 at 418, 422 (Vincent, Dep.)).

1750. Mr. Vincent briefly suspended the document destruction after Rambus filed a lawsuit against Hitachi in 2000. (CX3129 at 534-535 (Vincent, Dep.)).

1751. Rambus President David Mooring and Mr. Karp did not recall any changes to the Rambus document retention policy once the Hitachi litigation commenced. (CX2112 at 290-92 (Mooring, Dep.); CX2114 at 163 (Karp, Dep.)).

1752. After the hiatus in document destruction during the pendency of the Hitachi litigation, Vincent's law firm recommenced destroying documents. (CX3129 at 535 (Vincent, Dep.)). This wave of document destruction continued at least until Rambus filed the Infineon suit in August 2000. (CX3126 at 424 (Vincent, Dep.)); CX1329 at 542 (Vincent, Dep.)).

1753. CX0711 is a 199-page collection of emails authored by Richard Crisp that were preserved on Rambus's main server when Crisp transferred the messages from one laptop computer to another via the server. (Crisp, Tr. 3587-91). Crisp later deleted many of his emails, but "forgot about the directory." (Crisp, Tr. 3589-3591). Still, not all of Crisp's e-mails survived. (Crisp, Tr. 3572-73 ("unfortunately, not all of those files could go over the network because of funny characters in the names"))).

1754. Rambus's principal JEDEC representative, Richard Crisp, later joked about DDR SDRAM-related documents "fall[ing] victim to the document retention policy." (CX1079 at 1 (Crisp October 1999 email: "I'm looking for a copy (paper or electronic) of one of the original DDR datasheets from the 1996/1997 timeframe. Hopefully someone here has one that hasn't fallen victim to the document retention policy :-")); Crisp, Tr. 3431).

1755. Rambus knew or should have known from its participation in JEDEC that litigation over the enforcement of its patents was reasonably foreseeable. (February 26, 2003 Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument at 9; CX3051 at 1-26 (in December 1995, Rambus's attorneys received a fax of the FTC's proposed consent agreement in Dell, a case regarding anticompetitive unilateral conduct occurring within the context of a standards setting organization); Rambus Answer at 34, ¶ 81 (Rambus attorneys discussed the Commission's proposed consent order in Dell and "in January 1996 one or more attorneys for Rambus advised Rambus that it should no longer participate in any standards bodies"))).

1756. Rambus, at the time it implemented its document retention policy, clearly contemplated that it might be bringing patent infringement suits if its efforts to persuade semiconductor manufacturers to license its JEDEC-related patents were not successful. (February 26, 2003 Order Granting Complaint Counsel's Motion for Collateral Estoppel at 5; CX0613 at 2 (Mr. Karp attended a Rambus Board meeting in March 1998 to "update[] the Directors on the Company's strategic licensing and litigation strategy"); CX2109 at 163-164 (Davidow, Dep.); CX1804 at 23 (Rambus's privilege log withholds a March 1998 memorandum entitled "Rambus Strategic Patent Litigation" and describes two additional documents from the same time period as "Confidential attorney-client communications regarding legal strategy and reflecting work in anticipation of litigation."); CX2102 at 419 (Karp, Dep.); CX1032 at 1 (in May 1998, Rambus

executive Allen Roberts commented on the “fun times if/when we enforce our IP on DDR.”); CX1778 at 16 (Rambus 1998 Annual Report: “Litigation may be necessary in the future to enforce the Company’s patents and other intellectual property rights”).

1757. Rambus’s document destruction was done in anticipation of litigation. (February 26, 2003 Order Granting Complaint Counsel’s Motion for Collateral Estoppel at 5; CCFF 1756).

1758. When Rambus instituted its document retention policy in 1998, it did so, in part, for the purpose of getting rid of documents that might be harmful in litigation. (February 26, 2003 Order Granting Complaint Counsel’s Motion for Collateral Estoppel at 5; CCFF 1718, 1732-33).

1759. Paragraphs 1759-1799 are unused.

IX. High Royalty Rates, High Manufacturing Costs and Technical Problems Led to the Decline of the Rambus RDRAM Architecture.

A. DRAM Manufacturers Designed and Prepared to Manufacture Several Memory Architectures, Including RDRAM.

1800. Throughout the 1996-1999 timeframe, most DRAM manufacturers supported three future generation architectures: Direct RDRAM, SyncLink, and DDR SDRAM. (CX3110 at 1 (“RDRAM is just one product in our diverse DRAM family”); CX2716 at 1 (“At Micron, we will promote all three future memory technologies – DDR, SLDRAM, and DRDRAM”); CCF 1575, 1802-11, 2509).

1801. The DRAM industry was developing different memory architectures for different market segments. Companies planned to use RDRAM as main memory in mid-range and high end personal computers; DDR as main memory in servers and for graphic applications; and SyncLink as the possible next generation main memory in PC’s. (CX2718 at 45; Lee, Tr. 6727-28; CX2297 at 3, 81; Tabrizi, Tr. 9149-9151, 9155-56).

1802. After Intel announced its support for Rambus in late 1996, Hyundai devoted many resources to developing RDRAM and had a “minimum of 50 engineers working on Rambus project[s].” (Tabrizi, Tr. 9136-37 (“Rambus was a fully multilevel project within [Hyundai]. We had at least two or three project and engineering team[s] working on various Rambus project[s]”)).

1803. Hyundai decided to develop the 128Mb RDRAM product with the most advanced Hyundai technology. (CX2314A at 3 (“Direct RDRAM . . . Development without delay (0.18um Technology”); Tabrizi, Tr. 9180-83 (“.18 micron technology at the time of ‘98 was our most advanced technology”)).

1804. Hyundai hoped to become a leading producer of RDRAM and assigned its best engineers to the next generation Rambus project. (RX1487 at 6; Tabrizi, Tr. 9114-15 (Hyundai “wanted to be one of the leaders in Rambus” so it assigned its “best engineers to develop the next-generation Rambus project.”)).

1805. After Hyundai and Lucky Goldstar merged in 1998, Hyundai planned to develop LG’s more advanced RDRAM product. (Tabrizi, Tr. 9112-13; RX1487 at 6). Hyundai moved the best engineers from both companies to one location to facilitate work on its RDRAM device. (RX1487 at 6 (“Tabrizi July 1999 email: put “both companies best engineers to work on 256/288M RDRAM design by using next generation process”); Tabrizi, Tr. 9114-15 (“We wanted to put our best engineers together in one place”)).

1806. Hyundai prepared to deliver RDRAM to customers based on customer needs.

(CX2303 at 7; Tabrizi, Tr. 9164-66 (“We were trying to align our road map with Dell[’s] requirement in terms of Rambus”)).

1807. Compaq planned to transition to RDRAM because of Intel’s roadmap. (Gross, Tr. 2318). Compaq also planned to introduce RDRAM throughout its product line. (Gross 2326-27).

1808. After Micron signed a license for Direct RDRAM in 1997, Micron devoted many resources to developing RDRAM. (Appleton, Tr. 6354-6357) (“We started to do all those things you would do when you’re developing a product”). Micron formed a large design team to work on RDRAM and offered the team cash incentives to meet certain milestones. (Appleton, Tr. 6355-56). Micron also purchased new testing equipment for RDRAM. (Appleton, Tr. 6357).

1809. In 1998 and 1999, Micron included RDRAM on its DRAM product road map. (CX2718 at 26; Lee, Tr. 6722-23; CX2742 at 8-11). In September 1999, Micron’s packaging for RDRAM was nearly complete. (CX2747 at 66 (“RDRAM Product Status . . . Packaging . . .16-chip RIMM layout is nearly complete for FBGA package”)).

1810. In the 1999 timeframe, Micron moved to a higher density RDRAM part based on customer feedback and a “general migration of customers to higher density systems.” (Lee, Tr. 6744-46; CX2735 at 29 (“Decided not to develop the 64Mb/72Mb • Density did not meet customer requirements”)). The higher density parts also had “manufacturing cost advantages.” (Lee, Tr. 6745-47; CX2735 at 30 (“Lower relative cost” per bit)).

1811. In April 1999, Micron completed its higher density 144Mb Rambus design and “taped out” the part, meaning Micron “sen[t] it off for fabrication.” (CX2735 at 24; CX2735 at 29; Lee 6744-45). Micron expected to release its 144Mb samples in June 1999. (CX2735 at 31).

1812. In June 1999, Micron issued a press release announcing its first shipment of RDRAM samples to Intel. (RX1464 at 1).

1813. In 1999, Micron promoted RDRAM through product presentations and advertisements. (Appleton, Tr. 6357; CX3110 at 1 (1999 Advertisement: “With its revolutionary new architecture, RDRAM can help your design take flight. And Micron can show you how . . . We produce RDRAM and back it up with a team of experts”)).

B. The DRAM Industry Was Dissatisfied with Rambus RDRAM Royalty Rates.

1814. Even though DRAM manufacturers were gearing up to produce RDRAM, the

DRAM industry remained concerned about Rambus's royalty rates. (CCFF 1802-11, 1816-22).

1815. In the mid-1990's, Rambus acknowledged that high royalty rates could "scare" customers away. (CX0711 at 35 (Crisp email: "our proposition should be attractive there if we do not scare them away with extremely high license/royalty terms"); CX0711 at 13 (Crisp March 1994 email noting Terry Walther's statement that Micron did not like "license type business"); CX0711 at 61 (March 1995 Crisp email: "Farhad [Tabrizi of Hynix] says their #1 issue with the Rambus business proposal is the royalty rate.")).

1816. In December 1996, Rambus offered to license RDRAM to Micron for a 2% royalty rate. (Appleton, Tr. 6337-38; RX0828 at 1). Micron considered Rambus's proposed RDRAM royalty rate "high" because Rambus's technology "was just a very small piece of what was required in total to produce" a DRAM. (Appleton, Tr. 6338).

1817. Micron considered Rambus's royalty rates high because it had never paid a royalty to a company specifically relating to patents covering a memory interface technology. (Appleton, Tr. 6339; Lee, Tr. 7047-48 ("the kind of royalty rate that was being requested there, the 2 percent, was larger than anything we'd ever heard of for an interface technology and certainly the largest thing we ever heard of for some sort of fee we'd have to pay to produce main memory.")).

1818. In December 1996, IBM expressed concern to Rambus about its royalty rate on RDRAM. (CX0913 at 1 (Mooring December 1996 email: "Steve, Jeff, and I met with more than a dozen IBM apps . . . They have all TI's IP concerns, but worse . . . they are seriously considering Rambus. But the IP thing is a real dilemma.")).

1819. Siemens considered Rambus's proposed royalty rates of 1-2% unacceptable. (RX0855 at 1 (meeting minutes from January 1997 SyncLink meeting: "Siemens was eloquent. No future RB [Rambus] road map. . . . 0.1% royalty ok, 1-2% ridiculous. RB not acceptable"); Tabrizi, Tr. 9050-51; Lee, Tr. 7045-46 (Siemens's representative "was describing at that meeting that for the Rambus interface technology had the royalty been on the order of .1 percent [Siemens] wouldn't have had a problem with it and he thought the 1 to 2 percent royalty rate was ridiculous")).

1820. Richard Heye, Vice President of Advanced Micro Devices,
(Heye, Tr. 3918, *in camera*).

1821. Compaq's server group stated that they would "not use Rambus because of the royalty for the chip set." (CX1030 at 2).

1822. Throughout 1997 and 1998, Samsung expressed concern about Rambus's royalty rates. (CX0983 at 1 (Tate December 1997 email); CX2109 at 160 (Davidow, Dep.) ("we were

always going back and forth with Samsung, we were always going back and forth with Intel about issues like this . . . this was the type of issue that Samsung always kept raising about royalty rates’’)).

1823. When Samsung asked Rambus to lower its royalty rates in January 1998, Rambus CEO Geoffrey Tate replied, “we’d never lower the 1% long term royalty, period.” (CX0992 at 2). When Samsung repeated its request one year later, Rambus stated that “going below 1% would be very hard.” (CX1059 at 2 (Tate December 1998 email: Samsung’s “mentality is now that they are ramping volume they should get royalty breaks below 1% (suggested 0.5%) [and] that 2% is too steep for initial production (want 1%) . . . we told them . . . that going below 1% would be very hard . . . but i said on the 2% we had flexibility’’)).

1824. In November 1998, Rambus CEO Geoffrey Tate shared with Rambus executives a strategy to increase Rambus’s long-term RDRAM royalty rates. (CX1057 at 1 (Tate November 1998 email: only 3 dram companies are at 1% long term - samsung we can move up at 512Mbit . . . nec/toshiba we could negotiate up as part of an infringing dram license negotiation. so maybe we should be thinking of ‘1.5%’ as the long term royalty rate minimum for the major dram partners. [I]f we get samsung/nec/toshiba up to 1.5% over time; LG semicon/hyundai/hitachi are already at 1.5% 1.t; so then we’d have all the biggies at the same royalty rate (and higher than 1%!’’)).

C. Intel Was Concerned about Rambus RDRAM Royalty Rates.

1825. Intel, as a manufacturer of chipsets, has an inherent interest in ensuring that interface technology that it is supporting – such as RDRAM – be as widely adopted by makers of complimentary products as possible. Intel wanted to keep the cost of RDRAM low so that DRAM vendors would be motivated to build RDRAM. (MacWilliams, Tr. 4849-50 (if the DRAM vendors “couldn’t sell the new technology at a cost pretty close to the old technology once it got in volume, we couldn’t see how the market would transition.’’)).

1826. Because the DRAM industry was concerned about Rambus’s high DRAM-related royalty rates, Intel conditioned its support of RDRAM on low royalty rates. (RX1532 at 2 (“Intel made decision NOT to negotiate a contract for the memory vendors, but did add conditions into the contract to help the industry (limit royalties’’)).

1827. Intel’s contract with Rambus capped the royalty rate Rambus could charge for RDRAM technology at 2%. (CX0938 at 2 (Tate July 1997 email: “RDRAM royalty cap of 2% (per [] our contract with Intel)’’); CX2109 at 133 (Davidow, Dep.)).

1828. Intel pressured Rambus to keep its royalty rates low throughout the 1996-1998 time frame. (CX0912 at 2 (Tate November 1996 email: “intel’s goal here is to keep rambus from driving up dram royalties’’); CX0936 at 1 (Davidow July 1997 email noting that Intel

“limited the royalties” DRAM makers “have to pay” to Rambus); CX0952 at 2 (Tate September 1997 email reporting on Intel’s “NEW REQUEST” that Rambus institute “long term reduction of royalty based on volume going to less than ½% for rdrams”); Farmwald, Tr. 8404).

1829. Despite Intel’s efforts to keep Rambus’s royalty rates low, DRAM vendors believed Rambus was continuing to insist on higher than expected royalty rates. (MacWilliams, Tr. 4840 (Intel “heard back from several DRAM vendors who were not very happy with Rambus”); MacWilliams, Tr. 4841 (Intel “heard back from DRAM vendors many times that Rambus was taking maximum advantage of their position. They were charging higher royalties for lower volumes.”); CX0936 at 1 (Tate July 1997 email noting that “memory manufacturers feel beaten up” by Rambus); RX1532 at 2 (“Intel made the decision NOT to negotiate a contract for the memory vendors . . . In retrospect, this was a mistake . . . RamBus took advantage of the memory vendors”)).

1830. In September 1997, Rambus CEO Geoffrey Tate and Rambus Vice President David Mooring met with Intel executives Gerry Parker and Pat Gelsinger. (CX0952 at 1). Intel requested that Rambus, among other things, lower its RDRAM royalties even further to help overcome DRAM maker resistance to producing RDRAM devices. (*Id.* at 2 (“they want us to have license deals that reward time to market, etc (old request) AND have long term reduction of royalty based on volume going to less than ½% for rdrams (at this point i choked/gasped”)). Intel explained that if Rambus did not lower its RDRAM royalties, this could cause DRAM makers “to find alternate solutions to avoid paying rambus a royalty” and could cause Intel “to rearchitect things to be completely different if necessary.” (*Id.* at 2).

1831. Mr. Tate and Mr. Mooring responded to Intel by saying that the industry could successfully pursue an alternative to RDRAM only if it could set an industry standard with multiple compatible sources and avoid or prove invalid Rambus’s patent. (CX0952 at 2-3). They further stated that all industry proposals they had seen would infringe Rambus patent or patent applications. (*Id.* at 3)

1832. In October 1997, Rambus CEO Geoffrey Tate had a meeting with Pat Gelsinger, the senior Intel executive responsible for the Rambus relationship. The purpose of the meeting was to follow up on Mr. Gelsinger’s earlier request that Rambus “lower [] rdram royalties to <0.5%,” and his suggestion that if Rambus failed to do so DRAM makers would “insist on developing alternatives” to RDRAM. (CX0961 at 1).

1833. The October 1997 Rambus-Intel meeting focused in part on the extent to which DDR had “GAINED ground” with PC manufacturers and thus was a continuing “threat” to RDRAM. (CX0961 at 2-3). Intel believed that at least one DRAM maker was promoting DDR because of Rambus’s royalty rates. (*Id.* at 5 (Rambus CEO Geoffrey Tate’s report of the October 1997 Rambus-Intel meeting: “they see ddr being aggressively pushed by samsung BECAUSE of rambus royalties.”)).

1834. During the spring of 1998, Intel was still complaining to Rambus about size of Rambus's RDRAM royalty rates. (Farmwald, Tr. 8404-5).

1835. Intel expected Rambus to do its part to make RDRAM a success by lowering its RDRAM royalties. (CX1007 at 1-2) (Tate March 1998 email: "What Intel wants Rambus to do: Share in risk – offer royalty reduction for DRAM suppliers who are willing to risk starting RDRAM as directed by Intel/Rambus").

1836. Intel believed that one long term problem with RDRAM was Rambus's royalty-based business model. (CX1016 at 3-4) ("big issue is this one. the dram industry doesn't like the rambus business model. . . . [Intel] perceives that rambus business model has been what makes the r dram ramp so hard to manage – royalties – control/rambus using intel as a club").

1837. Rambus had the impression that Intel considered Rambus greedy. (CX1041 at 1-2) (Karp July 1998 email: "Senior executives at Intel don't like us. They think we're greedy and they're worried we could screw up their whole program. . . . GS Choi is very paranoid about Rambus. He's worried we'll bump the royalties way up (5%) once Direct [RDRAM] becomes the standard.").

D. As DRAM Manufacturers Worked to Develop RDRAM, They Encountered Significant Cost Problems.

1838. Rambus co-founder Mark Horowitz acknowledged that one obstacle to marketing RDRAM was the belief that "[i]t will never be cheap enough to be competitive." (CX1323 at 15 (presentation by Rambus co-founder Mark Horowitz)).

1839. In 1998, DRAM manufacturers were encountering significant cost issues associated with RDRAM production. (CX2521 at 1-2 (September 1998 letter from Samsung executive Yoon-woo Lee to Intel describing difficulties with its RDRAM program: "I'm concerned about high cost structure of RDRAM over PC-100 even without considering the royalty to Rambus."); CCFF 1840-47, 1853)).

1840. In the 1998 timeframe, DRAM manufactures estimated that RDRAM would be more costly to produce than other DRAMs. (Gross, Tr. 2364-65 ("the cost to manufacture RDRAM were higher than the costs to manufacture the alternative technologies"); CX2108 at 228 (Oh, Dep.) (the cost of producing Direct RDRAM was "much higher" than other types of DRAM); CX2718 at 44; Lee, Tr. 6733 (Micron "projected a 30 percent cost increase for direct RDRAM relative to an SDRAM."); CX2728 at 2 ("RDRAM cost is about 50% higher than SDRAM in 1999, about 30% in 2000); CX2303 at 16; Tabrizi, Tr. 9172-9174 (Based on die, packaging, and testing costs alone, Hyundai estimated that at the initial stage Rambus would cost 18% more to produce than SDRAM.); Tabrizi, Tr. 9172-9174 (In the high volume stage, Hyundai estimated that RDRAM would cost about 13% more to produce than SDRAM)).

1841. Several factors contributed to the high cost of producing RDRAM. (CX2716 at 1 (Lee January 1998 email: “There are several issues that effect the cost curve for DRDRAMs, which include the packaging, handlers, burn-in equipment, die size, licensing, and test. Some of these areas will require the purchase of new manufacturing equipment, and some areas have an inherently higher manufacturing cost.”); CX2083 at 132-133).

1842. Most importantly, RDRAM cost more to produce than SDRAM because Rambus’s royalty fees drove up the cost. (CX2303 at 16 (“Other Cost Adder - Direct Rambus Royalty); Tabrizi, Tr. 9174 (“Direct Rambus had other costs. We had to pay royalt[ies], so that was [an] additional cost.”)).

1843. RDRAM cost more to produce than SDRAM because RDRAM involved a larger die size. (Lee, Tr. 6733-5; Tabrizi, Tr. 9167-68; CX2303 at 15 (“13.5% die Penalty over SDRAM”)).

1844. RDRAM cost more to produce than SDRAM because companies had to change their packaging and assembly systems to accommodate Rambus’s different type of package. (Lee, Tr. 6733, 6735; Tabrizi, Tr. 9174-75; Peisl, Tr. 4416-17; CX2303 at 16; Gross, Tr. 2363-64 (“the RDRAM device was what was known as a ball grid array, BGA package, and that was a new package relative to high volume production in the DRAM industry.”)).

1845. RDRAM cost more to produce than SDRAM because companies had to invest in expensive new high performance testing equipment. (Lee, Tr. 6733, 6736; Peisl, Tr. 4416-17; Tabrizi, Tr. 9174-75 (Hyundai “had to invest [in] a new tester because Rambus require[d] a high performance tester, and each . . . tester is in multimillion-dollar range”); Gross, Tr. 2362-63 (“The issue with testing was that because [the] RDRAM product was very fast technology, it would have required new and expensive testing equipment”)). Manufacturers had to wait nine months to one year to obtain the new testing equipment. (Gross, Tr. 2363 (“describing “long lead time” to purchase testing equipment)).

1846. RDRAM cost more to produce than SDRAM because the RIMMs, memory modules that go with the Rambus memory, were more expensive. (Heye, Tr. 3700-01 (“rim has heat syncs, that’s more expensive . . . [also] the layout of the RIMMs, how you physically hook up to Rambus on those RIMMs was extremely expensive”)).

1847. In early 1998, the “cost of Rambus was starting to concern memory vendors.” (Heye, Tr. 3696-97 (“some of the initial cost projections of Rambus versus DDR were not coming in line to what had initially been expected . . . it was much more expensive than people had thought”)). Many memory vendors told Mr. Heye that RDRAM had a higher cost structure per part basis than DDR. (Heye, Tr. 3697).

1848. DRAM suppliers were reluctant to produce RDRAM because there were “issues

with the availability of test equipment and some packaging” and supply materials. (RX1287 at 5 (“Suppliers reluctant on move to RDRAM . . . issues with test, packaging”); Gross, Tr. 2362).

1849. Dell understood that the RDRAM cost premium inhibited the development and production of RDRAM. (CX2180 at 1, 4 (Dell Presentation regarding RDRAM Outlook: “Cost premiums continue to be the main ramp inhibitor . . . Rambus premium over SDRAM are inhibiting ramp . . . No evidence of any significant efforts to reduce Rambus premiums, Dell Customers don’t believe cost will ever drop”)).

1850. Compaq’s customers were price conscious and considered computers with RDRAM too expensive, even though RDRAM had performance advantages. (Gross, Tr. 2293-94 (“it didn’t seem that the customers were willing to pay extra for the benefits of RDRAM”)).

1851. Intel was very concerned about the cost of RDRAM. (CX0974 at 1 (Tate December 1997 email discussing Rambus-Intel meeting: “COST – biggest issue”; “rdram price premiums of 20-30%!!”; “die size premium”; “royalty reduction”); CX2109 at 218-19 (Davidow, Dep.) (Intel representatives attended Rambus Board meetings to review what Rambus was doing to reduce costs)).

1852. Intel believed that cost-related issues associated with RDRAM’s die size could prevent the industry from accepting RDRAM. (CX0961 at 2) (Tate May 1998 email: “die size is the new BIG concern at pat [Gelsinger’s] level – he’s concern that our die size premium could price us out of much of the market”).

1853. In 1998, Intel was doubtful that the cost of manufacturing RDRAM would ever be comparable to the cost of making SDRAM. (CX2541 at 1; CX2887 at 1 (“Rambus’s original commitment of achieving $\leq 5\%$ parity with SDRAM on cost has been grossly missed. Without dramatic efforts by Rambus, this goal will not be met for several years, if ever.”)).

1854. Rambus was aware of the cost issues associated with producing RDRAM. (CX1034 at 2 (“lots of discussion about cost/price of direct rambus”); CX0622 at 1-2 (July 1999 Rambus Board Meeting Minutes: “reviewed test issues and cost, packaging costs and an evaluation of RDRAM die area overhead”)).

1855. When Sun Microsystem expressed concern to Rambus about cost issues associated with RDRAM, Rambus responded, “once the technology gets to volume, the costs will come down.” (Bechtelsheim, Tr. 5823). Sun co-founder Andreas Bechtelsheim believed that Rambus did not “have any understanding of issues such as testing cost” and other problems that “later became significant burdens for their technology.” (*Id.*)

1856. In April 1999, the cost issues associated with producing RDRAM remained a problem. (Lee, Tr. 6747-6750; CX2735 at 33 (“Rambus and RIMM Issues Remain, RDRAM

die size adder - Will the customer pay for it?, Extra high-speed testing vs. SDRAM, CSP packaging learning curve; Royalty cost”); CX2334 at 27 (“Hyundai Rambus DRAM Strategy, Cons . . . Cost (royalty/test/yield)); Tabrizi, Tr. 9212-13 (one of the disadvantages of the Rambus product was high costs “due to royalty, test, and yield”).

1857. In September 1999, Micron projected that in 2000, RDRAM would cost 40-50% more to produce than SDRAM. (CX2747 at 68; Lee, Tr. 6763-64). Although Micron estimated that the relative cost of manufacturing RDRAM compared to SDRAM would decrease over time, Micron projected that the added cost of producing RDRAM would remain at 30% in second half of 2000. (CX2747 at 68; Lee, Tr. 6763-65).

1858. Micron also projected that RDRAM would always be more costly to produce than SDRAM because of RDRAM’s increased die size. (Lee, Tr. 6765-67; CX2747 at 69 (“Die size adder appears to be constant at ~25-30% for standard RDRAM”).

1859. Some people in the DRAM industry were concerned that Rambus could fail for technical reasons or because of cost issues. (Lee, Tr. 6931).

1860. One and a half years later, at the Intel Developer Forum in spring 2001, companies were still discussing ways to reduce the cost of RDRAM. (Hampel, Tr. 8712-19; RX1762 at 80 (Toshiba presentation on its RDRAM “Cost Reduction Plan”).

1861. As late as 2001, despite efforts to reduce the costs associated with producing RDRAM, Elpida expected the cost differential between RDRAM and SDRAM to continue into 2003. (RX1762 at 39).

E. The DRAM Industry Tried to Resolve the Problems with RDRAM Despite Only Mixed Support from Rambus.

1862. Despite several “cons” with RDRAM, including cost issues associated with testing and royalty payments, DRAM manufacturers were committed to fixing problems with RDRAM. (CX2334 at 27 (Hyundai made solving remaining problems with RDRAM a “High priority”); CX2108 at 227 (Oh, Dep.) (Hyundai assigned resources to solve design and technical related problems with RDRAM); Lee, Tr. 6747-51; CX2735 at 37-40 (Micron attempted to use better packaging); CX1368 at 1-2; Hampel, Tr. 8708-09 (Micron was working with Rambus to reduce the cost of RDRAM)).

1863. In mid-1997, Intel sought to influence Rambus to establish better relations with DRAM makers. (CX0944 at 1 (Tate August 1997 email noting that he had met with Samsung and that “the main objective of this meeting was to start to address intel’s ‘dram vendor happiness’ issue”); CX0954 at 1-2, *in camera*).

1864. Intel and Rambus executives discussed ways to fix Rambus's relationship with the DRAM manufacturers. (MacWilliams, Tr. 4871-72). Rambus "seemed to be sensitive to the fact that they needed to fix" problems with DRAM manufacturers. (MacWilliams, Tr. 4873). However, Intel "didn't see much action in many cases." (*Id.*) What actions Intel did see "didn't do much to fix the issues." (*Id.*)

1865. In 1998, Intel continued its work to make RDRAM a market success by investing in DRAM companies that developed and supplied RDRAM. (CX1006 at 1 (Rambus executive David Mooring reported that Intel "would invest about \$1 billion in . . . several of the top DRAM companies with the funding tied to RDRAM execution."); CX2522 at 2-3 (October 1998 Intel press release: "We will invest \$500 million in Micron to support the development and supply of next generation memory products, specifically Direct RDRAM . . . Key Messages: The investment in Micron is part of Intel's strategy . . . to help drive PC industry growth by accelerating the adoption of Direct RDRAM"); Appleton, Tr. 6375-6378)).

1866. Intel did not succeed in mending the relationship between Rambus and the DRAM manufacturers. (MacWilliams, Tr. 4874 (in "the end, the DRAM vendors were still telling us that there was a problem. [Rambus] somehow [wasn't] able to take the step to get the DRAM vendors to perceive them as a key part of the value added to the industry."))).

F. Rambus and Intel Averted a Major Blow-up in Spring 1998.

1867. Despite Intel's efforts to make RDRAM a market success, by 1998 the Rambus-Intel relationship was on a rocky road. (CCFF 1865, 1868-70, 1873-75).

1868. In March 1998, Intel sought to obtain "rights to Rambus IP for use in non-competing areas," and also in "competing areas after Intel introduces the broad range of products." (CX1007 at 2). Intel wanted "to eliminate any chance of IP-related litigation from Rambus." (*Id.*)

1869. On April 14, 1998, Rambus CEO Geoffrey Tate and Chairman William Davidow met with Pat Gelsinger of Intel to discuss Intel's concerns about Rambus. (Farmwald, Tr. 8402; CX1016 at 1; CX2109 at 174-75 (Davidow, Dep.); CX2083 at 127-28, 132 (Davidow, Dep.) (Intel's concern was "whether they could get RDRAMs in a volume and at a price that would enable them to sell their products competitively. And so, I think they were driving home that point to us."))). The basic message of the meeting was that in the intermediate term Intel would continue to support RDRAM, but Intel might support a competing architecture for the next generation. (CX1016 at 1-4 ("Intel says they are basically going to compete with us on next generation."))).

1870. The April 14, 1998 Rambus-Intel meeting caused Rambus executives to consider asserting Rambus's patents against DRAM manufacturers. As Rambus CEO Geoffrey Tate

wondered, “when will intel tell the dram companies that they are investigating next generation interface without rambus?” (CX1016 at 6; CX2109 at 176-78 (Davidow, Dep.)). Mr. Tate was concerned that a statement from Intel would cause DRAM manufacturers to switch support away from RDRAM for the next generation, which in turn could force Rambus to assert its intellectual property rights against DRAM manufacturers earlier than it wanted to. (*Id.* at 6 (“will the dram companies then not want to work with us (on next generation)? this could force us to play our IP card with the dram companies earlier.”)).

1871. Rambus’s strategy of “play[ing] the IP card” entailed threatening to sue companies that worked on non-Rambus DRAM devices for the next generation. (Farmwald, Tr. 8405-06 (Q. “do you have an understanding of what Mr. Tate meant here when he refers to the possibility of Rambus having to play its IP card with DRAM companies earlier? . . . [A.] this refers to our telling the DRAM companies that if you work on a new generation with Intel, we will sue you”); CX2109 at 176-77 (Davidow, Dep.) (“Q. What do you understand Mr. Tate to be referring to here when he says, ‘This could force us to play our IP card with the DRAM companies earlier’? . . . [A.] I would assume that this statement means is that we would inform the DRAM manufacturers that we had intellectual property that read on these technologies.”)).

1872. After the April 14, 1998 Rambus-Intel meeting, Tate called for a “**TENTATIVE BOARD MEETING**” and immediately began strategizing about how to address Intel’s announcement that it would compete with Rambus. (CX1016 at 1 (Tate April 14, 1998 email: “we’ll be doing brainstorming/strategy prep meetings at rambus over the next 2 weeks”); CX2109 at 178-79 (Davidow, Dep.)).

1873. Rambus executives were “angry” about some of the discussions at the April 14, 1998 Rambus-Intel meeting. (Farmwald, Tr. 8406-7 (“I remember being pretty angry about this”)).

1874. On April 15, 1998, Rambus co-founder Michael Farmwald responded to Mr. Tate’s concerns about Intel’s commitment to RDRAM by suggesting that Rambus “shouldn’t work with [Intel] and in fact should enforce [Rambus’s] patents against the next – a new standard.” (Farmwald, Tr. 8406-7; CX1021 at 1 (Farmwald April 1998 email: “[i]f it comes to all-out war” with Intel, Rambus might be “in a position to go after them for royalties,” or could produce documents that would make Intel “look extremely bad both to the press, a court, and to the FTC.”)).

1875. On April 16, 1998, Rambus Chairman William Davidow responded to Mr. Farmwald’s email by urging a more measured approach. (Farmwald, Tr. 8407; CX2109 at 179-183 (Davidow, Dep.); CX1022 at 1 (Davidow April 1998 email: “I am concerned that Mike [Farmwald] may be right although I would prefer a more measured approach.”)). Mr. Davidow suggested that Rambus “try to negotiate something” with Intel. (CX1022 at 2). Mr. Davidow believed that negotiations would gain time, during which Rambus could postpone asserting its

intellectual property rights against DRAM manufacturers. (*Id.* (“The advantage of trying to negotiate something with them is that it will take months. In the process we gain time. We will not have to play the intellectual property card with Micron and SDRAMs during this time.”)). He noted that if negotiations with Intel did not work, Rambus could still assert its intellectual property rights. (*Id.* (“If things blow up with Intel, then we can begin to pursue the intellectual property issue with these guys. That will get Intel really mad but they will already be really mad.”); CX2109 at 183 (Davidow, Dep.)).

1876. Richard Crisp believed that if Rambus’s failed to meet Intel’s performance standard, then Rambus would lose its “one and only chance for world dominance.” (CX0656 at 1).

G. Technical Problems and Product Delays Caused RDRAM to “Lose Momentum and Collapse.”

1877. Technical difficulties and the delay of Intel’s supporting chipset eventually caused RDRAM to “lose momentum and collapse.” (Tabrizi, Tr. 9221 (Hyundai executive Farhad Tabrizi: “the failure of Rambus was exclusively the Rambus difficulty in design and Intel failure to deliver Camino in time. . . . All the technical difficulties they had and the not readiness of the market and Intel chipset caused Rambus to lose momentum and collapse.”); CCFF 1878-94)).

1878. The Camino Chipset, also called the Intel 820 Chipset, “was the first chipset that Intel was developing to interface between their processor and direct Rambus.” (MacWilliams, Tr. 4853; Tabrizi, Tr. 9166, 9185). The Camino Chipset was intended to interface exclusively with RDRAM. (Tabrizi, Tr. 9185-86).

1879. From 1998 though 2000, “Intel continuously had problem[s] with the Camino Chipset.” (Tabrizi, Tr. 9185 (The Camino Chipset “never really materialized in terms of the technology.”)).

1880. In the second half of 1998, Intel encountered electrical issues with RDRAM. (RX1532 at 2 (Intel timeline: “2H’98 . . . Electrical side created several issues which were found late in the process”); MacWilliams, Tr. 4852-53 (“we expected these things to have been sorted out way back in the time where we had test chips or even before we had out direct RDRAM”).

1881. Technical problems with RDRAM forced Intel to delay the Camino Chipset launch several times. (MacWilliams, Tr. 4852-53; Tabrizi, Tr. 9185 (Intel “canceled their schedule of launch many times. At one time they introduced and then they had to pull back and recall all the boards.”)).

1882. In February 1999, Intel had to postpone its June 1999 target launch date until October 1999. (MacWilliams, Tr. 4852-53; CX2338 at 57 (“Feb. ‘99 . . . Intel 820 chipset

launch delayed”).

1883. In March 1999, technical problems caused Intel to internally reevaluate its exclusive support of RDRAM and begin investigating alternative DRAMs. (CX2527 at 2 (March 1999 email: “Summary: Most aspects of the Rambus transition have been more difficult than we anticipated. To that end, we believe that a strategy that puts our chipset and value processor line dependent, solely, on Rambus is no longer viable. Furthermore, the SDRAM 133 technology appears to be a relatively low risk approach for the DRAM manufacturers, and at least one chipset company (VIA) is already sampling a part that utilizes this higher speed technology.”)).

1884. In April 1999, Intel’s microprocessor rival, Advanced Micro Devices, suspended development work on its RDRAM product due to “continuing bad news about RDRAM.” (CX2158 at 2 (“(i820 delayed launch, low RDRAM yields”); Heye, Tr. 3799; 3704-05 (in late summer of fall of 1998 AMD shifted its focus to DDR because Mr. Heye believed “Rambus was going to fail as a commodity part, and that ultimately even Intel would have to go DDR”)).

1885. In May 1999, Intel’s customers were skeptical that the cost and availability issues with RDRAM could be resolved. (CX2529 at 1 (Intel May 1999 email: “OEMs skeptical that RDRAM issues will be resolved, some are waiting to see progress”); MacWilliams, Tr. 4884)).

1886. In May 1999, Intel considered adding DDR to Intel’s server memory roadmap because it was concerned that RDRAM would not “achieve the cost points in time to be competitive for the server products.” (MacWilliams, Tr. 4883-84; CX2529 at 1 (Intel May 1999 email: “Is server memory strategy POR competitive, Do we need to add DDR on Intel server memory roadmap”)).

1887. Just before the Camino chipset launch in October 1999, Intel encountered another technical problem that caused an additional one month delay. (MacWilliams, Tr. 4852-53; CX2338 at 57; CX2338 at 79 (“Sep. ‘99: 820 chipset delayed again”)).

1888.
(CX2501 at 1, *in camera* (
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1889. (CX2501 at 1, *in camera* (
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1890.

(CX0617 at 2, *in camera*).

1891. In 1999, DRAM manufacturers were hesitant to ramp up production of RDRAM because Intel was continuously modifying the Rambus system, which increased the costs of production. (Tabrizi, Tr. 9188-9190; RX1425 at 2 (“some DRAM suppliers . . . said privately that they are reluctant to commit additional funds to the [RDRAM] ramp because of design changes that are still being made to the chip.”)). Every time Intel changed the specifications for the Rambus system, DRAM manufacturers had to change the complete mask set at a cost of approximately one million dollars. (Tabrizi, Tr. 9190).

1892. In 1999, customer demand for RDRAM was dwindling due to product delays. (Tabrizi, Tr. 9188 (“the demand for RDRAM was continuously being reduced due to delay and delay”); Appleton, Tr. 6371-72 (“There were quite a few delays in the development of [RDRAM]”); CX2338 at 79 (“820 chipset delayed again”); RX1425 at 1 (Chou April 1999 email, quoting NEC Senior Vice President Shigeki Matsue: “Now that Intel has delayed the mass-market introduction of Direct Rambus, customer demand this year will be much lower than we expected.”)).

1893. In May 2000, Intel recalled the Camino motherboards due to a defect. (CX2338 at 79).

1894. In June 2000, Intel had major problems with Timna, another Intel chipset that interfaced with RDRAM, that delayed the Timna product launch. (CX2338 at 79; Tabrizi 9205-06).

H. After Intel Stopped Exclusively Supporting Rambus, RDRAM’s Projected Market Share Plummeted.

1895. In June 1999, Intel publically ceased its exclusive support of RDRAM and announced that the Pentium III chipset would support SDRAM. (Tabrizi, Tr. 9201-03; CX2338 at 57 (“Intel says PC133 SDR w/P-III is possible”); CX1077 at 1 (E. Kinsella, Intel to Back Alternative to Rambus Chips, street.com: “Ending months of speculation, Intel . . . embraced a low-cost alternative to Rambus-based . . . memory chips”)). This was the first time Intel indicated that SDRAM could compete with RDRAM as the interface with Pentium III. (Tabrizi, Tr. 9201-03; CX2338 at 57).

1896. In August 1999, Intel confirmed that it would provide support for SDRAM in the Pentium III chipset. (Tabrizi, Tr. 9201-03; CX2338 at 57 (“Intel confirms PC133 will be offered as alternative to D-RDRAM in P-III”)).

1897. After Intel announced its support of SDRAM, Rambus’s percentage of market penetration dropped because customers could choose between SDRAM and Rambus. (CX2338

at 57 (Hyundai document charting “Rambus’s rocky road”); Tabrizi, Tr. 9203 (“at that time Intel confirmed that they’re going to use PC133 . . . in P-III as an alternative to Rambus. As a result, the percentage of Rambus dropped again.”); Tabrizi, Tr. 9208 (“at the beginning when Intel introduced they’re going to use Rambus, the expectation was Rambus will be almost 80 percent of the market. With all the problems that Intel had and when Intel optioned the alternative, the Rambus penetration came down to maybe around 10 percent or lower than that.”)).

1898. During 1999 and 2000, Intel revised downward its estimates for the total available market (“TAM”) for RDRAM multiple times. (CX2338 at 79 (chart depicting Intel’s declining Rambus forecast); Tabrizi, Tr. 9193-97 (Hyundai executive Farhad Tabrizi: “from 1Q99 to 4Q2000, every time Intel came to us, they had to reduce their forecast”)).

1899. Intel reduced its forecast for RDRAM due to the “many challenges with Rambus.” (CX2338 at 79; Tabrizi, Tr. 9185, 9198 (Hyundai executive Farhad Tabrizi: “at the earliest stages when Rambus signed an Intel development agreement the potential was very high. And then as time goes on and as Intel saw many challenges with Rambus, many technical difficulties with the chipset, then they decided to reduce the potential.”)).

1900. In the first quarter of 1999, Intel met with Hyundai and projected that the total available market for RDRAM in the year 2000 would be 600 million pieces. (CX2338 at 79; Tabrizi, Tr. 9194-95).

1901. Intel met with Hyundai again in September 1999 and dropped its year 2000 RDRAM projection to 500 million pieces. (CX2338 at 79; Tabrizi, Tr. 9194-96).

1902. Intel and Hyundai had another meeting in the fourth quarter of 1999 and Intel dropped its year 2000 RDRAM projection to 300 million pieces. (CX2338 at 79; Tabrizi, Tr. 9194-96).

1903. During a Hyundai-Rambus meeting in first quarter 2000, Intel’s total available market estimate for RDRAM dropped to 250 million pieces. (CX2338 at 79; Tabrizi, Tr. 9194-96).

1904. Intel also reduced its estimates for the total available market for RDRAM the second and third quarters of 2000. (CX2338 at 79).

1905. Over the course of 1999 and early 2000, Intel’s projections for total RDRAM available market plummeted from 600 million pieces to 250 million pieces. (Tabrizi, Tr. 9194-96; CX2338 at 79, (600 million forecast in first quarter 1999); CX2338 at 79 (500 million forecast in fall 1999); CX2338 at 79, (300 million forecast in fourth quarter 1999); CX2338 at 79 (250 million forecast in first quarter 2000)).

1906. Micron never introduced RDRAM into the market for commercial sale because customer demand for RDRAM did not materialize. (Appleton, Tr. 6371-6374). In the early stages of development, Micron's customers, particularly Dell computer, forecast a large consumption of RDRAM. (Appleton, Tr. 6372-74). As Micron encountered challenges in the technology and delays, its customers "started to change their forecasts for consumption of RDRAM, and ultimately, it was at such a low level that it just wasn't worth it to try to take that to commercialization." (Appleton, Tr. 6372).

1907. Micron did not take RDRAM into volume production because "it didn't get adopted by the market in a large percentage." (Appleton, Tr. 6319)

1908. Samsung, the world's largest DRAM producer, entered commercialization and full production of RDRAM. (Appleton, Tr. 6373).

1909. Intel was not involved in the development of the initial SDRAM specifications. (CX2560 at 1 (MacWilliams July 2000 email: "PC133 specs were driven without us"); MacWilliams, Tr. 4911-13 ("other people in the industry [] proposed the spec changes from PC100 to make PC133 . . . and we weren't part of the loop initially.")).

1910. As projections for RDRAM declined in the 1999-2000 time frame, the anticipated market share shifted to SDRAM and DDR SDRAM. (Tabrizi, Tr. 9214-15).

I. Intel's Decision to Cease its Exclusive Support of RDRAMs and to Plan to Develop a Controller to Support SDRAMs and DDR SDRAMs Caused Rambus to Play the "IP Card."

1911. Between late 1996, when Intel decided to support RDRAM as its exclusive design for next generation main memory for personal computers, and October 1999, Rambus and Intel had a number of "blowup[s]." (Farmwald, Tr. 8419 ("This sort of blowup seemed to happen every one to two years with Intel. We had a number of these episodes."); Farmwald, Tr. 8423 (blowups "happened a lot"))).

1912. By September 1999, Intel engineers were very frustrated with Rambus. (CX2535 at 1 (September 1999 MacWilliams email: "we want to do a change to make cost better or enhance performance, if RDRAM is already established Rambus will likely use this as an excuse to generate more \$\$ for themselves."); CX2537 at 1 (September 1999 Ahmad email: "Samsung has done more work in debugging and ramping this technology than Rambus"); CX2536 at 1 (September 1999 Ahmad email: "other concern is that Rambus will use this as an opportunity to potentially gouge more \$\$"))).

1913.
(CX2503 at 2, *in camera* ();

MacWilliams, Tr. 5073-74, *in camera* (

)).

1914. By mid-October 1999, Intel's road map included SDRAM and DDR SDRAM solutions. (CX2540 at 1 (October 1999 MacWilliams email: "making RDRAM work does not solve the business issues Rambus is causing in the industry. Result is that we will not convert our roadmap 100% to RDRAM. In DT we continue to have SDRAM. In server we will try DDR. If the situation continues we will keep alternatives alive indefinitely.")).

1915. In late October 1999, Intel told Rambus that it wanted to have a comprehensive review of their business relationship. (CX2887 at 1 (October 26, 1999 letter from Gelsinger to Tate: "Events over the past several months, including changes within the global memory industry and changes in customer demand for memory products, lead us to believe that it is important for Intel and Rambus to conduct a very serious and comprehensive review of our current relationship"))).

1916. On October 26, 1999, Pat Gelsinger of Intel sent a letter to Messrs. Tate and Davidow highlighting many of Intel's concerns with Rambus. (CX2887 at 1-3; CX2109 at 201-202, 204 (Davidow, Dep.) ("Intel had lots of complaints about how things were going")). Intel believed that industry acceptance of RDRAM technology was "poor, at best" and blamed Rambus for failing to support Intel's efforts to promote RDRAM. (CX2887 at 1-2) ("Our customers are rapidly losing confidence in us and in the technology, largely due to the lack of total, prioritized support from Rambus."). Intel was also frustrated because Rambus had "grossly missed" its commitments in terms of projected cost reductions. (CX2887 at 1) (Rambus's original commitment of achieving $\leq 5\%$ parity with SDRAM on cost has been grossly missed.).

1917. Intel announced in its October 26, 1999 letter to Rambus that its chipset roadmap now included alternatives to RDRAM. (CX2541 at 2; CX2887 at 2-3 ("Intel has been forced to re-architect its chipset roadmap to accommodate additional SDRAM products as a direct result of Rambus's failure to adequately deal with the issues outline above. . . . we have no choice but to continue re-assessing our chipset road map"))).

1918.

(CX1080 at 1).

(CX1080 at 2).

1919. In October 1999, after reviewing the situation with Intel, Rambus decided to be "proactive" with DRAM manufacturers regarding its SDRAM and DDR-SDRAM related intellectual property. (CX1379 at 4 ("Since 1996 we assumed Intel would drive a rapid

transition from SDRAM to Rambus, Before we chose ‘not to rock the boat’ if all would be Rambus in 2-3 years, [Now] Intel has shifted to ‘let the market decide,’ is enabling DDR, and may be working on DRAM 2003, We must be proactive on our IP with DRAM companies”)

1920. In October 1999, Rambus’s executives and Board of Directors discussed which company to approach first about enforcing Rambus’s SDRAM and DDR SDRAM related patents. (Farmwald, Tr. 8416-17; Farmwald, Tr. 8239-40; CX0623 at 4 (October 1999 Board Meeting minutes: “Mr. Karp reviewed various strategic IP issues including target selection and a negotiation timeline.”); CX2109 at 199-200 (Davidow, Dep.) (“Q. What do you understand these minutes to be referring to when they use the term ‘target selection’? . . . [A.] those referred to who we were going to sit down and press extremely hard on in negotiation and what sequence we were going to talk with them and who we would litigate with and in what order if we were forced to litigate.”)).

1921. In November 1999, Rambus was strengthening its patent portfolio and assembling a patent prosecution team. (CX1085 at 1 (“congrats to Neil Steinberg for successful prosecution of another addition to our Strategic Patent Portfolio”); CX1083 at 1 (introducing “Lexington” program); CX1353 at 7 (“Portfolio 1: SDRAM/DDR/Controllers all infringe, Lexington initiated”)).

1922. In November 1999, Richard Crisp, Rambus’s primary JEDEC representative joked about enforcing Rambus’s DDR-related patents for “Double DRAM Royalties.” (CX1084 at 1 (Crisp November 1999 email: “ddr meaning, here is what it currently means: Desperate to Destroy Rambus, it will prove to mean: Didn’t Destroy Rambus, and in a year or two: Double DRAM Royalties (for Rambus)”)).

1923. In December 1999, Intel and Rambus conducted another operations review. (CX2546 at 1). Intel was “very disappointed” with Rambus’s presentation, which Intel believed contained “significant misrepresentations and self-serving commentary.” (*Id.*) Intel was most upset by Rambus’s failure to mention the “two most fundamental reasons why the ramp of RDRAM technology” proceeded slower than expected: technical problems and cost issues. (CX2546 at 2)).

1924.

(CX1418 at 112, *in camera*; CX1379 at 4; CX1355 at 127 (“Rambus has substantial IP and has an obligation to shareholders to get a return on the investment”)).

1925. Paragraphs 1925 - 1949 are unused.

X. Rambus Has Acted to Enforce U.S. and Foreign Patents with Respect to Technologies Incorporated in the JEDEC SDRAM and DDR SDRAM Standards.

A. Beginning in 1999, Rambus Asserted that its U.S. and Foreign Patents Covered Use of Programmable CAS Latency and Burst Length, On-Chip DLL and Dual Edge Clocking in JEDEC-Compliant SDRAMs and DDR SDRAMs.

1950. In late 1999, Rambus began informing DRAM manufacturing companies that their SDRAM and DDR SDRAM products might infringe Rambus patents. (Rambus Answer at 38-39, ¶ 92 (“Rambus admits that, in or about November 1999, it began contacting certain memory manufacturers to notify them that, based on analyses of the datasheets of products made by those companies, Rambus believed those products infringed certain of Rambus patents”); CCF 1953-58)).

1951. Rambus believes its patents cover SDRAM and DDR SDRAM. (CX1353 at 7 (“Intellectual Property . . . Strategic Patent Portfolio 1: SDRAM/DDR/Controllers all infringe”); CX1382 at 33 (“Non-Compatible License Terms, All agreements cover SDRAM, DDR and logic ICs which control these memories”); CX1364 at 1-2, *in camera* (

).

1952. As of November 2000, Rambus President Mooring testified that Rambus believed every SDRAM device it examined violated Rambus patents. (CX2055 at 265 (Mooring, Dep.)). In a later deposition in February 2001, Mr. Mooring testified that he was unaware of any firms making SDRAMs or DDR SDRAMs as to which Rambus would not claim patent protection. (CX2066 at 13-14 (Mooring, Dep.)).

1953. In late 1999, Rambus told Hitachi that it believed Hitachi’s SDRAM and DDR SDRAM products infringed Rambus’s patents. Rambus gave a presentation to Hitachi detailing which Hitachi products it believed infringed various Rambus patents. (CX2102 at 445-47 (Karp, Dep.)).

1954. In April 2000, Rambus told Mitsubishi that it believed Mitsubishi’s SDRAM and DDR SDRAM products infringed Rambus’s patents. (CX1109 at 1 (April 3, 2000 letter: “Rambus owns patents that are directed to various aspects of, and features implemented in Single Data Rate and Double Data Rate SDRAMs, and Cache DRAMs (‘CDRAMs’). . . . We wish to meet with Mitsubishi to discuss these patents and allowed applications in connection with Mitsubishi’s SDRAMs and CDRAMs.”); Crisp, Tr. 3435-3436).

1955. In April 2000, Rambus told NVidia that it believed NVidia products that interfaced with SDRAM and DDR infringed Rambus patents. (CX1371 at 3, 8) (chart: “Rambus IP - NVidia Product Line Overview”).

(CX1359 at 1, *in camera* ()).

1956. In June 2000, Rambus informed Hyundai that it believed Hyundai’s SDRAM and DDR SDRAM products infringed Rambus’s patents. (CX1129 at 1 (June 23, 2000 facsimile: “We have reviewed Hyundai’s memory product line and we believe that many of your products infringe one or more claims of the above-identified patents.”); Crisp, Tr. 3435-3436). Rambus also attached a chart detailing which Hyundai DDR and SDRAM products it believed infringed various Rambus patents. (CX1129 at 1-4 (“To facilitate your consideration of this matter, we have attached a chart summarizing our preliminary position by Rambus patents and Infineon product.”)).

1957. In June 2000, Rambus informed Infineon that it believed Infineon’s SDRAM and DDR SDRAM products infringed Rambus’s patents. (CX1127 at 1 (June 23, 2000 facsimile: “We have reviewed Infineon’s memory product line and we believe that many of your products infringe one or more claims of the above-identified patents.”)). Rambus also attached a chart detailing which Infineon SDRAM and DDR products it believed infringed various Rambus patents. (CX1127 at 1-2 (“To facilitate your consideration of this matter, we have attached a chart summarizing our preliminary position by Rambus patent and Infineon product.”)).

1958. In or about June 2000, Rambus informed Samsung and other memory manufacturers that it believed their SDRAM and DDR SDRAM products infringed Rambus’s patents. (Rambus Answer at 38, ¶ 92; CX2559 at 3).

1959. Rambus has asserted patents against JEDEC-member companies using programmable CAS latency, programmable burst length, on-chip DLL and dual edge clock technologies in JEDEC-compliant SDRAMs, SGRAMs, DDR SDRAMs and DDR SGRAMs, as well as memory controllers that interface with them. (CCFF 1960-67).

1960. Rambus has asserted that its innovations include “Programmable latency register on a SDRAM,” “Programmable burst techniques implemented on a SDRAM,” “DLL implemented on a SDRAM,” and “Double data rate.” (CX1371 at 5; CX1383 at 4; *see also* CX1363 at 1).

1961. Rambus has asserted that “programmable latency on a DRAM” and “Programmable burst on a DRAM,” as used in SDRAMs, are Rambus innovations covered by its patents. (CX1363 at 3).

1962. Rambus has asserted that “programmable latency on a DRAM,” “Programmable

burst on a DRAM,” “DLL implemented on a DRAM” and “Double data rate,” as used in DDR SDRAMs, are Rambus innovations covered by its patents. (CX1363 at 3).

1963. Rambus has asserted that its issued patents cover programmable CAS latency, as described and depicted in JEDEC SDRAM and DDR SDRAM data sheets and individual company data sheets. (CX1371 at 46, 53 (demonstrating that the phrase “value which is representative of a time delay after which the memory device responds to a read request” in claim 44 of Rambus’s ‘365 patent corresponds to the CAS latency portion of the mode register diagram in the JEDEC 64M DDR SDRAM Data Sheet); CX1383 at 47, 51 (same); *id.* at 20, 23 (demonstrating that same language from claim 23 of Rambus’s ‘195 patent corresponds to the CAS latency portion of the mode register in Micron’s 16M SDRAM Datasheet); *id.* at 41, 44 (similar language from Rambus’s ‘918 patent compared to the CAS latency portion of Micron’s 16M SDRAM Datasheet)).

1964. Rambus also disclosed to NVidia the specific language of a claim in a pending patent application – claim 190 of its application no. 09/357,989. Rambus demonstrated how the elements of that claim correspond to specific elements of the JEDEC 64M DDR SDRAM Data Sheet, including the functional block diagram and the mode register diagram of that JEDEC data sheet. (CX1371 at 33-36, 35 (demonstrating that the term “value” in the element “a value which is representative of a number of clock cycles of a first external clock signal to transpire before data is output by the memory device” in claim 190 corresponds to the CAS latency portion of the mode register diagram in the JEDEC 16M DDR SDRAM Data Sheet.)

1965. Rambus has asserted that its issued patents cover programmable burst length, as described and depicted in JEDEC SDRAM and DDR SDRAM data sheets and individual company data sheets. (CX1371 at 64, 68 (demonstrating that the phrase “a first amount of data to be output onto a data bus in response to a read request” in claim 1 of its ‘214 patent corresponds to the burst length portion of the mode register diagram in the JEDEC 64M DDR SDRAM Data Sheet); CX1383 at 60, 64 (same); *id.* at 31, 36 (demonstrating that similar language from Rambus’s ‘918 patent corresponds to the burst length portion of the mode register in Micron’s 16M SDRAM Datasheet)).

1966. Rambus has asserted that its issued patents cover on-chip DLL as depicted in JEDEC SDRAM and DDR SDRAM data sheets. (CX1371 at 84-85 (demonstrating that the term “delay locked loop” in claim 11 of its ‘214 patent corresponded to the indication “DLL” in the functional block diagram of the JEDEC 64M DDR SDRAM Data Sheet)).

1967. Multiple witnesses have testified that Rambus has asserted that its patents cover use of programmable CAS latency, programmable burst length, on-chip DLL and dual edge clock in JEDEC-compliant SDRAMs and DDR SDRAMs. (Lee, Tr. 6776-77; Rhoden, Tr. 529-531).

(CX1384 at 1-5, *in camera*; Macri, Tr. 4753-55, *in camera*).

(Macri, Tr. 4756, *in camera*).

1968. Rambus has also asserted that its issued foreign patents cover use of programmable CAS latency, programmable burst length, on-chip DLL and dual edge clock in JEDEC-compliant SDRAMs and DDR SDRAMs. (Bechtelsheim, Tr. 5884-85; CCF 1969-74).

1969. In a presentation involving Rambus's foreign patents, Rambus matched elements of claim 1 of its European Patent No. EP 0525068 B1 to portions of Infineon's 256M DDR SDRAM Datasheet that illustrated the DDR SDRAM's mode register, the storing of CAS latency information in the mode register and the timing of data output following the CAS latency. (CX1268 at 1-8).

1970. In a presentation involving Rambus's foreign patents, Rambus matched elements of claim 5 of its European Patent No. EP 0525068 B1 to portions of Infineon's 256M DDR SDRAM Datasheet that illustrated the DDR SDRAM's delay lock loop. (CX1268 at 13-14).

1971. The block diagram from the Infineon 256 DDR SDRAM Datasheet used by Rambus to match elements of claims 1 and 5 of European Patent No. EP 0525068 B1 is nearly identical to a functional block diagram contained in the DDR SDRAM specification JESD 79. (CX1268 at 4, 14; JX0057 at 8).

1972. In a presentation involving Rambus's foreign patents, Rambus matched elements of claim 1 of its European Patent No. EP 0525068 B1 to portions of Micron's 64M DDR SDRAM Datasheet that illustrated the DDR SDRAM's mode register, the storing of CAS latency information in the mode register and the timing of data output following the CAS latency. (CX1269 at 1-8, 22-28, 37-44, 57-63).

1973. In a presentation involving Rambus's foreign patents, Rambus matched elements of claim 5 of its European Patent No. EP 0525068 B1 to portions of Micron's 64M DDR SDRAM Datasheet that illustrated the DDR SDRAM's delay lock loop. (CX1269 at 13-14, 48-49).

1974. The block diagram from the Micron 64M DDR SDRAM Datasheet used by Rambus to match elements of claims 1 and 5 of European Patent No. EP 0525068 B1 is nearly identical to a functional block diagram contained in the DDR SDRAM specification JESD 79. (CX1269 at 4, 14; JX57 at 9).

B. Rambus Has Pursued a Strategy of Licensing DDR SDRAMs Only at Royalty Rates Higher than Those Charged for RDRAMs, in Order to Discourage Use of DDR SDRAMs.

1975. Part of Rambus's licensing strategy for SDRAM and DDR SDRAM was to approach Asian DRAM manufacturers first. (CX1273 at 5, *in camera* (

); CX1273A at 6 ("Timeline" listing presentations to "Major Asian DRAM companies" before presentations to U.S. and European DRAM companies); CX1273A at 12 (work schedule discussing "Asian exec presentations")).

1976. Rambus also initially targeted companies that were not supportive of RDRAM. (CX1366 at 5 (February 2000 Rambus Presentation: "Rambus IP . . . Initial focus is on those companies not helping to grow RDRAM market")).

1977. Through its licensing strategy, Rambus sought to reduce the competitive threat that SDRAM and DDR SDRAM posed to RDRAM. (CX1097 at 2 (Tate January 2000 email: one way to convince DRAM companies to pay royalties on RDRAM is to "reduce attractiveness of alternatives"); CX1115 at 3, *in camera* (

); CX2109 at 229 (Davidow, Dep.); CX1385 at 112 (suggesting that one of the ways for Rambus "to win" was to decrease the RDRAM price premium through "[r]oyalties on alternative DRAMs (eg SDRAM and DDR)"); CX1411 at 3 ("Fight like heck for RDRAM, Have DDR/Lex hammer in order to win on RDRAM, Can make RDRAM more attractive than DDR, 'If we're paying Rambus anyway'"); CX1273A at 9 ("Objectives for DDR . . . Royalty rates for DDR products are higher than [RDRAM] products . . . by at least 100%, Level the playing field – at least from a perception point of view, Reverse current momentum on Direct vs. DDR design wins"); CX1273A at 23 ("2000: Regain Momentum . . . Publicly disclose DDR licensing policy, Partners choose to ship RDRAMs over DDR, 2003 - Rambus technology will be used"); CX1864 at 6 ("Our policy is that a competitive memory interface that utilizes our patented inventions to achieve its performance cannot have a lower royalty rate than the RDRAM compatible interface")).

1978. Rambus charged a higher royalty rate for DDR than SDRAM because Rambus believed that DDR was more of a threat to RDRAM. (CX2098 at 453-54 (Mooring, Dep.), *in camera* (); CX1864 at 6 ("Why lower royalty on SDRAM? . . . we have never viewed SDRAM as competition . . . DDR on the other hand was created specifically to compete with Direct RDRAM"); CX2070 at 78-81 (Harmon, Dep.); CX2102 at 306 (Karp, Dep.) (when Joel Karp came to Rambus in late 1997 and started working on non-compatible licensing, he initially focused more on DDR than SDRAM, because it was his "sense . . . that DDR was looked on as more of a problem for Rambus than anything else at that point.")).

1979. Rambus made it clear to companies that the royalty rates for SDRAM and DDR SDRAM would be higher than the royalty rates for RDRAM. (CX1864 at 1 (Rambus press release after Hitachi settlement noting the higher royalty rates for SDRAM and DDR than for RDRAM); CX1680 at 18, *in camera* (); CX1384 at 5, *in camera* (); CX1420 at 8, *in camera* (); Heye, Tr. 3898-99, *in camera* ()).

1980. All companies that signed SDRAM/DDR-related license agreements with Rambus agreed to pay royalties on DDR that exceeded Rambus's RDRAM royalty rates. (CX1385 at 102 ("All agreements provide DDR memory and logic royalty rates which are greater than the Rambus compatible royalty rates"); CX1382 at 33; CX2080 at 181 (Karp, Dep.); McAfee, Tr. 7623, *in camera*; CX2067 at 147 (Davidow, Dep.) (qualitatively the rate for DDR is higher than the rate for RDRAM); CX1403 at 27 ("DDR memory and logic royalty rates are greater than Rambus-compatible royalty rates")).

1981. Rambus used a carrot and a stick approach when discussing terms with potential licensees. (CCFF 1982-86).

1982. Several years before Rambus began enforcing its patents, in spring 1998, Joel Karp and Rambus marketing executive Subodh Toprani discussed using a "stick and carrot" approach when talking with companies about Rambus's intellectual property. (CX1744A at 48, 52; CX2114 at 127-128 (Karp, Dep.) ("there was this idea of a stick and a carrot . . . you would have some kind of reward system. . ."); CX2114 at 129-130 (Karp, Dep.) ("The twig concept so bundles of division equals a stick.")).

1983. Rambus informed a number of companies that, if they did not sign a license agreement by a particular date selected by Rambus, Rambus would unilaterally raise their royalty rates. (CCFF 1984-89).

1984. Rambus offered Mitsubishi favorable terms if it signed a SDRAM/DDR license agreement early, but also told Mitsubishi that in a few weeks the preferential licensing terms may not be available and Rambus would be "free to pursue other courses of action if [it] needed to." (CX2060 at 73-82 (Tate, Dep.)).

1985.

(CX1141 at 1, *in camera*). Tate also informed NEC that if it did not immediately reach an agreement, Rambus and "send an official notice of patent infringement to NEC." (CX1141, *in camera*; CX1141A at 1).

1986. Rambus CEO Geoffrey Tate offered Samsung the “most favored royalty rate,” which he argued would give Samsung a “substantial competitive advantage” over companies that chose to litigate rather than agree to Rambus’s terms. (CX1146 at 1). At the same time, Mr. Tate threatened to charge Samsung higher rates if it did not immediately sign the license agreement. (*Id.* (“If Samsung doesn’t sign now, Samsung’s eventual license terms will be on much less favorable terms and Samsung will be at a competitive disadvantage to NEC/Elpida and Toshiba.”)).

1987.

(CX1384 at 1, 2, 4, *in camera* (
)).
))

1988.

(CX1396 at 1, 3, 5, *in camera* (
); CX1394 at 3, 5, *in camera* (
)).

1989.

(CX1384 at 2, *in camera* (
); Macri, Tr. 4753-55, *in camera* (
)).

).

1990. Part of Rambus’s patent licensing strategy was to demand higher royalty rates from any DRAM manufacturer that refused to license Rambus patents and instead chose to litigate. (CX1385 at 99 (“Rambus Licensing Approach . . . Those companies that decide to litigate will pay higher royalty rates”); CX1382 at 31 (same); CX1379 at 13 (Rambus Policy on Licensing, Settle: Now - Best terms, Later - Higher, but still good; Fight: Then settle - Even higher terms”)).

1991.

(CX1687 at 2, *in camera*).

1992. Part of Rambus’s patent licensing strategy was to consider refusing to license any DRAM manufacturer that chose to litigate. (CX1385 at 99 (“Rambus Licensing Approach . . . Rambus may not license those companies that litigate and lose”); CX1382 at 31 ; CX1097 at 1 (Tate January 2000 email: if Hitachi insists “on a fight to the finish we have said we want an injunction: NO LICENSE.”); CX2109 at 211-212 (Davidow, Dep.); CX1379 at 13 (Rambus

Policy on Licensing . . . Fight: Then settle - Even higher terms, Until decision - No guarantee of a license”)).; Rambus Answer at 39, ¶ 94 (“Rambus admits that certain Rambus employees have said that Rambus might treat firms that chose to litigate rather than enter licensing agreements with Rambus less favorably than others.”)).

1993. Rambus intended to threaten to refuse to license its patents to DRAM manufacturers that were unsuccessful in litigation. (CX1864 at 3 (Rambus internal Q&A: “if we are forced to litigate in court, we reserve the right to refuse to license.”)).

1994. Rambus believes it does not have an obligation to license its patents. (CX1097 at 1 (When asked if Rambus had to license Hitachi, Rambus CEO Geoffrey Tate replied “we have NO obligation to do so”); CX3124 at 235 (Vincent, Dep.) (“Rambus would not be under an obligation to license somebody if they didn’t want to”); CX2109 at 212 (Davidow, Dep.) (“I don’t think we had to license anybody.”); Bechtelsheim, Tr. 6387 (“it became public in the press . . . that they may not license companies on these patents moving forward.”); CX1864 at 6 (June 2000 Rambus press release Q&A: “We have no obligation to license our patent at all.”)).

C. After Rambus Sued Hitachi, Several Companies Signed License Agreements Calling For Payment of Royalties to Rambus for SDRAMs and DDR SDRAMs.

1995. On January 18, 2000, Rambus initiated litigation against Hitachi in federal district court in Delaware, alleging that Hitachi’s SDRAMs and DDR SDRAMs infringed Rambus patents. (CX1855 at 1-14 (Complaint for Patent Infringement asserting that Hitachi’s JEDEC-compliant SDRAMs and DDR SDRAMs infringed Rambus patents); Crisp, Tr. 3435 (“Rambus did sue Hitachi at one point for patent infringement”); Rambus Answer at 39, ¶ 95).

1996. Days after Rambus filed a patent infringement lawsuit against Hitachi, Rambus was still concealing from Samsung that Rambus believed SDRAM and DDR SDRAM infringed Rambus patents. On January 23, 2000, Rambus misled Samsung executives about the nature of Rambus’s lawsuit against Hitachi, implying that Rambus sued Hitachi over a contract breach relating to RDRAM. (CX1099A at 1 (Tate January 23, 2000 email: “our strategy in this meeting was to avoid discussing sdram/ddr/infringing ip . . . yw’s first question was ‘why did you sue hitachi . . . we said 1. hitachi has contracts with rambus for r-chips going back to 93 but have never shipped anything”)).

1997. On March 23, 2000, Rambus filed a section 337 complaint against Hitachi before the United States International Trade Commission alleging that Hitachi unlawfully imported products infringing Rambus patents. (CX1859 at 5, 20).

1998. Rambus’s objective in filing these lawsuits against Hitachi was to stop the import, sale, manufacture and use of Hitachi’s DDR and SDRAM products. (CX1366 at 5 (“Hitachi

Lawsuit; Filed by Rambus 1/18/00 in Delaware . . . Objective of suit: injunctions against import, sale, manufacture, & use of Hitachi products”).

1999. In June 2000, Hitachi settled with Rambus and agreed to pay a royalty on SDRAMs and a royalty on DDR SDRAMs. (CX1864 at 1; Rambus Answer at 39, ¶ 95; CX1681 at 15, *in camera*).

2000. (CX1681 at 15, *in camera* (); CX1680 at 4, *in camera* (); CX1683 at 13, *in camera* (); CX1685 at 19, *in camera* (); CX1686 at 17, *in camera* (); CX1687 at 16, *in camera* (); CX1689 at 20, *in camera* (); CX2059 at 236-37 (Karp, Dep.), *in camera*).

2001. Rambus CEO Geoffrey Tate testified that Rambus (CX2060 at 297-298 (Tate, Dep., *in camera* treatment requested) ()).

2002. Intel believed the Rambus-Hitachi litigation “poison[ed] the industry” by further straining relations between Rambus and DRAM suppliers. (CX2559 at 3 (MacWilliams-Burns June 2000 email exchange: Subject: “Rambus and Hitachi Settle legal dispute . . . [things] turned much more ugly this week in Abid’s meeting with DRAM suppliers. Rambus has sent letters to more of them, including Samsung. . . . Bottom line is that Rambus appears to have taken yet another step in poisoning the industry. The extent of this was not expected.”); MacWilliams, Tr. 4903 (Rambus was “going to the extent of taking legal action against some of the same vendors, it was very concerning to us that these vendors might not even want to do business with Rambus in the future”)).

2003. In 2000, a number of companies signed license agreements with Rambus covering SDRAMs and DDR SDRAMs. (Crisp, Tr. 3436-37; Rambus Answer at 39, ¶ 93).

2004. In June 2000, Toshiba signed a license agreement with Rambus that included a royalty on SDRAMs and a royalty on DDR SDRAMs. (CX1680 at 4, *in camera*; CX2558 at 1 (June 2000 Ahmad email: “Toshiba, last week signed a license for DDR and SDR (PC100/PC133) to cover themselves against any DDR/SDR IP they may have”)).

2005. (CX1683 at

13, 24, *in camera*).

2006.

(CX1685 at

19, 34, *in camera*).

2007. By September 2000, Rambus had secured licenses with several major semiconductor companies, representing over 20% of worldwide SDRAM production. (CX1385 at 101 (“4 SDRAM/DDR Patent Licensees; NEC, OKI, Toshiba, Hitachi; 3 of the 7 largest semiconductor companies . . . >20% of the Worldwide SDRAM Production”)).

2008.

(CX1687 at 16, 28, *in camera*).

2009.

(CX1686 at 17, 32, *in*

camera).

2010. By November 2000, Rambus had license agreements covering SDRAM and DDR SDRAM with more than 40% of the DRAM market. (CX1391A at 8 (“>40% SDRAM/DDR market licensed our IP”); CX1154 at 1 (“great job on samsung/lexington!! . . . great job by Neil & the IP team for their excellent work in getting the SPP1 [strategic patent portfolio] patents and negotiating long and hard for months . . . with samsung on board we now have about 40% of the dram market . . . licensed for sdr/dDR. considering it was about 1 year ago that neil/joel first went to see hitachi this is FANTASTIC progress. add to that the ~10%ish share for r dram and we are close to getting royalties from HALF of the entire dram market! we’re not done with the lexington campaign but we sure are winning!”)).

2011.

(CX 1689 at 20, 37, *in camera*).

2012. By July 2001, Rambus had signed SDRAM/DDR SDRAM license agreements with DRAM manufacturers (Toshiba, Hitachi, NEC, Elpida, Oki, Samsung, Mitsubishi, Matsushita (controllers)) accounting for over one half of the DRAM market. The remaining hold-outs (Infineon, Hyundai, Micron) accounted for the remainder of the DRAM market. (CX1403 at 28, 49).

2013.

(CX1364 at 1-2, *in camera* (

); CX1681 at 10, *in camera* (

); CX1683 at 10, *in camera* (); CX1687 at 12, *in camera* ()
); CX1685 at 12, *in camera* (); CX1689 at 14, *in camera* ()
); CX1686 at 11, *in camera* (); CX1680 at 24, *in camera* ()
)).

D. Several Companies Refused Rambus’s Licensing Demands and Face Patent Litigation with Rambus In the United States and in Various Foreign Countries.

2014. Several companies did not sign license agreements with Rambus for SDRAMs and DDR SDRAMs. (Crisp, Tr. 3437).

2015. On August 7, 2000, Rambus filed a patent infringement lawsuit against Infineon Technologies in a German District Court. (CX1866 at 1, 28; Crisp, Tr. 3437).

2016. On August 8, 2000, Rambus filed a patent infringement lawsuit against Infineon Technologies in federal district court in Virginia. (CX1867 at 1; Crisp, Tr. 3437; Rambus Answer at 40, ¶ 97). Infineon asserted various counterclaims, including fraud and antitrust violations. (Rambus Answer at 40, ¶ 97).

2017. On August 10, 2000, Rambus informed Infineon that it would proceed with patent infringement litigation unless Infineon signed Rambus’s proposed license agreement. (CX1137 at 1 (“if we are not able to reach agreement on Monday, or make acceptable progress towards finalizing our agreement, we will proceed with litigation.”)).

2018. (CX3111 at 1, *in camera*)
(); CX3112 at 1-2, *in camera*).

2019. In August 2000, Hynix sued Rambus in federal district court in California seeking a declaratory judgment that its manufacture and sale of JEDEC-complaint SDRAM did not infringe Rambus’s patents. (CX1878 at 2-3; Rambus Answer at 40-41, ¶ 98)). Hynix also accused Rambus of antitrust violations, unfair competition, and breach of contract. (CX1878 at 2-3). Rambus asserted counterclaims accusing Hynix of patent infringement. (CX1891 at 1-5; Rambus Answer at 40-41, ¶ 98). The court stayed the lawsuit pending a final ruling in the Infineon litigation. (Rambus Answer at 41, ¶ 98).

2020. In August 2000, Micron sued Rambus in federal district court in Delaware seeking a declaratory judgment that its manufacture and sale of JEDEC-complaint SDRAM did not infringe Rambus’s patents. (CX1880 at 16-21; Rambus Answer at 41, ¶ 99; CX1140 at 1) (Appleton August 2000 email: “Based on Rambus’ past and recent behavior the only way to

have a sensible resolution is through litigation. Although this is unfortunate, it appears to be compelled by Rambus' action in dealing with others in the industry. We feel strongly that neither judge or jury will approve of Rambus' behavior.”). Micron also accused Rambus of monopolization, attempted monopolization, and deceptive trade practices. (CX1880 at 12-15). Rambus asserted counterclaims accusing Micron of patent infringement. (CX1880 at 29-38; Rambus Answer at 41, ¶ 99). The court stayed the lawsuit pending a final ruling in the Infineon litigation. (Rambus Answer at 41, ¶ 99).

2021. Rambus litigation has cost Micron tens of millions of dollars and distracted valuable staff resources. (Appleton, Tr. 6398-99).

2022. Each of the Rambus patents involved in the Infineon, Micron, and Hynix lawsuits claims priority to Rambus's '898 application. (Rambus Answer at 41, ¶ 100). Moreover, every patent that Rambus has asserted in patent litigation can trace its lineage to one of two patent applications in the '898 family: either the 08/222,646 (“'646”) or the 07/847,961 (“'961”). (First Stipulations, No. 22; Exhibit A to First Stipulations, No. 22; Nusbaum Tr. 1506-1508; see also DX0014). The '646 and '961 applications, as well as the '490 application which was a continuation of the '961 application, and the '327 patent which issued from the '646 application, were pending while Rambus was a member of JEDEC (CCFF 1008, 1028, 1049, 1076-77, 1092-95) and contained claims that related to ongoing work at JEDEC (CCFF 1028, 1049, 1125-63, 1164-82, 1199-1215, 1216-37).

2023. Rambus believes it possesses additional patents and patent applications, some claiming priority back to the '898 application, that it could in the future seek to enforce against memory manufacturers producing JEDEC compliant SDRAM. (Rambus Answer at 41-42, ¶ 101 (“Rambus admits the allegations in paragraph 101 of the Complaint”).

2024. Rambus has numerous foreign patents that are directly based on its original U.S. patent application no. 07/510,898 (the '898 application). (CX1452 (India); CX1453 (Taiwan)). Many of these foreign patents claim priority based on the '898 application and the benefit of its April 18, 1990 U.S. filing date. (CX1485 (Israel); CX1489 (Israel); CX1496 (Israel); CX1499 (Israel); CX1515 (Korea); CX1527 (Germany); CX1529 (Europe); CX1533 (Europe); CX1536 (Europe)).

2025.

(CX2072 at 45-46 (Tate, Dep.), *in camera*).

2026. Rambus is involved in patent infringement lawsuits in various foreign countries that involve foreign patents that cover some of the same inventions at issue in the U.S. litigation. (Rambus Answer at 42, ¶ 102).

2027. In August and September 2000, Rambus filed several patent infringement lawsuits against Micron in European countries. Rambus alleged that Micron's SDRAM and DDR SDRAM products infringed Rambus's foreign patents. (CX1869 at 1, 40 (patent infringement lawsuit against Micron Semiconductor in a German District Court); CX1871 at 1 (patent infringement lawsuit against Micron in a British Patent Court); Appleton, Tr. 6396-6397 (Rambus asserted foreign patents against Micron in France, Germany, Italy, and the United Kingdom)).

2028. Rambus's foreign patent infringement lawsuits "pose risks" for Micron. (Appleton, Tr. 6397-98 (Micron has invested hundreds of millions of dollars in its Italian wafer manufacturing plant, which employs 1,500 to 2,000 people)). If Micron had to shut down its European operations due to litigation with Rambus, it would lose a major source of its product. (Appleton, Tr. at 6397-98 ("we wouldn't be able to service our customers with the products that they're currently buying from there")). If successful, Rambus's foreign patent infringement lawsuits would have a global impact on Micron's business. (Appleton, Tr. 6397-98 (the product that Micron makes in Europe "gets sold around the world"))).

2029. Rambus President Bill Davidow testified that even if Infineon prevailed in its litigation with Rambus, "there [was] a whole set of subsequent patents that they would be litigating." (CX2067 at 110 (Davidow, Dep.)).

2030. In a May 2001 press release, Rambus stated that it has additional U.S. and foreign patents covering SDRAMs and DDR SDRAMs that it has not yet asserted in any litigation. (CX1888 at 1 (Rambus May 2001 press release: "Rambus holds newly issued U.S. and European patents covering Rambus inventions used by SDRAMs and DDR SDRAMs that have not yet been asserted in any litigation and are not impacted by the [Infineon trial] Court's decision.")).

2031. In July 2001, Rambus noted that the "Virginian decision involved only 4 patents" and that Rambus has "many others which are used by SDRAM/DDR." (CX1403 at 30).

2032. In July 2001, Rambus admitted that even if it lost in the U.S. litigation, it could still successfully enforce its foreign patents. (CX1890 at 35 (Rambus Senior Vice President of Finance and CFO Bob Eulau: "I'll take a question then which is "What is the likelihood of SDRAM licensees not paying due to the Virginia outcome? We don't think this is very likely. . . We've said that the litigation requires success in a major jurisdiction, but not in every jurisdiction.")).

E. Rambus's Enforcement of Patents with Respect to Technologies Incorporated in the JEDEC SDRAM and DDR SDRAM Standards Has Caused, and Will Cause, Substantial Economic Harm and Threatens the Integrity of Open Standard Setting.

2033. Rambus has raised the price for use of programmable CAS latency, programmable burst length, on-chip DLL, and dual edge clocking technologies in DDR SDRAM from free (i.e. 0%) to a royalty of . (CCFF 734, 742, 745, 2000).

2034. Rambus has the power to raise the royalty for use of programmable CAS latency, programmable burst length, on-chip DLL, and dual edge clocking technologies higher, and has stated its intention to do so. (CCFF 2035, 2041-43).

2035. In 2000 and 2001, Rambus planned to continue increasing its royalty rates on SDRAM, DDR SDRAM, and RDRAM. (CX1380A at 3 (August 2000 KR01 Kickoff Meeting: “We are ratcheting up royalty rates over time to the value of the IP”); CX1391A at 32-33 (November 2000 Big Picture Update: “over time we can drive royalties [on RDRAM] from 1-2% average to 3-5% (DDR shows the value of our technology; price our own standards to value)”).

2036. (CX1273 at 11, *in camera* ()).

2037. Rambus plans to charge companies that decide to litigate higher royalty rates, or it will decide not to offer any license to those who lose. (CX1385 at 99 (“Rambus Licensing approach . . . Those companies that decide to litigate will pay higher royalty rates. Rambus may not license those companies that litigate and lose.”).

2038. Rambus’s requested royalty rate would cost Micron hundreds of millions of dollars. (Appleton, Tr. 6390-92).

2039. Rambus claims that approximately 90% of the entire DRAM market is covered by Rambus patents. (CX1386 at 4 (“Today - We are on the cusp of achieving our original BHAG [big hairy audacious goal] - SDRAM+DDR+RDRAM>>90% of the DRAM market - SDRAM/DDR: ~20% paying us royalties now; all by 01E”); CX2112 at 309-310 (Mooring, Dep.) (FTC Deposition January 2003: “If I were to guess on a revenue basis in the most recent quarter . . . I would think that DDR is about 50 percent, SDRAM 40 percent, RDRAM less than 10 percent with EDO taking up the piece that RDRAM doesn’t make in the 10 percent. It’s a guess.”); CX2067 at 171 (Davidow, Dep.) (“Q. So am I right, then, that it’s Rambus’s position [] that any SDRAM or RDRAM being used in main memory PCs today [January 31, 2001] are covered by their patents? . . . [A] I would say that it is highly likely that is true.”)).

2040. In the year 2000, Rambus’s 5-year goal was to collect royalties on over 90% of the DRAM market. (CX1380A at 3 (“5 year objectives . . . All/90%+ DRAMs/controllers pay us royalties”)).

2041. Graphs from Rambus's "November 2000 Big Picture Update" show, during the 2000-2005 period, (1) Rambus's "Market Share" increasing to 100%; (2) its "Average Royalty Rate" increasing from 1% to 5%; and (3) its annual royalty income increasing from \$90 million to \$3 billion. (CX1391A at 32).

2042. One of Rambus's "2001 Really Big Picture Goals" was to "[c]ollect royalties on all DRAM and controllers forever." (CX1386 at 1, 8; CX1388 at 8 ("BHAG [Big Hairy Audacious Goal] – Our standards dominate the DRAM interface market and our IP is fundamental to all DRAM interfaces forever"))).

2043. Rambus expects to collect
in fees and royalties from DRAM manufacturers. (CX0527 at 1, *in camera* (
); CX0528 at 1, *in camera*; CX0529 at 1, *in camera*; CX0530 at 1, *in camera*;
CX1343 at 22, *in camera*; CX1401 at 10, *in camera* (
)).

2044. Rambus's royalties could cause a decrease in the volume of DDR SDRAM that DDR manufacturers produce. (CX2558 at 1 (Ahmad-Krisa June 2000 email: "in talking with memory suppliers, they are re-evaluating their plans for DDR support. Comments that DRAM suppliers have made are that they do not want to produce DDR DRAMs if they have to pay this high royalty"); McAfee, Tr. 7744-45, 7749-50; CX2561 at 2 (Ahmad August 2000 email: "Feedback from suppliers was that if they do end up signing for a royalty structure for DDR then their [sic] inclination would be to limit the DDR volume"))).

2045. In the long run, the increased royalty cost imposed, or threatened to be imposed, by Rambus on manufacturers of DRAMs and memory controllers are likely to be passed on to customers in the form of higher DRAM prices. (CX2107 at 140 (Oh, Dep.) ("Q: . . . Are you saying that the price to the customer is a function of the cost? A: Certainly, yes."); *see also* CX0839 at 2 (Farhad Tabrizi told Richard Crisp that Hyundai "pass[es] on license fees and royalties to their customers"); McAfee, Tr. 7175-76).

2046. Rambus's conduct has also caused DRAM manufacturers and others to incur substantial litigation-related costs. (Appleton, Tr. 6398-99 (the litigation has resulted in direct litigation costs of tens of millions of dollars; "more importantly, the litigation costs associated with having all of our technical people and our administrative people and individuals like myself, all of us to focus and prepare for these trials and these cases is obviously a great deal of time and a great burden.")).

2047. Rambus's conduct has caused DRAM manufacturers and others to spend time and effort trying to design around Rambus's patented technologies. (Rhoden, Tr. 532-33 (Mr.

Rhoden presented a proposal to JEDEC to change from programmable to fixed CAS latency); Lee, Tr. 6776-6806 (describing efforts to convince JEDEC to adopt alternatives to the technologies claimed by Rambus)).

2048. Rambus's lawsuits seeking an injunction threaten to shut down DRAM plants. (Appleton, Tr. 6397 ("There's no question [the foreign lawsuits instituted by Rambus] pose risks. . . . [In Italy] Rambus even tried to get a preliminary injunction to shut us down there. Fortunately, it wasn't successful, but it would have a – just a dramatic effect on the company.")).

2049. Rambus's conduct threatens to have a significant adverse impact on JEDEC and other standard-setting organizations. (CCFF 2050-54).

2050. JEDEC officials believe that Rambus's conduct and resulting lawsuits could cause a fundamental change in JEDEC and a shift away from open standard setting. (Rhoden, Tr. 536 (Mr. Rhoden, Chairman of the JEDEC Board of Directors and the JC-42 Committee, testified that Rambus' lawsuits could lead to "a fundamental change in JEDEC and a fundamental shift away from open industry standardization.")).

2051. Failure to disclose relevant patents and patent applications could cause companies to refuse to participate open standard setting organizations such as JEDEC. (Rhoden, Tr. 537-38 (industry members would "operate in some other environment rather than disclosing [proposals] in an open environment like JEDEC."); *see also* G. Kelley, Tr. 2474-75 (Mr. Kelley intended to inform Texas Instruments that "IBM would not participate in a standards organization where patent information was being hidden while the process of approval went on"); *id.* at 2476-77 ("If companies like IBM are going to leave the process of standardization out of fear of patented material that is not disclosed during the process of standardization, then the standardization process will be so weakened that it will have very little meaning.")).

2052. Rambus's conduct could also discourage industry participants from relying on standards developed by JEDEC or other standard setting bodies. (Bechtelsheim, Tr. 5888-89 ("if that trust into the nature of an open standards process is violated, it makes it very difficult for me to rely on the standards groups developing standards, and this would be extremely disruptive to the industry at large."); (CX2851 at 15 ("Whatever the outcome of [Rambus's] legal cases, the greatest loser will be the wider semiconductor industry. There is bound to be a loss of confidence in the ability of companies to work collectively under the auspices of bodies such as JEDEC to produce industry standards, and this can only retard future semiconductor development. Knowingly or not, Rambus has done a great job of undermining the credibility of one of the main sources of competition in the IP market - the standards bodies.")).

2053. During the time that Rambus was a member of JEDEC, JEDEC members recognized that failure of members to disclose patents and patent applications relating to JEDEC

work could “destroy the work of JEDEC.” (CX2384 (G. Kelley letter regarding the Quad CAS incident: “I am and have been concerned that this issue can destroy the work of JEDEC. If we have companies leading us into their patent collection plates, then we will no longer have companies willing to join the work of creating standards”); CX0083 at 15-16 (“The result [of any attempt by a member of standards group to patent an emerging standard, even for defensive purposes] is more likely to be loss of mutual trust essential to the success of the standardization effort, as well as a 'clean room' restart of the standards effort aimed at avoiding the patent.”)).

2054. Rambus’s narrow interpretation of the JEDEC disclosure policy, as accepted in part by the two- member majority of the Federal Circuit panel, threatens the ability of JEDEC to function effectively as a standards setting organization. (CX3089 at 3-4 (JEDEC brief amicus curiae: Rambus’s proposed interpretation of the JEDEC disclosure policy, as adopted by the 2- member majority of the Federal Circuit, “impairs JEDEC’s ability to effectively function as a standards setting organization.”); CX3090 at 4 (industry members’ brief amicus curiae: the standard setting process “is deeply impacted by the [Federal Circuit] decision.”); *see also* J. Kelly, Tr. at 2066-67 (if companies can drop their membership without having the duty to disclose, that “destabilizes the whole system.”)).

2055. Paragraphs 2055 - 2099 are unused.

XI. Had Rambus Timely Disclosed its Intellectual Property Claims, JEDEC Would Have Acted to Avoid Granting Economic Power to Rambus.

2100. Had Rambus disclosed to JEDEC before the SDRAM and DDR SDRAM standards were finalized and the industry became locked in to use of the standards that it had pending patent applications that might relate to programmable CAS latency and burst length, on-chip DLL, and a dual edged clock, JEDEC and JEDEC members would have acted to avoid granting economic power to Rambus. CCF 2101-2464.

A. Had Rambus Disclosed On a Timely Basis, JEDEC Likely Would Have Adopted Alternative Technologies.

2101. Had Rambus disclosed the scope of its patent applications while JEDEC was still working on the standards, some JEDEC members testified that they would have adopted alternative technologies. (Sussman, Tr. 1416-17 (“If I understood that there was IP on the programmable [CAS latency and burst length], I would have voted – changed my direction and voted to take the fixed one.”); Prince, Tr. 9022-23 (if she had known before 1996 that Rambus might have patents on programmable CAS latency and burst length, it would have affected her decision-making on those two technologies); Lee, Tr. 6635-36 (if Rambus had disclosed to JEDEC before 1996 that it had a pending patent application that it believed contained claims that would cover use of programmable CAS latency and burst length, he would have opposed the use of those technologies in SDRAM and supported the SDRAM lite device that proposed a fixed latency and length); Lee, Tr. 6717 (if Rambus had disclosed to JEDEC before 1996 that it had a pending patent application that it believed contained claims that would cover the use of dual edged clocking, he would have opposed the vote to standardize dual edged clocking in DDR SDRAM); Lee, Tr. 6686 (if Rambus had disclosed to JEDEC before 1996 that it had a pending patent application that it believed contained claims that would cover use of on-chip PLL or DLL, he would have recommended that Micron avoid using that technology); *see also* Kellogg, Tr. 5136, 5146, 5170, 5187 (IBM would consider patent issues seriously and would certainly consider alternatives); CX2107 at 137 (Oh, Dep.) (Hyundai would not have developed DDR SDRAM if it had known that it would have royalties associated with it); (Meyer, Tr. 440-41 (had Rambus disclosed before 1996, Infineon engineers would have come up with specific proposals for him to present to JEDEC as alternatives to technologies that Rambus would be obtaining patents on.)).

1. There Were Multiple Alternatives To Avoid the Technologies In Question.

2102. There are almost always multiple ideas about what features JEDEC should and should not include in a particular device. (Rhoden, Tr. 414-15). “[I]f you give ten engineers a problem, you’ll probably get 12 or 14 solutions, and the same is true inside the [JC 42.3] committee. People were proposing a number of other approaches to the same type of thing.”

(*Id.* 434-35).

2103. DRAM manufacturers could have developed commercially viable solutions that would have avoided Rambus patents.(CX2109 at 77-78 (Davidow, Dep.) (“I think you could have sat a group of people down in a room and said you can't use this stuff, come up with different solutions and people could have come up with different solutions.”); *Id.* at 77 (“[C]ould they have done alternatives, [] could [they] have competed within the market effectively by making different cost performance trade-offs, my guess is the answer would be [] yes.”)).

2104. Before 1996, there were alternatives to programmable CAS latency, programmable burst length, dual edge clocking, and on-chip DLL. (Jacob, Tr. 5365; Wagner, Tr. 3859-60; Kelley, Tr. 2548-49; CX2109 at 67-68 (Davidow, Dep.) (based on internal discussion at Rambus, Mr. Davidow concluded that there were “many ways to improve performance” without infringing Rambus patents); CX2109 at 68-69 (Davidow, Dep.) (Davidow assumes that JEDEC could have pushed work-arounds to dual edged clocking “pretty far”); CX2109 at 70-71 (“[t]here are lots of other solutions” besides programmable cas latency and burst length)).

2105. Before 1996, JEDEC considered alternatives to programmable CAS latency, programmable burst length, dual edged clocking, and on-chip DLL. (CCFF 2131, 2235, 2323-24, 2367).

2106. It would have been relatively easy to implement alternatives to programmable CAS latency, programmable burst length, dual edged clocking, and on-chip DLL in the 1991-1996 time frame. (Polzin, Tr. 3987-89 (Rambus patents on dual edge clocking, programmable CAS latency, and programmable burst length and on-chip DLL were “pretty simple things to work around if we had known about them a long time ago.”); Peisl, Tr. 4452 (it would have been “relatively easy” to implement alternatives in the early 1990's)).

2107. JEDEC members viewed the alternatives as viable, and many members preferred one or more of the alternatives to the technologies that were actually selected. (Kellogg, Tr. 5117, 5131-32 (testifying that manufacturers would have likely preferred a fixed burst length and that burst length alternatives were viable); Bechtelsheim, Tr. 5811 (testifying that he would have preferred the use of pins to set CAS latency); Sussman, Tr. 1380 (“I had a lot of arguing to do to get the degree of programmable features [programmable CAS latency and burst length] into the [JEDEC standard];” Lee, Tr. 6666, 6683 (testifying that a read clock, or an echo clock, was a viable alternative and that Micron preferred to avoid the use of an on-chip DLL); Kellogg, Tr. 5168-69 (testifying that he preferred vernier circuits to on-chip DLL); Polzin, Tr. 3991-92 (“Pin strapping” was a viable design alternative to the current JEDEC standard of setting CAS latency and “[c]ertainly no more costly.”)).

2. There is No Reliable Evidence to Contradict The Commercial Viability of Alternative Technologies.

2108. Dr. Soderman and Mr. Geilhufe lacked the expertise and experience to conclude what technologies JEDEC members would have considered to be acceptable alternatives to the technologies at issue. (CCFF 2109-2115).

2109. During the relevant time period, neither Dr. Soderman nor Mr. Geilhufe was involved in or supervising the design of DRAMs. (Soderman, Tr. 9342-43; Geilhufe, Tr. 9627-28 (“Of course not. I was an executive in the industry. I was no longer designing.”)).

2110. Much of Dr. Soderman’s recent experience has involved the sales of software. (Soderman, Tr. 9337-38.) Dr. Soderman’s primary experience from 1981 to 1997, at ASIC Design & Marketing, Xilinx, Intel, and LSI Logic, involved programmable logic and gate arrays, not DRAMs. (*Id.* 9338-42.)

2111. Dr. Soderman hasn’t designed a DRAM since the late 1970’s. (Soderman, Tr. 9342-43.) The DRAM he designed was used in typewriters. (*Id.* 9343.)

2112. The last time Mr. Geilhufe formally contributed to a DRAM design was sometime in the mid to late 1980s. (Geilhufe, Tr. 9625-26). Mr. Geilhufe’s last hands-on DRAM design experience was in 1978. (*Id.* 9626).

2113. Neither Dr. Soderman nor Mr. Geilhufe ever designed an SDRAM or DDR SDRAM. (Soderman, Tr. 9342-43; Geilhufe, Tr. 9628). Neither Dr. Soderman nor Mr. Geilhufe ever designed a JEDEC-compliant DRAM. (Soderman, Tr. 9424 (“that particular part was a unique IBM part”); Geilhufe, Tr. 9628).

2114. Mr. Geilhufe worked at Winbond from 1999 to 2000. (Geilhufe, Tr. 9628). Winbond did not design any DRAMs. (*Id.* 9628-29). Mr. Geilhufe’s manufacturing experience at Winbond was limited to being aware of the volumes and types of DRAMs that were being manufactured and the profitability of the DRAM business. (*Id.* 9629).

2115. Neither Dr. Soderman nor Mr. Geilhufe attended JEDEC meetings during the relevant time period. (Soderman, Tr. 9429, 9447-48, 9473 (“[Mr. Macri] was at the [JEDEC] meeting. I was not . . . I have no firsthand knowledge how the JEDEC committee decided to standardize on the [burst length] values.”)). Mr. Geilhufe attended only one JEDEC meeting approximately twenty years ago. (Geilhufe, Tr. 9624). The only person he remembers supervising whose job responsibility included attending standard-setting organization meetings, was an employee of Intel who briefly reported to him sometime in 1975. (Geilhufe, Tr. 9625).

2116. Dr. Soderman and Mr. Geilhufe failed to consult highly relevant materials relating

to JEDEC's consideration of alternative technologies. (CCFF 2117-2221).

2117. Dr. Soderman failed to consider a number of critical presentations at JEDEC. (Soderman, Tr. 9493, 9493-94, 9503-04). Dr. Soderman couldn't recall whether he had considered a number of other important presentations at JEDEC. (Soderman, Tr. 9485-86, 9487 ("I've seen a lot of presentations about incorporating Vernier's on these. They are all kind of blending together, all very similar."); 9491, 9502-03).

2118. Mr. Geilhufe never reviewed any JEDEC meeting minutes or any JEDEC policy manuals. (Geilhufe, Tr. 9622).

2119. Dr. Soderman failed to review the deposition or trial testimony of virtually all the relevant fact witnesses, including Drs. Oh and Peisl and Messrs. Lee, Shirley, Sussman, Kellogg, Heye, Macri, Goodman, Rhoden, Gross, Becker, and Krashinsky. (Soderman, Tr. 9427-28, 9433, 9435, 9440, 9494, 9499, 9503, 9505-06, 9508). Mr. Geilhufe did not recall reviewing the testimony of any fact witness other than the deposition testimony of Dr. Peisl, who disagreed with his conclusions. (Geilhufe, Tr. 9619, 9729-31).

2120. Dr. Soderman failed to interview anybody who had attended JEDEC meetings during the relevant time period and who had observed the JEDEC work in progress. (Soderman, Tr. 9447-48, 9472, 9488, 9491, 9503, 9506-07). As a result, he had no understanding of why various alternatives were proposed at JEDEC, how JEDEC members reacted to it, what was said in the discussions of the alternatives, or which companies supported the alternatives. (*Id.* 9447-48).

2121. Mr. Geilhufe did not do anything to ensure that the analysis that he did was the type of analysis that was done at JEDEC. (Geilhufe, Tr. 9622). Nor did he speak to any JEDEC member or any JEDEC employee to determine how the questions he was asked to answer are answered at JEDEC. (*Id.* 9623). Mr. Geilhufe did not even know whether the questions he was asked to answer were ever asked at JEDEC. (*Id.* 9622).

2122. The methodology that Mr. Geilhufe used to reach his conclusions about the costs of alternative technologies was unreliable. (CCFF 2123-24).

2123. Mr. Geilhufe recognized that his estimates were "rough estimates." (Geilhufe, Tr. 9696). He agreed that the margin of error for each of the cost elements described in his presentation is as high as 25 percent. (*Id.* 9665).

2124. Mr. Geilhufe did not compare his projections in this case with any actual data. (Geilhufe, Tr. 9665-66). Mr. Geilhufe reviewed no evidence in this case relating to the costs of DRAM manufacturers for the product design, good die yield, final test and good unit yield cost elements from the relevant period other than the Peisl deposition and, in the case of good unit

yield, “confidential” evidence that is not in the record. (Geilhufe, Tr. 9680, 9698, 9706).

2125. Dr. Soderman’s conclusions regarding the coverage of certain of Rambus’s patents is inherently unreliable. (CCFF 2126-29).

2126. Dr. Soderman failed to consider technical dictionaries, treatises, or learned texts to determine the common usage of the terms in the claims. (Soderman, Tr. 9478). Dr. Soderman failed to consider the expert reports filed by Rambus’s patent experts in the private patent litigation to determine whether his interpretation of terms was consistent with those of Rambus’s patent experts. (*Id.* 9478-79).

2127. Dr. Soderman failed to present a claims chart or any other analysis demonstrating that each of the elements of the claim is satisfied. (Soderman, Tr. 9371-73, 9373-74 (In analyzing whether claim 1 of the ‘120 patent covers use of transmitting burst length information as part of the read command, Dr. Soderman’s entire analysis of the various terms used in and elements of that claim consists of: “Claim 1 covers this. It just says, ‘receiving block size information’.”)).

2128. Among the terms in claim 1 that Dr. Soderman failed to analyze was the term “operation code.” On cross-examination, Dr. Soderman admitted that he had previously interpreted that term as part of a request packet. (Dr. Soderman, Tr. 9456 (“Operation code . . . something that happens, okay. In this case you were requesting the information that has the protocol packet transmit to the DRAM.”); *id.* 9457 (“Operation code . . . just means some sort of operation to me, and the information here was well defined as transmitting information to this packet to the DRAM.”)). Unlike RDRAMs, JEDEC-compliant SDRAMs and DDR SDRAMs do not use packets. (CCFF 1268, 1272, 1306, 1357).

2129. Dr. Soderman testified previously that other individuals, including patent attorneys or legal opinion, could answer better than he could whether the claims would be infringed only if, in the alternative in question, values representing both the number of clock cycles and block size were received. (Soderman, Tr. 9457-58; *see also id.* 9479 (his conclusion could be subject to a more legal interpretation that he was not prepared to do)).

3. Alternatives to Programmable CAS Latency.

2130. In the 1991-1996 time frame, there were at least six alternatives to the use of programmable CAS latency in JEDEC SDRAM and DDR SDRAM. (Jacob, Tr. 5370-71). JEDEC could have used fixed CAS latency parts. (Jacob, Tr. 5370). Second, it could have had OEMs blow fuses to determine the CAS latency of a part. (Jacob, Tr. 5378-79). Third, it could have chosen to scale CAS latency to clock frequency. (*Id.* 5370). Fourth, it could have chosen to use either an existing or dedicated pin(s) to set CAS latency. (Jacob, Tr. 5385-86). Fifth, JEDEC could have chosen to encode the CAS latency in either the read or write command.

(Jacob, Tr. 5389-90). Sixth, it could have stayed with an asynchronous style DRAM. (Jacob, Tr. 5370-71).

2131. Three of these alternatives – fixed CAS latency, use of fuses to set CAS latency, and use of pins to set CAS latency – were proposed for incorporation in the JEDEC SDRAM standard in the 1991-1992 time period. (JX0010 at 71, 74; CX0034 at 149; Rhoden, Tr. 425-434; Kellogg, Tr. 5136; Williams, Tr. 798; Kelley, Tr. 2548-49).

2132. In the 1991-1992 time period, the manufacturing costs associated with three of these alternatives – fixed CAS latency, use of fuses, or use of a dedicated pin(s) – compared to programmable CAS latency using a mode register were relatively similar. (*See generally* CCF 2133-2177, 2184-2218; Kellogg, Tr. 5143 (“Q. Was there also some difference in cost among the three options? A. This is a fine-grained question in that if "cost" is my ability to react, yes. If "cost" is strictly manufacturing, the difference between these is so -- it's slightly different. It's very difficult to assess, and I don't recall that we actually assigned a cost differential between these. I do believe it's somewhat fine-grained. In other words, it's not a large number.”)).

(A) Fixed CAS Latency.

2133. Fixed CAS latency means that a manufacturer would sell DRAM parts that could operate with only one CAS latency. (Jacob, Tr. 5371). A manufacturer could fix the CAS latency of a part at either the design phase, processing phase, or packaging phase. (Jacob, Tr. 5371).

2134. At the design phase, a manufacturer could design a part to only perform with one CAS latency. (Jacob, Tr. 5373).

2135. A manufacturer could use a metal mask option to fix CAS latency during the processing phase. (Jacob, Tr. 5373-74). To use a metal mask option to fix CAS latency, a manufacturer could hardwire the chip to operate with either a CAS latency of 2 or 3. (*Id.*). During the processing phase, the metal mask would create a connection with either the CAS latency of 2 circuitry or the CAS latency of 3 circuitry. (*Id.*). That connection would determine that CAS latency of the part. (*Id.*).

2136. A manufacturer could use a bond wire option to fix CAS latency during the packaging phase. (Jacob, Tr. 5375). To fix CAS latency during the packaging phase, the manufacturer could design a chip containing both CAS latency 2 circuitry and CAS latency 3 circuitry. (*Id.*). A multiplexor, or a mux, could be attached to both the CAS latency of 2 circuitry and the CAS latency of 3 circuitry. (*Id.*). The CAS latency of the part would depend on whether, during the packaging phase, a bond wire connected the mux to a power pin or a ground pin. (*Id.*).

2137. In comparison to the use of a mode register to program CAS latency, there are technical and cost advantages to fixed CAS latency. (Jacob, Tr. 5376). It is potentially a cheaper design because it eliminates the mode register. (*Id.*). The die size of a part refers to the geographic area that a chip occupies on a semiconductor wafer. (Jacob, Tr. 5377). The cost of a part depends substantially on its die size. (*Id.*). Before 1996, fixed CAS latency was potentially cheaper than using a mode register to program CAS latency because it would require a smaller die size. (Jacob, Tr. 5377). It is potentially cheaper to test fixed CAS latency parts because it is no longer necessary to test each part for operation with multiple CAS latencies. (*Id.*).

2138. In 1991-1992, JEDEC considered using fixed CAS latency. Samsung presented an SDRAM proposal that included a fixed CAS latency of 2. (JX0010 at 71; Rhoden, Tr. 425-27; Kellogg, Tr. 5099-5101).

2139. In 1995-1996, JEDEC considered an SDRAM lite part. (JX0027 at 64-68). The use of a single fixed CAS latency was among the features proposed for SDRAM lite. (Lee, Tr. 6626). The use of fixed CAS latency was proposed to reduce cost. (JX0027 at 65 (NEC's SDRAM lite presentation stated that it would "Save money (for everyone)."); Lee, Tr. 6633 ("It was simpler for us. It was -- it would be faster for design. We felt it would be cheaper to produce and cheaper to test. Our feedback from the test group and design was they much preferred the "lite" device over a full-feature device."))).

2140. Dr. Soderman's testimony that fixed CAS latency would interfere with a manufacturer's ability to speed grade parts and thus would impact a manufacturer's yield is contradicted by the weight of the evidence. (Soderman, Tr. 9347-48; CCF 2141-2148). Likewise, Mr. Geilhufe's testimony that fixed CAS latency would result in reduced yield due to speed distribution is contradicted by the weight of the evidence. (Geilhufe, Tr. 9577; CCF 2141-2148).

2141. Manufacturers supported fixed CAS latency. (CCF 2142-2144, 2146).

2142. In September 1995, NEC made a proposal for an SDRAM lite part in which it proposed a part with a fixed CAS latency of 3. (JX0027 at 65; Lee, Tr. 6626, 6629). NEC's presentation on SDRAM lite stated that it would "save money (for everyone)." (JX0027 at 65). It also proposed to mark parts based on frequency rather than cycle time. (*Id.*).

2143. In the 1995-1996 time frame, there was substantial support for one fixed CAS latency of 3. (JX0029 at 13-14; Lee, Tr. 6627-31 (discussing SDRAM lite survey ballot results). There was unanimous support that no values other than CAS latencies of 2 and 3 were needed. (*Id.*).

2144. Mr. Lee testified that Micron supported SDRAM lite and, in January 1996, fixed CAS latency was acceptable from a technical and cost perspective. (Lee, Tr. 6633). Design and

test groups at Micron, at the time, preferred SDRAM lite. (*Id.* (“Our feedback from the test group and design was they much preferred the "lite" device over a full-feature device.”). Fixed CAS latency “would be faster to design and it would be cheaper to produce and test.” (*Id.* 6626). As Mr. Lee explained, Micron preferred fixed CAS latency at the time because it would have enabled Micron to avoid designing in different modes of operation and considering combinations of CAS latency and burst length. (*Id.*).

2145. Mr. Kellogg testified that there would be a measurable performance advantage to fixed CAS latency “if ‘fixed’ implied no circuitry in the access path.” (Kellogg, Tr. 5138 (“I would just point out that fixed CAS latency would result in measurably improved performance if "fixed" implied no circuitry in the access path.”).

2146. Micron was in favor of using a fixed CAS latency for Burst EDO. At the January 1995 JC 42.3 meeting, Micron made a presentation on a Burst EDO that would use a fixed CAS latency. (Williams, Tr. 823, 825; JX0023 at 68).

2147. Mr. Lee, an experienced engineer for Micron, testified that using a fixed CAS latency would not impact a manufacturer’s ability to speed grade parts. (Lee, Tr. 11012). At the wafer probe stage, a manufacturer would test the part to determine what the highest operating frequency was for the part to operate with a particular fixed CAS latency. (*Id.* (“Q. Now, with respect to the SDRAM-Lite proposal, did you have any concern that if JEDEC adopted that proposal, Micron would not be able to speed grade parts? A . No. Q. Can you please explain why not? A. Sure. We would speed grade our parts, we would be able to test that at probe would be the typical way we would do it, at that time, so we would have the same ability to do that whether it was a fixed latency or multiple latencies.”); *see also* Becker, Tr. 1140-42 (discussing CX2466, which is an Infineon parts catalogue, and testifying that manufacturers speed grade their products by operating frequency)).

2148. Mr. Lee testified further that Micron believed that the yield for SDRAM lite “would be the same or better than the full-feature [SDRAM] part.” (Lee, Tr. 11013).

2149. Both Dr. Soderman and Mr. Geilhufe testified that fixed CAS latency would require multiple parts. (Soderman, Tr. 9346-47; Geilhufe, Tr. 9578). Mr. Geilhufe’s cost model assumed that fix CAS latency would require three parts. (Geilhufe, Tr. 9578). Their testimony is contradicted by the weight of the evidence. CCF 2150-2153.

2150. Although other values have existed, the typical CAS latencies for SDRAM are 2 and 3. (Rhoden, Tr. 394).

2151. For SDRAM, customers primarily use CAS latencies of 2 and 3. (Lee, Tr. 11004-05). No one has used CAS latency of 1 for SDRAM. (*Id.* 11005). Further, no one has used CAS latency of 4 for main memory. (*Id.*).

2152. In the 1995-1996 time frame, JEDEC considered adopting an SDRAM lite part. (Lee, Tr. 11007). “The goal of the SDRAM-Lite was to try to end up with one CAS latency and one burst length.” (*Id.*). Settling on one CAS latency and burst length would have resulted in a simpler part that was cheaper to produce. (*Id.* 11008). There was a unanimous position that no value other than CAS latencies of 2 and 3 were needed. (JX0029 at 13-14).

2153. When JEDEC published Release 9 of Standard 21-C, it had removed CAS latency of 1 from the SDRAM standard because no one was using that CAS latency. (Lee, Tr. 11006-07 (“CAS latency one was being not used, none of the customers were using it as such, so they removed it from the standard.”); *Cf.* JX0056 at 114 (Release 4 showing a required CAS latency of 1) with CX0234 at 150 (Release 9 showing that CAS latency of 1 is no longer either a required or optional feature)).

2154. Mr. Geilhufe testified that fixed CAS latency would involve extra photo tool costs of approximately \$50,000 for each part. (Geilhufe, Tr. 9576). This testimony is contradicted by the weight of the evidence. (*Id.*).

2155. SDRAM lite, which was a proposal for a fixed CAS latency part, would not have involved extra photo tool costs. (Lee, Tr. 11016 (“Okay, my understanding is it did not involve extra tool costs. We were only going to provide the one latency, so there was no other mask required.”)).

2156. Even if SDRAM lite would had included two different CAS latencies, it still would not necessarily have involved extra photo tool costs. (Lee, Tr. 11017 (“[If] [w]e had two choices[,] [w]e could have implemented this with a fuse, which would therefore require no extra tooling, or if we created a second metal mask, then there would be an extra tool charge.”)).

(B) Blowing Fuses to Set CAS Latency.

2157. Manufacturers could have included in their designs CAS latency circuitry with a value of 2 and CAS latency circuitry with a value of 3. (Jacob, Tr. 5378-80; see DX0071). Each hardware would have a fuse attached to it. (*Id.*). The CAS latency of the part would have depended on which fuse was blown. (*Id.*). The latency of the part would correspond to the latency value that was not blown. (*Id.*).

2158. Fuses are used to disable connections between DRAM circuits. (Jacob, Tr. 5379-80). The concept of fuses is that they can select among DRAM circuits by disabling the connection to the undesired circuit while leaving intact the desired circuit. (*Id.*). Antifuses can be used to perform the same function as fuses. (Lee, Tr. 11170-71 (Micron uses fuses for redundancy repair); *see*).

2159. Manufacturers have reliably used fuses since at least the early 1990s for redundancy repair. (Jacob, Tr. 5381; Kellogg, Tr. 5130; Lee, Tr. 11167-70;). In 1991, fuses were commonly used to select between particular functions of a DRAM. (Rhoden, Tr. 428-29 (“So, fuses were pretty common at this time, still are very common, and [Samsung] w[as] proposing using a fuse similar to the ones that were in common use at the time and still today to actually select this option.”)).

2160. It is possible to blow fuses either electrically or with laser technology. (Jacob, Tr. 5380-81; see DX0071-DX0073; Lee, Tr. 11170). Lasers can only blow fuses before packaging. (*Id.*). Electrically blown fuses, however, are typically used to blow fuses after packaging parts. (*Id.*).

2161. Manufacturers could design parts that were capable of operating with more than one CAS latency. (Jacob, Tr. 5378-79). Manufacturers or OEMs could then use fuses to determine the CAS latency of a part. (Jacob, Tr. 5378-79;).

2162. Manufacturers could have used either electrically blown or laser blown fuses to determine the CAS latency of a part on behalf of OEMs. (Rhoden, Tr. 425-28 (discussing a proposal from a DRAM manufacturer, Samsung, to the JC 42.3 Subcommittee to use fuses to determine one of the DRAM’s operating modes); Sussman, Tr. 1379 (“Some companies were saying that we should [not] have [programmable CAS latency or burst length] at all. Their customers only are a very narrow base, not needed. There were some that were proposing that we do it by fuse option.”)).

2163. JEDEC could have adopted use of electrically blown fuses to set CAS latency, which would have permitted either manufacturers or OEMs to set the latency. (Jacob, Tr. 5597;). Manufacturers could have tested the functionality of parts for different CAS latencies before they shipped the parts to OEMs who would have blown electrical fuses to determine latency. (Jacob, Tr. 5597).

2164. Using fuses to determine latency, before 1996, would have been simpler and cheaper and could have lowered test costs. (Jacob, Tr. 5382 (“After blowing the fuse, you would only need to test one CAS latency value instead of having to test all possible CAS latency values, so it would be a cheaper alternative potentially.”)).

2165. Using fuses to determine CAS latency would have preserved a manufacturer’s ability today to use latency as a way to distinguish between faster and slower DRAMs and fetch higher prices for parts that can operate at faster latencies. (Kellogg, Tr. 5141-42;).

2166. At the December 1991 JC 42.3 meeting, Samsung gave a presentation that

proposed a fuse option to select between two different types of DRAM operating modes. (JX0010 at 71 (“Fuse option for serial and interleaved wrap mode.”); Rhoden, Tr. 427-428 (In testifying about Samsung’s presentation, Rhoden stated, “[Serial and interleaved wrap mode] were two different modes of operation of the device, and they were proposing for selecting between those two different burst options. [Samsung] w[as] proposing using a fuse to do that.”)).

2167. At the May 1992 JC 42.3 meeting, Cray gave a presentation that proposed the use of fuses to choose between two different CAS latencies, 2 and 3, for an SDRAM part. (CX0034 at 149 (proposing feature sets, which included CAS latency, for two SDRAM configurations and stating, “[d]efault [s]et fuse programmable by supplier”)).

2168. Both Dr. Soderman and Mr. Geilhufe testified that blowing fuses to test CAS latency would result in fixed CAS latency parts, which would create the same inventory costs that were associated with multiple fixed CAS latency parts. (Soderman, Tr. 9354; Geilhufe, Tr. 9585-86).

2169. If the fuses were blown before packaging, Dr. Soderman and Mr. Geilhufe would be correct that thereafter, the parts would resemble fixed CAS latency parts. The issues identified by Dr. Soderman and Mr. Geilhufe could have been overcome, however, by use of slightly more sophisticated memory controllers that could detect when incompatible DIMMs are placed in the same system. (Jacob, Tr. 5382-83). Or, more sophisticated labeling of DIMMs. (*Id.*). Dr. Soderman and Mr. Geilhufe disregard the advantages of fixed CAS latency parts, including faster access time and lower cost. (Soderman, Tr. 9346-53; Geilhufe, Tr. 9575-79; Jacob, Tr. 5375; Kellogg, Tr. 5138 (“I would just point out that fixed CAS latency would result in measurably improved performance if “fixed” implied no circuitry in the access path.”)).

2170. If OEMs were to blow the fuses to set the CAS latency at the desired value, the issue identified by Dr. Soderman and Mr. Geilhufe as being associated with fixed CAS latency parts would not arise. (Bruce, Tr. 5379 (As Dr. Jacob explains, “[T]he DRAM manufacturer could ship a part that was capable of performing as a CAS latency 2 part or a CAS latency 3 part, ship that part to the OEM and the OEM would blow a fuse and it would at that point become a fixed latency part, but it would have either 2 or 3.”)).

2171. Dr. Soderman and Mr. Geilhufe testified that electrically blown fuses are unreliable. (Soderman, Tr. 9356-57; Geilhufe, Tr. 9581-82). As evidence to support his point, Dr. Soderman testified that only two of the fifty Micron data sheets he reviewed included the use of electrically blown fuses. (Soderman, Tr. 9357). Mr. Geilhufe further testified that antifuse technology is generally not available in the DRAM process. (Geilhufe, Tr. 9583). The testimony of Dr. Soderman and Mr. Geilhufe on fuses is contradicted by the weight of the evidence. CCF 2172-2177.

2172. All of Micron's SDRAM parts use electrically blown fuses. (Lee, Tr. 11022-23). Micron's data sheets do not indicate the use of electrically blown fuses because Micron's use of fuses is transparent, or invisible, to the customer and customers do not use fuses during system operation. (*Id.*).

2173. Inside DRAM chips, there are redundant storage elements which enable the repair of defective elements. In 1991 and 1992, manufacturers used fuses to replace bad bits of memory with good bits. (Rhoden, Tr. 428-29). Manufacturers still use fuses today to perform the same function. (*Id.*). Today, manufacturers use both electrical and laser fuses to disable defective memory storage elements. (Jacob, Tr. 5381).

2174. Micron has used fuses reliably for redundancy repair since at least 1989. (Lee, Tr. 11170, *in camera*). In 1989, it used electrical fuses for that purpose. (*Id.*). For a period of time, Micron used laser fuses. (*Id.*). It then began to use electrically blown antifuses. (*Id.*).

2175.

(Lee, Tr. 11170, *in camera*).

(Lee, Tr. 11170-71, *in camera*).

(*Id.*).

2176. In 1992, IBM used electrical fuses for redundancy repair. (Kellogg, Tr. 5130).

2177. Before 1996, it was potentially simpler and cheaper to use fuses to determine latency. (Jacob, Tr. 5382).

(C) Scale CAS Latency with Clock Frequency.

2178. The concept of scaling CAS latency with clock frequency could be implemented in one of two ways. (Jacob, Tr. 5383). The DRAM could sense the speed of the bus and internally calculate its own CAS latency. (*Id.* 5383-84). Or, the memory controller could tell the DRAM the speed of the bus. (*Id.* 5384-85).

2179. If CAS latency were scaled with clock frequency, parts would operate with their optimum latency. (Jacob, Tr. 5384-85).

2180. Dr. Soderman's testimony that this alternative would require complex additional circuitry carries little weight. (Soderman, Tr. 9358; CCFF 2181).

2181. Dr. Jacob testified that implementing this alternative would only require "a simple circuit that would look at the bus frequency, the existing bus frequency, and do an edge detect to see if the bus frequency is faster than or slower than the internal reference." (Jacob, Tr.

5384).

2182. It is true that this alternative would require either a slightly more sophisticated memory controller or labeling system in order to prevent the situation in which there were DIMMs operating with two incompatible latencies. (Jacob, Tr. 5385).

2183. Dr. Soderman's testimony that this alternative would have been covered by Rambus patents is not supported by any evidence. (Soderman, Tr. 9359). Dr. Soderman did not identify which Rambus patent would be infringed. (*Id.*). Further, he did not engage in any patent analysis whatsoever beyond testifying that the alternative would require "some sort of a register." (*Id.*)

(D) Using Dedicated Pin(s) to Set Latency.

2184. Rather than storing the CAS latency value at which a DRAM will operate in a mode register after system initialization, JEDEC could have dedicated a pin to set the CAS latency value during operation. (Jacob, Tr. 5386).

2185. JEDEC could have used one dedicated pin to store two different CAS latency values. (Jacob, Tr. 5386-87; Lee, Tr. 11025-26). Binary signals, or signals that can carry either a high or a low voltage level, are used to transmit information to DRAMs. (Rhoden, Tr. 359-60). A manufacturer could design a part that would operate as a CAS latency of 2 part when a high voltage level is present on a dedicated pin and a CAS latency of 3 part when a low voltage is asserted on that pin. (Jacob, Tr. 5386-87).

2186. In the 1991-1992 time frame, JEDEC considered the use of pins to set CAS latency. (Rhoden, Tr. 434).

2187. Mr. Bechtelsheim testified that he would have preferred the use of pins to set CAS latency because it was simpler and less effort on the system side. (Bechtelsheim, Tr. 5811 ("Personally, I actually preferred the pins because it was simpler, less effort on the system side, but the JEDEC group chose the mode register.")).

2188. Use of a dedicated pin provided the same advantage of flexibility as programmable CAS latency without the need for circuitry on the DRAM. (Kellogg, Tr. 5127-38 (The use of dedicated pins was "one means by which we could produce parts through the production facility, put them into stock and have those parts capable of doing more than one mode of operation."); *Id.* 5129 ("The predominant advantage is that we could produce a part that could provide multiple functional modes to service a variety of applications.))).

2189. The disadvantage of using dedicated pins to set CAS latency was the test cost, which was also a disadvantage of programmable CAS latency. (Kellogg, Tr. 5127 ("The

predominant disadvantage would be that we would have to test each mode, which would have some impact to our test cost, test time.”); Kellogg, Tr. 5127). Kellogg articulated the same disadvantage for the use of a programmable mode register. (Kellogg, Tr. 5129 (“The predominant disadvantage -- and I'm summarizing here -- was that we would have to test each of the mode register options to ensure they all functioned properly.”)).

2190.

(Macri, Tr. 4770, *in camera*)

2191. Both Dr. Soderman and Mr. Geilhufe assume that JEDEC would have had to add pins to DRAM packages in order to implement the dedicated pin alternative. (Soderman, Tr. 9362; Geilhufe, Tr. 9580). This assumption is not necessarily valid. (CCFF 2192-2201).

2192. JEDEC would not necessarily had to have added new pins to DRAMs in order to implement the dedicated pin alternative to programmable CAS latency. (Jacob, Tr. 5387).

2193. No-connect pins are pins that do not connect to any circuit and therefore have no existing function for the part. (Jacob, Tr. 5387; Lee, Tr. 11030). JEDEC could have used a no-connect pin to set CAS latency. (*Id.*).

2194. JEDEC almost always provides for no-connect pins in its SDRAM and DDR SDRAM pinouts. (Lee, Tr. 11037; CX0234 at 80-142).

2195. At the time JEDEC was considering whether to adopt programmable CAS latency, there were pins available that could have been used to set CAS latency. (Sussman, Tr. 1377-78). Howard Sussman, for example, proposed a package for SDRAM that had a no-connect pin that could have been used to program CAS latency. (*Id.*). There were a number of presentations made at JEDEC that proposed using no-connect pins for other functions. (*Id.* 1378).

2196. In Release 9 of JEDEC Standard No. 21-C, forty-four out of forty-seven pinouts for SDRAM and DDR SDRAMs have no-connect pins that are available to use for a function like determining CAS latency. (CX0234 at 80-142). Because the vref pin is hardly ever used, it could be available as a no-connect. (Lee, Tr. 11035). Counting the vref pin, forty-four out of forty-seven pinouts for SDRSAMS and DDR SDRAMs have two or more no-connect pins available. (Lee, Tr. 11037; CX0234 at 80-81 83, 85, 86, 87, 88-89, 90, 99, 100, 102, 104, 105, 106, 107-09, 110,121-22, 124-125, 127-28, 130, 131, 132-33, 134-35, 142).

2197. Even if there were no available no-connect pins, JEDEC would not necessarily

have to add new pins in order to implement the dedicated pin alternative. (Lee, Tr. 11031-32). Before the standard was adopted, there was some flexibility with respect to assigning functions to pins, and a pin could have been reassigned to set CAS latency. (Kellogg, Tr. 5123-26).

2198. To avoid adding a new pin, JEDEC could have asserted a super voltage on an existing pin to set the CAS latency if there were no available no-connect pins. (Lee, Tr. 11032). Manufacturers know how to use super voltages today because they use them in test mode. (*Id.*).

2199. Another way to avoid adding a pin to determine CAS latency would be to multiplex existing pins or use a single pin for two functions. (Polzin, Tr. 4026 (“Q. And if there were no available pins on the DRAM, you’d have to add pins to the package; right? A. Or multiplex existing pins.”)).

2200. JEDEC could have multiplexed column address pins to determine CAS latency. (Kellogg, Tr. 5125-26 (In discussing options to determine burst length and other functions, Kellogg testified: “My first preference in that time period would be to use column address pins or pins that were not used during the column address portion of the read or write operation.”)).

2201. JEDEC’s SDRAM and DDR SDRAM standard multiplexes a column address pin, A10. (CX0234 at 147, 151; Kellogg, Tr. 5125). Address pin, A10, can either be used to identify a column address or tell the DRAM to perform an autoprecharge function. (*Id.*).

2202. (Macri, Tr. 4765-77, in *camera*).

2203. JEDEC could have used a DC pin that was dedicated only to determining the CAS latency of a part. (Kellogg, Tr. 5126; Jacob, Tr. 5387-88).

2204. There are cost advantages associated with the use of DC pins to implement this alternative. (Jacob, Tr. 5387-88). DC signals are constant signals and would therefore not require complicated receivers. (*Id.*).

2205. DC pins are less expensive than data pins. (Jacob, Tr. 5387-88). Unlike data pins, whose voltage level change rapidly, DC pins carry a constant voltage level. (*Id.*; Kellogg, Tr. 5120). This allows for flexibility in the placement of DC pins in a package. (Jacob, Tr. 5387-88; Kellogg, Tr. 5124-25). DC pins can be placed in the less desirable location in the package so that more desirable locations can be reserved for data pins. (Kellogg, Tr. 5124-45 (In describing his understanding at the time of how a proposal, in 1992, for a dedicated burst length pin could be implemented, Mr. Kellogg testified, “We would select a pin in a region of the package that was not characterized or would not require special consideration from high speed set of attributes. In other words, this is a DC pin, so we’ll place it somewhere out of the

way.”)).

2206. Dr. Soderman assumed that the dedicated pin alternative would require storage like a mode register. (Soderman, Tr. 9360-62)(discussing a serially shifted register that could store a latency value). Dr. Soderman’s testimony is not reliable. CCF 2207-2210.

2207. Assuming that the burst length and burst type of a part were not programmed in a mode register, there is one implementation of the dedicated pin alternative that would entirely eliminate the need for storage. (Kellogg, Tr. 5126). If the DC pin were dedicated exclusively to identifying the CAS latency latency that a part would operate with, then the DC pin could hold the CAS latency value during system operation without a register. (*Id.*). The DC pin itself would essentially function as ‘storage.’ (*Id.*).

2208. Even if JEDEC had chosen not to use a DC pin, it still would not need a register to implement the dedicated pin alternative. (Kellogg, Tr. 5126-27). It could have used a latch, which is not a register, to store the CAS latency value. (*Id.*).

2209. A latch is a storage element that can store a bit of information, either a positive or negative charge. (Kellogg, Tr. 5127). A register, on the other hand, stores a number of bits. (*Id.*). As Mr. Kellogg, from IBM, testified: “My view of a latch versus a register in th[e] [1992] time frame was that a latch typically stored a bit of information, either a plus or minus, whereas a register typically stored a numerous set of bits for an extended period of time.” (*Id.*).

2210. Dr. Soderman did not consider Mark Kellogg’s testimony that the dedicated pin concept would not require a register at all, but instead would only require a latch. (Soderman, Tr. 9450-51 (“I have not read [Kellogg’s testimony], but a latch is just a type of register, so you’re calling it -- you’re changing the name, but it’s the same thing.”)).

2211. Because the dedicated pin alternative would eliminate the mode register and the interface necessary to program it, it would be simpler and therefore cheaper than programming CAS latency with a mode register. (Jacob, Tr. 5388).

2212. Dr. Soderman testified that the dedicated pin alternative would require three pins and possibly four if it were necessary to add three additional pins in order to implement the alternative. (Soderman, Tr. 9362). His testimony is not reliable. (CCFF 2213-2218).

2213. Dr. Soderman’s testimony is based on the assumption that it would be necessary to preserve all of the optional values for CAS latency that currently exist in the mode register. (Soderman, Tr. 9362, 9462-63). Dr. Soderman admits that if the industry had decided that they only wanted two CAS latency values, then it could have done that with only one pin. (Soderman, Tr. 9463).

2214. JEDEC could have decided that they only needed two options for CAS latency. (CCFF 2215-2218).

2215. Although other values have existed, the industry has typically only used CAS latency 2 or 3 for SDRAM. (Rhoden, Tr. 394).

2216. In September 1995, the JC 42.3 Subcommittee began to consider a number of proposals to reduce the number of required CAS latency options for SDRAM. (JX0029 at 8, 64-68). The Subcommittee overwhelmingly voted in favor of eliminating any required CAS latency values other than 2 and 3. (Cf. JX0056 at 114 (showing the original SDRAM mode register as requiring cas latencies 1, 2, and 3) with JX0027 at 8 (showing that the Committee reached a strong consensus in favor of making cas latency of 1, which would leave only cas latency of 2 and 3 as required)).

2217. In January 1996, the JC 42.3 Subcommittee reviewed votes on a survey ballot for SDRAM lite. (JX0029 at 13). A majority of the Subcommittee wanted SDRAM lite to use a CAS latency of 3, but there was no consensus on whether to also needed to include the capability to use a CAS latency of 2. (*Id.*; Lee, Tr. 6630-31).

2218. When JEDEC published Release 9 of Standard 21-C, it had two required CAS latency values for SDRAM and DDR SDRAM. (Lee, Tr. 11006).

(E) Identifying CAS Latency in the Command.

2219. Identifying CAS latency in the command involves including CAS latency information in the command signal that is sent to initiate any operation. (Jacob, Tr. 5389-90).

2220. Identifying CAS latency in the command would require defining a presently unused command set to identify the CAS latency for DRAM operation. (Jacob, Tr. 5389-90).

2221. The truth table for SDRAM and DDR SDRAM contains command sets that are available to create new read commands that identify one or more CAS latencies. (Jacob, Tr. 5390). The five command lines can carry a combination of thirty-two signals; only about twelve combinations of which are currently used. (Jacob, Tr. 5390-91).

2222. In the JEDEC standard for SDRAM and DDR SDRAM, there is a “truth table” which defines all of the combinations of command signals that are currently used for “standard SDRAM operational functions.” (CX0234 at 145; Lee, Tr. 11031-32). There are many combinations of command signals that currently do not define any function in the truth table. (Jacob, Tr. 5391). Instead of adding a new pin, JEDEC could have used one of the currently undefined combinations of command signals in the truth table to define a particular CAS latency. (Lee, Tr. 11032).

2223. Identifying CAS latency in the command might require more complex decoding circuitry for command sets. (Jacob, Tr. 5392). However, the increased complexity of the decode circuitry would not have significant cost implications. (*Id.*). The cost implications of more complex decode circuitry may be balanced out by the removal of the initialization circuitry that was necessary to program CAS latency with a mode register. (*Id.*).

2224. Dr. Soderman testified that identifying CAS latency in the command would require something that looks like a register. (Soderman, Tr. 9365). This testimony is not reliable. (CCFF 2225).

2225. A latch could be used to store the CAS latency value after the command which identified the CAS latency for a system's operation was sent over the command bus. (Jacob, Tr. 5393). A latch is not a register. (Jacob, Tr. 5393; Kellogg, Tr. 5126-27 discussed, *supra*, at CCFF 2207-2209).

2226. Mr. Geilhufe testified that identifying CAS latency in the read command might require an additional pin and possibly two if the package needs to be balanced. (Geilhufe, Tr. 9580). His testimony is contradicted by the weight of the evidence.

2227. Identifying CAS latency in the command only requires defining a new command set and sending over wires to existing pins. (Jacob, Tr. 5389-90). It therefore does not require the addition of a new pin. (*Id.*).

(F) Stay Asynchronous.

2228. The primary difference between asynchronous and synchronous memory is whether or not the system clock directly controls the DRAM or not. (Jacob, Tr. 5394-95). In synchronous memory, the system clock directly controls both the memory controller and the DRAM. (*Id.*). In asynchronous memory, the system clock directly controls the memory controller. The memory controller in turn controls the DRAM by means of the RAS and CAS signals that the memory controllers sends to it over the bus. (*Id.*).

2229. In the early 1990s, JEDEC considered an asynchronous design as an alternative to the SDRAM proposals. (CX0711 at 1 (During a September 22, 1993, JEDEC meeting, Crisp noted that HP, Micron, and Mitsubishi stated that "EDO is the right thing to do [and] that it offers better performance than DRAM at a much lower cost than SDRAM.")).

2230. Burst EDO is an asynchronous memory. (CX2632 at 1). In the 1994-1996 time frame, Micron promoted Burst EDO within JEDEC as an alternative to SDRAM for the PC market. (Williams, 821-22).

2231. For 66 mhz busses, BEDO could have been faster than SDRAM by two clock

cycles for each burst of data. (CX2632 at 5 (figure 2 illustrates the speed advantages of BEDO compared to SDRAM).

2232. In 66 mhz PC main memory applications, BEDO had one less lead-off cycle than SDRAM in all accesses. (CX2632 at 6). This could equate to as much as a 10 to 12 percent performance advantage in favor of BEDO as compared to SDRAM. (*Id.*).

2233. Asynchronous memory could have been improved incrementally just as synchronous memory has been. (*See, e.g., Williams, Tr. 829-30 (testifying that improvements could have been made to increase the performance of BEDO devices)*).

4. Alternatives to Programmable Burst Length.

2234. In the 1991-1996 time frame, there were at least six alternatives to the use of programmable burst length in JEDEC SDRAM and DDR SDRAM. (Jacob, Tr. 5397-98; see DX0078). First, JEDEC could have used a fixed burst length. (*Id.* 5397). Second, it could have used fuses to program the burst length. (*Id.* 5398). Third, it could have used a dedicated pin(s) to determine the burst length. (*Id.*). Fourth, it could have identified the burst length in the read command. (*Id.*). Fifth, JEDEC could have used a burst terminate mechanism to determine burst length. (*Id.*). Sixth, JEDEC could have toggled the CAS pulse in order to determine burst length. (*Id.*).

2235. Five of these alternatives – fixed burst length, use of fuses to set burst length, use of pins to set burst length, burst terminate, and identifying burst length in the command – were proposed for incorporation in the JEDEC SDRAM standard in the 1991-1992 time period. (JX0010 at 71, 74-75; CX0034 at 149; JX0027 at 64-69; Kellogg, Tr. 5102, 5110-11; Rhoden, Tr. 426-434; Sussman, Tr. 1388-89, 1416-17; Lee, Tr. 6625-26).

2236. In the 1991-1992 time period, the costs associated with these alternatives – fixed burst length, use of fuses to set burst length, use of pins to set burst length, and burst terminate – compared to programmable burst length using a mode register were relatively similar. (Kellogg, Tr. 5132 (“Q. And again, in the 1992 time period, when you were doing this analysis, did you consider any of the four options listed on DX-57 to be unsatisfactory from a cost point of view? A. The cost associated with each of those was relatively similar in the large scheme of things, so I would say from a cost standpoint, that was a large factor in our decision.”)).

(A) Fixed Burst Length.

2237. As with fixed CAS latency, a manufacturer could fix the burst length of a part during the design, manufacturing, or packaging phase. (Jacob, Tr. 5398-99).

2238. During the design phase, a manufacture could hardwire a single burst length value

that would drive the burst length circuitry inside of a chip. (Jacob, Tr. 5399; see DX0080).

2239. In 1991-1992, fixing a single burst length in the design phase would have had technical and cost advantages. (Kellogg, Tr. 5117-18). It would have simplified the design and thereby reduced the design cycle time necessary to implement it. (*Id.*). It would have improved the performance of SDRAM by eliminating the propagation delay that occurs when the circuitry necessary to implement programmable burst length is driven. (*Id.*). It would reduce test costs because it would not have been necessary to test a part for its ability to work with different burst length options. (*Id.*).

2240. Assuming that CAS latency and burst type were fixed as well, a fixed burst length could potentially eliminate the mode register. (Jacob, Tr. 5401-02). It could thereby also eliminate the circuitry that is necessary to initialize the mode register. (*Id.*). Because it potentially eliminates circuitry, fixed burst length would result in a smaller and therefore potentially cheaper part than programmable burst length. (*Id.*). Depending on the phase at which burst length was fixed, it could also have reduced test costs. (*Id.*).

2241. If JEDEC had wanted to preserve the flexibility of a part without using a mode register to program burst length, a manufacturer could have hardwired two different burst length values in a chip, each of which could drive the burst length circuitry inside of the chip. (Jacob, Tr. 5399-5400; see DX0081; *see also* Kellogg, Tr. 5118-19). During the manufacturing phase, a metal mask option would have selected one of the hardwired values to drive the burst length circuitry. (*Id.*).

2242. A manufacturer could hardwire a multiplexor inside of a chip with two different burst length values that connected to the burst length circuitry. (Jacob, Tr. 5400-01; see DX0082). In one implementation, one of the burst length values inside of the multiplexor would connect to power and the other would connect to ground. (*Id.*). During the packaging phase, a bonding option would connect the multiplexor to either power or ground and thereby determine what burst length value would drive the burst length circuitry. (*Id.*).

2243. In 1991-1992, JEDEC considered using fixed burst length. Samsung presented an SDRAM proposal that included a fixed burst length of 8. (JX0010 at 71; Rhoden, Tr. 426-27).

2244. In 1995-1996, JEDEC considered an SDRAM lite part. (JX0027 at 64-68). The use of a single fixed burst length was among the features proposed for SDRAM lite. (Lee, Tr. 6626).

2245. In 1995-1996, Micron was in favor of SDRAM lite because it was simpler and faster to design than full-featured SDRAM. (Lee, Tr. 6633).

2246. In 1995-1996, the use of fixed burst length was acceptable from both a technical

and cost perspective. (Lee, Tr. 6633-34; *see also* Kellogg, Tr. 5131-32).

2247. Both Dr. Soderman and Geilhufe assumed that fixed burst length would require multiple parts. (Soderman, Tr. 9369; Geilhufe, Tr. 9595). Mr. Geilhufe testified that fixed burst length would require four parts. (Geilhufe, Tr. 9595). Their testimony is contradicted by the weight of the evidence. (CCFF 2248-2250).

2248. Release 4 of JEDEC Standard 21-C requires only two burst lengths, a burst length of 4 and 8. (JX0056 at 114; Lee, Tr. 11013-14).

2249. Release 4 of JEDEC Standard 21-C contains two optional burst lengths, a burst length of 1 and 2. (JX0056 at 114; Lee, Tr. 11014). Neither has been used in main memory. (Lee, Tr. 11014).

2250. In the 1995-1996 time frame, JEDEC considered adopting an SDRAM lite part. (Lee, Tr. 11017). “The goal of the SDRAM-Lite was to try to end up with one CAS latency and one burst length.” (*Id.* 11007). For SDRAM lite, JEDEC considered the most popular burst length at the time which was a burst length of 4. (Lee, Tr. 11015).

2251. Mr. Geilhufe testified that adopting fixed CAS latency and fixed burst length would require 12 parts for SDRAM and 15 parts for DDR SDRAM per density. (Geilhufe, Tr. 9601). Mr. Geilhufe’s testimony assumes that JEDEC would have needed to standardize three different CAS latencies and four different burst lengths for SDRAM. (*Id.*). It also assumes that JEDEC would have needed to standardize three different CAS latencies and five different burst lengths for DDR SDRAM. (*Id.*). This testimony is contradicted by the weight of the evidence. (Refer to CCFF 2149-2153, 2247-2250, challenging the Mr. Geilhufe’s testimony that fixed CAS latency requires three parts and fixed burst length requires four); *see also* CCFF 2252-2255).

2252. In 1995-1996, JEDEC considered adopting an SDRAM lite part with a single fixed latency and length. (JX0029 at 13; Lee, Tr. 11018-19). If JEDEC had reach agreement on a single fixed latency and length for SDRAM lite, that would have resulted in one part per density. (*Id.*).

2253. At most, JEDEC would have needed to standardize two different CAS latencies for SDRAM and DDR SDRAM. For SDRAM, customers primarily use CAS latencies of 2 and 3. (Lee, Tr. 11004-05). The use of CAS latency of 1 for SDRAM was never widespread. (*Id.*). In Release 9 of JEDEC Standard 21-C, there are only two require CAS latencies. (*Id.* 11006; CX0234 at 150).

2254. At most, JEDEC would have needed to standardize two different burst lengths for SDRAM and DDR SDRAM. Intel-compatible PCs use a burst length of 4. (Polzin, Tr. 3994).

DRAM customers like AMD, however, use a burst length of 8. (*Id.*). Use of burst lengths of 1 and 2, however, have not been widespread. (Lee, Tr. 11014).

2255. If JEDEC had reached agreement on two different CAS latencies and burst lengths, that would have resulted in only four parts per density. (Refer to Geilhufe, Tr. 9601 (explaining his methodology on the number of parts fixed CAS latency and burst length would require)).

2256. Mr. Geilhufe testified that fixed burst latency would involve extra photo tool costs of \$50,000 for each part. (Geilhufe, Tr. 9594). This testimony is contradicted by the weight of the evidence. (*Id.*).

2257. SDRAM Lite, which was a proposal for a fixed burst length part, would not have involved extra photo tool costs. (Lee, Tr. 11016 (“Okay, my understanding is it did not involve extra tool costs. We were only going to provide the one latency, so there was no other mask required.”)).

2258. Even if SDRAM lite would had included two different burst lengths, it still would not necessarily have involved extra photo tool costs. (Lee, Tr. 11017 (“[If] [w]e had two choices[,] [w]e could have implemented this with a fuse, which would therefore require no extra tooling, or if we created a second metal mask, then there would be an extra tool charge.”)).

2259. Mr. Geilhufe testified that fixed burst length parts would require \$100,000 extra in design costs per part. (Geilhufe, Tr. 9594 (“You will find that fixed burst length is identical to fixed CAS latency. It has exactly the same characteristics. So, the \$100,000 is a design effort for each part type.”). Mr. Geilhufe’s testimony is contradicted by the weight of the evidence. (CCFF 2260).

2260. The design costs of SDRAM lite with a fixed burst length would have been less than the design costs for an SDRAM part with programmable burst length. (Lee, Tr. 11018 (“Q. Mr. Lee, what was your understanding in the 1995 to 1996 time frame as to the cost of designing an SDRAM-Lite with fixed burst length as opposed to the cost of designing an otherwise identical SDRAM with programmable burst length? A. Our design effort would have been less for the fixed length part, and therefore, our design costs would have been less.”)).

(B) Blowing Fuses to Set Burst Length.

2261. A manufacturer could hardwire a part with two burst length values. (Jacob, Tr. 5403). Either electrical or laser blown fuses could be used to select the burst length value for a part. (*Id.* 5403-04; DX0084-85).

2262. For example, a manufacturer could use either electrical or laser blown fuses to

connect two different hardwired values for burst length to the burst length circuitry. (Jacob, Tr. 5403; DX0083). The manufacturer would blow one of the fuses to disable the connection. (*Id.*). Thereafter, the burst length circuitry would operate according to the hardwired burst length that was still connected to it. (*Id.*).

2263. Using fuses to set the burst length is potentially cheaper to design, produce, and test than programmable burst length. (Jacob, Tr. 5404-05).

2264. Using fuses to determine burst length would have preserved the degree of flexibility that a manufacturer has today to make one part that serves multiple applications. (Kellogg, Tr. 5131).

2265. In December 1991, JEDEC considered the use of fuses to determine a mode of operation that JEDEC ultimately decided to determine in the mode register. (JX0010 at 71; JX0056 at 114). Samsung proposed to use fuses to determine the burst type of a part. (JX0010 at 71).

2266. In May 1992, JEDEC considered the use of fuses to choose between two different burst lengths, full page and 8, for an SDRAM part. (CX0034 at 149).

2267. Dr. Soderman testified that one of the disadvantages of using fuses to set burst length is that manufacturers would have to distribute a part with a specific burst length. (Soderman, Tr. 9370). The weight of the evidence indicates that this would not have been a significant issue for DRAM manufacturers. CCF 2268.

2268. In 1995-1996, JEDEC considered an SDRAM lite part with a fixed burst length. (JX0029 at 13; Lee, Tr. 6630, 6632). There was substantial support for a fixed burst length of 4. (*Id.*).

2269. Dr. Soderman testified that he would raise the same technical points about the feasibility and reliability of fuses to discredit the use of fuses to set burst length as he raised to discredit the use of fuses to set CAS latency. (Soderman, Tr. 9370-71). The weight of the evidence indicates that manufacturers have used fuses reliably since the early 1990s and continue to use fuses today. (CCFF 2159, 2172-2177).

(C) Using a Dedicated Pin to Set Burst Length.

2270. JEDEC could have dedicated a pin to holding the burst length value during system operation. (Jacob, Tr. 5405).

2271. The findings for using a dedicated pin to set CAS latency are applicable by extension to the use of a dedicated pin to set burst length. (Jacob, Tr. 5405-06 (“Q. Now, when

you were discussing use of a pin, a dedicated pin, to determine CAS latency, I believe you described certain attributes, such as DC power, et cetera. Would those attributes also apply to the pin that you'd have in mind to determine burst length? A. Absolutely. The same -- the same conditions apply.”); Geilhufe, Tr. 9599 (“Q. If we could go then to the next alternative, Burst Length Via Pins, is – is your understanding of how this alternative works similar to your understanding of how you would set CAS latency via pins? A. That is correct.”)).

2272. JEDEC could have used one dedicated pin to set one of two different burst length values. (CCFF 2213, 2291; Lee, Tr. 11025-26). JEDEC could have used a DC pin, which is less expensive than a data pin, to set the burst length. CCFF 2282-2283.

2273. Using a pin to set the burst length is potentially smaller, cheaper to produce, and easier to test than programming the burst length in a mode register. (Jacob, Tr. 5405).

2274. In December 1991, JEDEC considered the use of two dedicated pins to set burst length and burst type. (JX0010 at 74). Mitsubishi proposed an SDRAM that would use two pins, BT and WP, to program the burst length. (*Id.*; Kellogg, Tr. 5102). In its proposal, Mitsubishi provided for two burst length options, a burst length of 4 and 8. (JX0010 at 74).

2275. Before 1996, the use of a pin was viable from both a technical and cost perspective. (Kellogg, Tr. 5131-32).

2276. Both Dr. Soderman and Mr. Geilhufe testified that the dedicated pin alternative would have required the addition of new pins to the DRAM package. (Soderman, Tr. 9371; Geilhufe, Tr. 9599-9600).

2277. The dedicated pin alternative does not necessarily require the addition of new pins. CCFF 2192-2201.

2278. JEDEC could have used a no-connect pin to implement this alternative. CCFF 2193-2196.

2279. If a no-connect pin was not available, JEDEC could have multiplexed a column address pin to implement this alternative. CCFF 2197, 2199-2201.

2280. If a no-connect pin was not available, JEDEC could have asserted a super-voltage level on a pin to define the burst length in order to implement this alternative. CCFF 2198.

2281. This alternative would not necessarily require storage. CCFF 2206-2210.

2282. JEDEC could have dedicated a DC pin exclusively to holding the burst length value during a system’s operation, which would have eliminated the need for storage entirely.

CCFF 2207.

2283. Cost advantages are associated with the use of DC pins to set burst length. CCFF 2205. DC pins are less expensive than data pins. (*Id.*). They can also be placed in the less desirable locations of a chip package. (*Id.*).

2284. Even if JEDEC chose not to dedicate a DC pin exclusively to setting burst length, this alternative would still not require a register. CCFF 2208-2209.

2285. JEDEC could have multiplexed an existing pin, sharing it to set burst length and perform some other function. CCFF 2199-2201, 2208-2209. After the burst length was asserted on that pin, a latch could store the burst length value during system operation. (*Id.*). Although a latch is a type of storage, it is not a register. (*Id.*).

2286. Assuming that CAS latency and burst type are set by some other method than a mode register, this alternative would eliminate the mode register. (Jacob, Tr. 5406). It also eliminates the circuitry required to initialize the mode register. (*Id.*). This would make the part potentially smaller and therefore cheaper. (*Id.*).

2287. If there was both an insufficient number of no-connect pins and JEDEC could not multiplex existing pins to implement the dedicated pin alternative, then adding pin(s) to implement this alternative might add cost. (Jacob, Tr. 5406-07). However, the cost of adding the kind of pin that would have been necessary to implement this alternative would not have been as significant as adding a data pin. (*Id.* (“Q. How significant would the cost increases have been had it been necessary to add an additional pin? A. Not -- as I said before, not as significant as adding a data pin because this would be a signal that would not be changing over -- it would not be changing dynamically, so it would be a DC value, it would be a simpler receiver, the pin could be in an undesirable location on the package, the pad could be in an undesirable location on the DRAM die, and much simpler to add this.”)).

2288. Mr. Geilhufe testified that adding four pins would have been necessary in order to set the burst length via pins. (Geilhufe, Tr. 9599-9600). However, assuming that four pins had already been added to set the CAS latency, Mr. Geilhufe testified that setting burst length would then only require the addition of two more pins. (*Id.*). This testimony is contradicted by the weight of the evidence. (CCFF 2289-2291).

2289. In 1995-1996, JEDEC considered adopting a part that operated with a single burst length of 4. (JX0029 at 13).

2290. JEDEC could have decided that it only needed two options for burst length. (*See* following proposed findings). Intel-compatible PCs use a burst length of 4. (Polzin, Tr. 3994). DRAM customers like AMD, however, use a burst length of 8. (*Id.*). Use of burst lengths of 1

and 2, however, have not been widespread. (Lee, Tr. 11014).

2291. JEDEC would only have needed one pin to support two different burst length options. (Lee, Tr. 11025-26).

2292. Dr. Soderman testified that claim 1 of Rambus patent 6,324,120 (the '120 patent) covers the concept of using pins to determine burst length. (Soderman, Tr. 9371; *see* RX 2099-52 at 31). Dr. Soderman's testimony is contradicted by the weight of the evidence. (CCFF 2293-2295).

2293. Dr. Soderman's testimony regarding the '120 patent is unreliable because Dr. Soderman did not present a proper claims analysis demonstrating that every element of the claim would be satisfied. (Soderman, Tr. 9456-57).

2294. Dr. Soderman did not consult technical dictionaries, treatises or textbooks, or the expert reports in the private litigation to determine the ordinary meaning in the industry of the terms used in the patent. (Soderman, Tr. 9456-57).

2295. Dr. Soderman's own interpretation of the term "operation code" to a portion of a packet signal limits the scope of claim 1 to Rambus's packetized system. (Soderman, Tr. 9456-57).

(D) Identifying Burst Length in the Command.

2296. Identifying burst length in the command involves including burst length information in the command signal to initiate any operation. (Jacob, Tr. 5407). This would be similar to the method of identifying the CAS latency in the read command. (*Id.*).

2297. JEDEC could have used one or more of the available command sets in the truth table to encode the burst length in the read command. (Jacob, Tr. 5408). The effect of implementing this alternative would be to have two or more different read commands, each encoding a different burst length within the command set. (*Id.*).

2298. Assuming that CAS latency and burst type are set by some other means besides a mode register, identifying burst length in the command could potentially eliminate the mode register. (Jacob, Tr. 5408). It would also eliminate the circuitry necessary to initialize the mode register. (*Id.*). This could potentially make this alternative cheaper than programming burst length with a mode register. (*Id.*).

2299. This alternative would require that the circuitry within the chip that decodes command sets recognizes new read commands which identify the burst length. (Jacob, Tr. 5408). This could require more complex decode circuitry than currently exists to implement

programmable burst length with a mode register. (*Id.*). However, the increased complexity in the decode circuitry would not be significant. (*Id.* 5407-08).

2300. Dr. Soderman testified that claim 1 of Rambus patent 6,324,120 covers the concept of identifying burst length in the read command. (Soderman, Tr. 9374; *see* RX 2099-52 at 31). Dr. Soderman's testimony is contradicted by the weight of the evidence. (CCFF 2301-2303).

2301. Dr. Soderman's testimony regarding the '120 patent is unreliable because Dr. Soderman did not present a proper claims analysis demonstrating that every element of the claim would be satisfied. (Soderman, Tr. 9456-57).

2302. Dr. Soderman did not consult technical dictionaries, treatises or textbooks, or the expert reports in the private litigation to determine the ordinary meaning in the industry of the terms used in the patent. (Soderman, Tr. 9456-57).

2303. Dr. Soderman's own interpretation of the term "operation code" to a portion of a packet signal limits the scope of claim 1 to Rambus's packetized system. (Soderman, Tr. 9456-57).

2304. Mr. Geilhufe testified that identifying burst length in the read command might require an additional pin and possibly two if the package needs to be balanced. (Geilhufe, Tr. 9580, 9596). His testimony is contradicted by the weight of the evidence.

2305. Identifying burst length in the command only requires defining a new command set and sending over wires to existing pins. (Jacob, Tr. 5407). It therefore does not require the addition of a new pin. (*Id.*).

(E) Burst Terminate.

2306. JEDEC could support two burst lengths, such as 4 and 8, with the burst terminate command. (Jacob, Tr. 5409-10).

2307. To implement the burst terminate alternative, a manufacturer could design a part to operate with a long burst length (e.g., burst length of 8). (Jacob, Tr. 5409-10). To effect a short burst length, the memory controller could send a read command before the longer burst length was completed. (*Id.*). So, for example, to effect a burst length of 4 in parts that are designed to operate with a burst length of 8, the memory controller would send a read command after the DRAM sent four bits of data onto the bus. (*Id.*). The read command would thereby terminate the burst length of 8. (*Id.*).

2308. JEDEC's SDRAM and DDR SDRAM standards include a burst terminate

command. (CX0234 at 161; JX0056 at 121 (reference to “interrupted bursts”)).

2309. Implementation of the burst terminate command alternative would not require the addition of a pin. (Jacob, Tr. 5410-11).

2310. This burst terminate command alternative could have potentially made the part a simpler to design, test, and manufacture. (Jacob, Tr. 5411-12).

2311. Dr. Soderman testified that a cuing mechanism issue is associated with the burst terminate command. (Soderman, Tr. 9374-75). He testified that the burst terminate causes a wasted cycle when a write interrupts a read, which would degrade performance and cause problems with pipelining. (*Id.* 9374-76).

2312. SDRAMs and DDR SDRAMs are already designed to handle wasted cycles. (Jacob, Tr. 11109-10). A wasted cycle is not a significant problem. (*Id.*). In DDR SDRAM, a wasted cycle already occurs every time a read follows a write or a write follows a read. (*Id.* 11110 (“[F]or example, if you look at current DDR protocols, whenever the bus is being handed off from one driver to another, from one bank to another or from the memory controller to a bank, so currently whenever you have a read followed by a write or a write followed by a read and some reads followed by other reads, you already have wasted cycles. That’s the definition of the DDR protocol. So, [burst terminate] would introduce nothing more than that.”)).

2313. Mr. Geilhufe testified that it might not be possible to use the burst terminate command to effect a burst length of 1. (Geilhufe, Tr. 9598). This testimony is contradicted by the weight of the evidence. (CCFF 2314). Even if Mr. Geilhufe’s testimony were true, it is not clear that it detracts from the viability of the burst terminate command as a technical and commercial alternative. (CCFF 2315).

2314. Release 9 of JEDEC Standard 21-C, which includes the SDRAM and DDR SDRAM standards, provides for a burst terminate command that could effect a burst length of 1. (CX0234 at 161). JEDEC’s SDRAM standards includes burst length of 1 as an optional burst length. (*Id.* at 150). It states that, “If the Burst stop command [also called Burst Terminate] is included in an SDRAM [], the following functionality is required: 1. BST applies to all burst lengths, including the optional full page burst length when included.” (*Id.* at 161).

2315. Burst length of 1 is used infrequently, if at all, in the DRAM market. (Lee, Tr. 11014).

2316. Dr. Soderman testified that DDR II limits the use of burst terminate to terminating a burst length of eight to get a burst length of 4 because of timing difficulties. (Soderman, Tr. 9376-77). Whether or not Dr. Soderman’s testimony is true does not detract from the viability of burst terminate as an alternative to programmable burst length. (CCFF 2317-2318).

2317. Burst lengths of 1 and 2 are used infrequently, if at all, in the DRAM market. (Lee, Tr. 11014).

2318. JEDEC's decision to include a modified version of the burst terminate command in the DDR II standards confirms that the burst terminate command was a viable means of selecting between burst lengths of 4 and 8.

(Macri, Tr. 4774, *in camera*).

(*Id.*, *in camera*).

(*Id.* 4775, *in camera*)

(*Id.* 4774, *in camera*)

(F) Toggle CAS Pulse to Control Data Output.

2319. JEDEC could have toggled the CAS pulse to output data. (Jacob, Tr. 5411-12).

2320. Assuming that CAS latency and burst type were set by others means besides a mode register, toggling CAS to output data would have eliminated the mode register. (Jacob, Tr. 5412). It also would have eliminated the circuitry necessary to initialize the mode register. (*Id.*). This would have made the part "simpler, smaller, easier to test." (*Id.*).

2321. There are no significant disadvantages to using the CAS pulse to control data output as compared to using a programmable mode register to control the burst length. (Jacob, Tr. 5412).

5. Alternatives to Dual Edge Clocking.

2322. In the 1991-1996 time frame, there were at least seven alternatives to dual edged clocking. (Jacob, Tr. 5416-17). JEDEC could have doubled the clock frequency instead of using both edges of the clock to double the data rate. (*Id.* 5416). Second, it could have interleaved on-chip banks. (*Id.*). Third, it could have interleaved banks at the module level. (*Id.*). Fourth, it could have increased the data width of the DRAM chip to double the data rate. (*Id.*). Fifth, it could have increased the data width at the module level. (*Id.*). Sixth, it could

have used simultaneous bidirectional I/O. (*Id.*). Seventh, it could have used toggle mode DRAM. (*Id.*).

2323. In 1990-1991, JEDEC considered using toggle mode DRAM. (CX0314 at 1; CX0315 at 1-3; CX0318 at 1; CX2431 at 1).

2324. In 1996-2000 time frame, JEDEC considered doubling the clock frequency of SDRAM in order to achieve double the data rate. (JX0031 at 64; CX0371 at 3; Lee, Tr. 6710-11; Kellogg, Tr. 5176-77). JEDEC also considered interleaving on-module banks. (CX0150 at 109-117; Kellogg, Tr. 5176-77).

(A) Single Edge Clock with Double Clock Frequency.

2325. Doubling the clock frequency would require keeping the single-edged clocking scheme used in SDRAM but with a faster clock that would output data on the positive edges fast enough to achieve the desired data rate. (Jacob, Tr. 5433 (“[Double the clock frequency] means using a single-edged clocking scheme and simply doubling that clock, at least for read commands, and doubling the data bandwidth as well.”)).

2326. Use of a single edge clock operating at double the frequency of a dual edge clock could be accomplished in various ways. A faster single edge clock could be run throughout the entire system (a faster system clock) or the system clock could run at the same speed throughout the system and then be doubled by means of a clock splitter on the DRAM. (CX0371 at 3).

2327. Use of dual edge clocking involves certain technical difficulties. Dual edged clocking requires something close to a 50% duty cycle. (Jacob, Tr. 5422; Williams, Tr. 836-837; Sussman, Tr. 1371; Lee, Tr. 6802; _____). It also requires relatively symmetric slew rates. (*Id.*). A 50% duty cycle means that the positive edge, or high voltage state of the clock signal, takes up half a clock cycle and the negative edge, or the low voltage signal state, takes the remaining half of the cycle. (Jacob, Tr. 5422; *see* DX0090; Kellogg, Tr. 5181; Williams, Tr. 836; _____). Symmetric slew rates means that it takes as much time to go from a low to a high signal state as it does to go from a high to a low signal state. (Jacob, Tr. 5422).

(Macri, Tr. 4780, *in camera*). It is much easier to design and test a clock circuit that produces an asymmetric clocking scheme than a symmetric clocking scheme. (Jacob, Tr. 5424-45; *see* DX0090).

(Macri, Tr. 4780, *in camera*).

2328. Use of a single edge clock with double the clock frequency would not require either a 50% duty cycle or symmetric slew rates. (Jacob, Tr. 5433; Kellogg, Tr. 5181-82; Williams, Tr. 836-837); _____, *in camera*). It is therefore an easier clocking

scheme to design and test. (*Id.* 5424-25).

2329. High speed clock chips would have been available to implement this alternative. Companies had made standard SDRAMs that could run at 250 mhz. (Wagner, Tr. 3871). By September 2000, 400 mhz clock chips were already available. (CX2769 at 13). Today, NVidia uses a specialized DDR2 SGRAM that operates with a 500 mhz clock chip. (Wagner 3837-38, 3845-46).

2330. What is and is not considered a very high speed signal changes over time. (Kellogg, Tr. 5182). In the 1996-97 time frame, signals that traveled at speeds of greater than or equal to 533 mhz were considered “very high speed signals.” (Kellogg, Tr. 5182-83). Today, signals that are greater than or equal to 2.5 ghz are considered to be very high. (*Id.*).

2331. (Macri, Tr. 4780, *in camera*).

2332. In March 1996, JEDEC considered running a single-edged clock faster in order to double the data rate. (JX0031 at 64; Rhoden, Tr. 542-43). VLSI proposed using higher speed clocks to achieve data rates of up to 300 mhz. (*Id.*).

2333. In July 1997, JEDEC considered two different implementations of a single edge clock. (CX0371 at 3; Lee, Tr. 6710-11). TI made a presentation for two different versions of a single edged data rate clock. (*Id.*). In one version, TI proposed using a high speed clock throughout the entire system. (CX0371 at 3 (refer to the top drawing); Lee, Tr. 6712). It also proposed to use an on-chip clock frequency doubler to double the clock speed of the external clock signal. (CX0371 at 3 (refer to bottom drawing); Lee, Tr. 6712-13).

2334. In 1996-97, using a single edge clock at double the frequency was a viable alternative. (Kelley, Tr. 5184-95; Lee, Tr. 6713 (The TI proposal to use an on-chip clock frequency doubler was technically feasible; TI’s proposal to run a high speed clock throughout the entire system was technically feasible as well but would have required “changes to the bus topology to make it work at the data rates [TI] wanted to make it work at.”)).

2335. In 1996-97, using a single edge clock at double the frequency was acceptable from a cost perspective. (Lee, Tr. 6713-14 (Micron did not view TI’s proposals for doubling the clock frequency as adding additional cost over existing proposals to use both edges of the clock; Both of TI’s proposals represented acceptable alternatives to dual edged clock from a cost perspective.); *see also* Kellogg, Tr. 5185 (using a single edge clock might or might not incur some cost depending on how it was implemented)).

2336. Dr. Soderman testified that doubling the clock frequency would create clock

distribution problems. (Soderman, Tr. 9393). Dr. Soderman testified, further, that operating internal core circuitry twice as fast is difficult. (*Id.* 9394). This testimony is contradicted by the weight of the evidence. (CCFF 2337).

2337. Doubling the clock frequency does not require the internal core circuitry to operate twice as fast. (Jacob, Tr. 11114-15). Dr. Soderman misunderstands the alternative proposed by Professor Jacob. (*Id.*). In a high speed single-edged data rate scheme, nothing inside the DRAM runs any faster than it did before if only the data is designed to run with the higher speed clock. (*Id.*). In the clocking scheme that Dr. Jacob proposed, command and data run off a slower speed system clock while data runs off a clock that runs at double the speed of the system clock. (*Id.* 11115 (“So, nothing runs any faster than it did before if you’re going to compare it to DDR, for example.”)).

2338. When he reviewed TI’s presentation on two different implementations for a high speed single-edged clock, Mr. Lee did not understand there to be any clock distribution problems associated with the proposal. (Lee, Tr. 11039-40).

2339. Dr. Soderman testified that doubling the clock frequency would increase electromagnetic radiation in a way that could run afoul with Federal Communication Commission (“FCC”) guidelines. (Soderman, Tr. 9395). His testimony is contradicted by the weight of the evidence. (CCFF 2340-2341).

2340. Soderman has no experience with FCC guidelines. He is not an expert in the FCC’s regulation of electromagnetic interference. (Soderman, Tr. 9500). He does not have any individual experience in trying to comply with FCC guidelines. (*Id.*).

2341. There are clocks that run very fast today, from 400 mhz up to over 2.5 ghz, that do not appear to run afoul of FCC guidelines. (CX2769 at 13; Kellogg, Tr. 5182).

2342. Mr. Geilhufe testified that doubling the clock frequency would require an on-DIMM PLL/DLL. (Geilhufe, Tr. 9609). He estimated the cost of an on-DIMM PLL/DLL at \$3.80 per unit. (*Id.* 9610). His testimony is contradicted by the weight of the evidence. (CCFF 2343).

2343. Micron uses on-DIMM PLLs for its registered DIMMs to redistribute the clock to all of the DRAMs on the module. (Lee, Tr. 11040-42).

(Lee, Tr. 11179, *in camera*);
see also Goodman, Tr. 6048-49 (a standard PLL generally costs around \$1)).

(B) Interleaving On-chip Banks.

2344. There are two different ways to double the data rate by interleaving on-chip

banks. (Jacob, Tr. 5418-20; *see* DX0089). This alternative assumes that each SDRAM has two internal banks. (*Id.*). One implementation of this alternative would be to send two read commands that are delayed from each other by half a clock cycle; one read command would be directed to bank 1 while the other read command would be directed to bank 2. (*Id.*). Another way to implement this alternative would be to send a clock and a delayed clock where the first clock would control bank 1 and the delayed clock would control bank 2. (*Id.*). Either implementation would result in two bits of data being sent across the bus per clock cycle. (*Id.*).

2345. An advantage to interleaving on-chip banks is that it does not require symmetric duty cycles or slew rates. (Jacob, Tr. 5424-25). It is possible to implement this alternative with asymmetric duty cycles and slew rates. (*Id.*).

2346. There would not have been any significant disadvantages to interleaving on-chip banks to double the data rate. (Jacob, Tr. 5425).

2347. Interleaving on-chip banks would not necessarily require a multiplexor. (Jacob, Tr. 11136-37).

2348. Dr. Soderman testified that efficient implementation of this alternative would still use dual edged clock. (Soderman, Tr. 9386-87). Dr. Soderman testified that this alternative would require three clocks, clock, delayed clock, and a clock to guarantee the duty cycle. (*Id.*). Based on his conclusion that this alternative would require multiple clocks, Dr. Soderman further testified that this would result in “significant overhead” and “increased power assumption.” (*Id.*). This testimony is contradicted by the weight of the evidence. (CCFF 2349).

2349. Dr. Soderman’s testimony assumes that it would be necessary to guarantee a 50% duty cycle to efficiently implement interleaving on-chip banks. (Jacob, Tr. 11117, 11119-20; *see* DX0358). This assumption is contradicted by the weight of the evidence. (CCFF 2327-2328, 2345). If it were necessary to use symmetric clocks to drive banks 1 and 2, then it would look like data is synchronous with the positive and negative edges of each clock. (Jacob, Tr. 11118-19). The clocks driving banks 1 and 2, however, can be asymmetric. (CCFF 2345). The use of asymmetric clocks to implement interleaving on-chip banks means that this alternative would only require the use of the positive edge of each clock and could differ significantly from dual edge clocking. (*Cf.* Jacob, Tr. 11118-20 with Jacob, Tr. 11120-21; *see also* DX0358).

2350. JEDEC would have chosen asymmetric clocks in order to interleave on-chip banks. (Jacob, Tr. 11124 (“Because it’s cheaper, it’s easier to build, it’s just a simpler design.”)).

(C) Interleaving Banks on the Module.

2351. There are multiple DRAM chips on a module. (Jacob, Tr. 5426-27). Groups of DRAM chips can be organized into ranks of memory. (*Id.*). The positive edge of two clocks, clock and delayed clock, would drive the data from each rank of memory on a module in order to double the data rate. (*Id.*).

2352. Interleaving banks on the module in order to double the data rate would have simplified the design of DRAM chips. (Jacob, Tr. 5427).

2353. In 1996-97, JEDEC considered interleaving SDRAM chips on the module in order to double the data rate. (Kellogg, Tr. 5177-78, 5783-86; *see also* CX0150 at 109-117 (Kentron made a proposal to JEDEC to interleave SDRAM chips on the module: “Operate each bank with its individual CLK . . . Provide/Sample data for every rising edge of both CLKs.”)).

2354. This alternative would not have required asymmetric duty cycles or slew rates. (Jacob, Tr. 5428). JEDEC would have chosen asymmetric clocks to implement this alternative. (Jacob, Tr. 11124 (“Because it’s cheaper, it’s easier to build, it’s just a simpler design.”)).

2355. Interleaving banks on the module would slightly increase the complexity of the module. (Jacob, Tr. 5428; Kellogg, Tr. 5185-86 (“That’s relatively low cost, but that would still remain.”)).

(D) Increasing DRAM Width.

2356. JEDEC could have doubled the data rate by doubling the width of the data bus. (Jacob, Tr. 5429). With this alternative, JEDEC would not have had to increase the clock rate in order to increase the data rate and could have still used a single-edged clocking scheme. (*Id.*).

2357. JEDEC would have only had to double the number of data pins on the DRAM in order to implement this alternative and add any necessary power and ground pins. (Jacob, Tr. 5429). It would not have had to add any command or address pins. (*Id.* 5429-30).

2358. Increasing the number of pins on the DRAM in order to double the data rate would have required a far simpler clock circuit than dual edged clocking. (Jacob, Tr. 5430 (“Q. Now, what, if any, would have been the advantages had JEDEC chosen to increase the number of pins per DRAM rather than using a dual-edged clock? A. Again, you could retain the use of the single-edged clocking scheme, which means that you could use a far simpler clock circuit design. It would mean that your signals are transitioning at a slower rate than, for instance, a DDR-type interface, so rather than having a 200-megabit-per-second data pin, now you stick with a 100-megabit-per-second data pin, so the power of the DRAM actually goes down comparatively.”)). Slower clock circuits and pins indicates that this alternative might consume less power than dual edged clocking. (*Id.*). Increasing the number of pins would not have resulted in a significant increase in noise relative to dual edged clocking. (*Id.* 5430-31).

(E) Increase Pins on the Module.

2359. JEDEC could have doubled the data rate by doubling the number of data pins on the memory module. (Jacob, Tr. 5431). With this alternative, JEDEC would not have had to increase the clock rate in order to increase the data rate and could have still used a single-edged clocking scheme. (*Id.*). Further, JEDEC would not have had to increase the number of pins on the DRAM. (*Id.*).

2360. There are advantages to increasing the number of pins on the module in order to double the data rate rather than dual edged clocking. (Jacob, Tr. 5431-32). It would have been a “far cheaper design to build and test.” (*Id.*) Compared to DDR SDRAM, noise and power levels would have been reduced. (*Id.*).

(F) Simultaneous Bidirectional I/O.

2361. Simultaneous bi-directional I/O could have been an alternative to dual edged clocking. (Jacob, Tr. 5435-36). It is a technology that allows reads and writes to be occur simultaneously. (*Id.*). This would allow for more efficient bus utilization, which could improve the performance of the bus. (*Id.*).

2362. Simultaneous bi-directional I/O technology would have increased the data rate “without having to increase the speed of the system, so this would not increase the power consumption of the system. It would not increase the power consumption of the clock or power dissipation of the clock.” (Jacob, Tr. 5436-37).

(G) Toggle Mode DRAM.

2363. JEDEC could have used IBM’s toggle mode to double the data rate. (Jacob, Tr. 5416-17).

2364. Rambus does not consider toggle mode to be the same or similar to dual edged clocking. (Soderman, Tr. 9398; Geilhufe, Tr. 9610). Although Professor Jacob testified that it was an example of dual edged clocking, he included toggle mode DRAM on his list of alternatives to dual edged clocking because of Rambus’s characterization. (Jacob, Tr. 5418; *see* DX0088).

2365. In 1990-1991, JEDEC considered IBM’s toggle mode DRAM multiple times. (CX0314 at 1; CX0315 at 1-3; CX0251 at 1; CX0318 at 1).

6. Alternatives to On-Chip PLL/DLL.

2366. In the 1991-1996 time frame, there were at least seven alternatives to the use of

on-chip DLL in JEDEC SDRAM and DDR SDRAM. (Jacob, Tr. 5444-45; see also DX0094). Jeduc could have decided not to use any method to align the system clock with data. (CCFF 2369, 2372). Second, JEDEC could have used either a PLL or DLL in the memory controller. (*Id.* 5444). Third, it could have put either a PLL or DLL on the module. (*Id.*). Fourth, it could have used a vernier circuits instead of a either a pll or dll circuit. (*Id.*). Fifth, if JEDEC had decided to increase the number of pins in order to increase performance, it could have avoided the use of on-chip DLL circuits. (*Id.*). Sixth, JEDEC could have decided to rely entirely on the DQS strobe and avoided the use of on-chip DLL circuits. (*Id.* 5445). Seventh, JEDEC could have adopted read clocks, which were sometimes referred to as echo clocks, in order to avoid replicating DLL circuits on each DRAM chip. (Lee, Tr. 6664, 6666-67).

2367. In the 1994-1997 time frame, JEDEC considered five of these alternatives to on-chip DLL for incorporation into the JEDEC DDR SDRAM standard. (Kellogg, Tr. 5154-55 (JEDEC considered vernier circuits, DQS strobe, read clocks, and doing nothing at all); JX0031 at 71 (PLL on the controller); JX0036 at 64 (vernier circuits); CX0368 at 4 (rely on DQS strobe); JX0029 at 17 (echo clocks)).

(A) Use No Method of Aligning Data to the System Clock.

2368. In JEDEC DDR SDRAM, on-chip DLL circuits are used to align the data valid window of each DRAM chip with the system clock. (Jacob, Tr. 5438-42; see DX0093; JX0029 at 17; Kellogg, Tr. 5154-55).

2369. In working towards a DDR SDRAM standard, JEDEC considered not doing anything at all with respect to aligning the data with the clock. (Kellogg, Tr. 5155). When it did consider how to align the data with the clock, however, it considered using PLL/DLL circuits as a solution. (JX0029 at 17).

2370. PLLs, or phase locked loops, and DLLs, or delay locked loops, are very similar circuits. (Jacob, Tr. 5443). The primary difference between them is that a PLL contains an oscillator and a DLL does not. (*Id.*).

2371. In January 1996, JEDEC was debating two different objectives for future SDRAM clocking. (JX0029 at 17). JEDEC had been considering the use of PLL/DLL circuits to accomplish the objective of aligning the read data to the system clock. (*Id.*). In 1996, however, Micron questioned the wisdom of replicating PLL/DLL circuits in every DRAM in the system. (JX0029 at 18). Micron recommended shifting the focus of future SDRAM clocking towards ensuring that read data capture occurred during the data valid windows. (*Id.* at 17, 20).

2372. In 1996-1997, JEDEC did not need to perfectly align the data with the system clock for high speed DRAM operation. (Jacob, Tr. 5442-43; Lee, Tr. 6662-63; Kellogg, Tr.

5161).

2373. What was necessary, in 1996-1997, was to design a system that guaranteed that the memory controller would capture data during the data valid window. (Jacob, Tr. 5442-43; Lee, Tr. 6662-63; Kellogg, Tr. 5154-55, 5161).

2374. The problem of guaranteeing high speed data capture stems from the fact that it takes time to propagate signals through a memory system. (Jacob, Tr. 5438-39). There are three kinds of signal propagation delays: outbound, internal, and return. (*Id.*; *see* DX0093). At high rates of speed, it becomes necessary to mitigate the effect of some of the timing uncertainties that result from these propagation delays. (*Id.*). On-chip PLL/DLLs cancel out some of the internal chip delays in a system that can cause the data valid window to vary. (*Id.* 5442-43).

2375. There are five different types of skew that can cause the data valid window to vary: (1) clock skew to DRAMs; (2) on-chip skew (DRAMs); (3) chip-to-chip skew (DRAMs); (4) data path skew after DRAMs; (5) memory configuration skew (minimal populated vs. maximally populated). (JX0029 at 20; Lee, Tr. 6655-61 (explaining each of the five components of skew)).

2376. On-chip PLL/DLL primarily improves the third component of skew, which is the skew between DRAM chips in a system. (Lee, Tr. 6663).

2377. Using an on-chip PLL/DLL is one way to facilitate valid data capture. (Kellogg, Tr. 5154-56).

2378. In January 1996, Micron proposed a new clocking scheme that would use echo clocks to control the variation in data valid windows. (JX0029 at 17, 20). It would not replicate PLL/DLL circuits in every DRAM in the system. (*Id.* 18). Micron would later propose the use of a data strobe, which is slightly different than the echo clock concept, for data capture in DDR SDRAM. (CX0368 at 4; Lee, Tr. 6666-67).

2379. In 1996-1997, JEDEC members considered not using an on-chip DLL and instead relying on the data strobe to ensure valid data capture. A majority of JEDEC members agreed that on-chip DLL could be eliminated if a data strobe were used to capture data. (Lee, Tr. 6682-83). JEDEC could not, however, reach a consensus in favor eliminating on-chip DLL. (*Id.*). A compromise was struck to include both the data strobe and on-chip DLL in the DDR standard in order to allow for those few companies who wanted to use DDR parts in applications that would not rely on a data strobe. (*Id.*).

2380. In 1996-1997, numerous mechanisms were available besides on-chip PLL/DLL to facilitate valid data capture. (Jacob, Tr. 5443; Kellogg, Tr. 5154-55, 5162; *see* DX0059; CX2109 at 67-68 (based on internal discussions at Rambus, Davidow concluded that there were

“many ways to improve performance” without using an on-chip DLL)).

(B) DLL in the Memory Controller.

2381. The memory controller could use a DLL circuit to “make sure that all of the DRAMs are in sync with each other rather than [having] each DRAM do[] [that] on its own.” (Jacob, Tr. 5445).

2382. If the DLL circuit were in the memory controller, it could potentially eliminate outbound, internal chip, and return delays. (Jacob, Tr. 5446).

2383. This alternative would eliminate DLL circuitry in the DRAM. (Jacob, Tr. 5446-47). As a result, the DDR SDRAM would consume less power and have lower test costs. (*Id.*). It would also reduce the die size of the part, which would lower manufacturing costs. (*Id.*).

2384. In March 1996, JEDEC considered the use of a PLL in the memory controller instead of every DRAM chip in the system for future SDRAM. (JX0031 at 71; Rhoden, Tr. 513-514; Lee, Tr. 6691). Samsung proposed taking the PLL circuit off the DRAM chip and place it inside of the memory controller in order to generate a phase-shifted read clock that the memory controller would use to sample data off both of the read clock’s edges. (Lee, Tr. 6691).

(C) DLL on the Module.

2385. DDR SDRAM could have used either a single or multiple DLLs on the module to ensure that each DRAM chip on the module was in sync with the system clock. (Jacob, Tr. 5448). The internal delay could thereby be accounted for. (*Id.*).

2386. This alternative would eliminate DLL circuitry in the DRAM, “thereby reducing its power consumption, reducing its cost, reducing the design time. (Jacob, Tr. 5450).

2387. Mr. Geilhufe testified that it would cost \$3.80 to pay for the DLL circuit necessary to move the DLL onto the module. (Geilhufe, Tr. 9613). This testimony is contradicted by the weight of the evidence. CCF 2388..

2388. Micron uses on-DIMM PLLs for its registered DIMMs to redistribute the clock to all of the DRAMs on the module. (Lee, Tr. 11040-42).

(Lee, Tr. 11179, *in camera*);
see also Goodman, Tr. 6048-49 (a standard PLL generally costs around \$1.00)).

(D) Verniers.

2389. A vernier circuit is a circuit that can introduce a static amount of delay on a signal

in order to reduce timing uncertainties in a memory system. (Jacob, Tr. 5450). JEDEC could have used a vernier circuit in every DRAM in order to eliminate internal chip delays. (*Id.* 5451). If it were necessary to compensate for dynamic changes in skew, the memory controller could have periodically recalibrated each vernier circuit. (*Id.* 5452-43).

2390. On-chip verniers could have potentially eliminated all three types of delays: outbound, internal, and return. (Jacob, Tr. 5451). Vernier circuits would have been easier to design than DLLs. (*Id.*).

2391. In January 1997, JEDEC considered the benefits of vernier circuits to control the problem of skew in high speed DRAMs. (Kellogg, Tr. 5154-55; CX0367 at 3 (“The inclusion of the vernier in the memory for read data timing manipulation is good for all but the simple one memory device system.”)).

2392. In March 1997, JEDEC considered the use of on-chip vernier circuits. (JX0036 at 58, 64). Desi Rhoden, from VLSI, gave a presentation on DDR SDRAM clocking that included a slide showing SLDRAMs with vernier circuits. (*Id.*).

2393. Dr. Soderman testified that vernier circuits were not a viable alternative to on-chip DLLs, in part, because they could not account for temperature and voltage variations on the DRAM. (Soderman, Tr. 9411). He further testified that recalibration of the vernier is not sufficiently precise and consumes bandwidth. (*Id.* 9412). This testimony is contradicted by the weight of the evidence. (CCFF 2394-2399).

2394. Mr. Lee testified that, in the 1996-1997 time frame, he considered verniers to be a viable technical and commercial alternative to on-chip DLLs. (Lee, Tr. 6676-77). Mr. Lee further testified that he understood verniers to have certain advantages compared to on-chip DLL. (*Id.* 6677). For example, verniers did not require the lock time that was necessary to initialize the DLL. (*Id.*). Also, Mr. Lee testified that at the time he did not believe it was necessary to replicate vernier circuits in every DRAM but instead one vernier circuit could be used in the memory controller. (*Id.*). Using a single vernier circuit in the memory controller would have reduced the cost and complexity of DRAM. (*Id.*).

2395. Some IBM systems were using memory busses with vernier circuits instead of DLL circuits. (Kellogg, Tr. 5161-62). For example, the z900 memory card had a vernier circuit. (*Id.*). Mr. Kellogg believed that vernier circuits were the optimal solution to the data capture issue. (Kellogg, Tr. 5168).

2396. In the 1995-1998 time frame, IBM assessed the data capture problem. (Kellogg, Tr. 5157). It looked at all the elements associated with data capture, and concluded that the vernier compensated for the largest portion of those elements. (*Id.*).

2397. IBM promoted the use of vernier circuits at JEDEC meetings. (Kellogg, Tr. 5154-55).

2398. Dr. Soderman relied, in part, on the fact that SLDRAM initially considered using vernier circuits in the controller and every DRAM without use of on-chip DLL, but ultimately decided to add DLL circuits to conclude that on-chip DLLs are necessary. (Soderman, Tr. 9412-14). This testimony is contradicted by the weight of the evidence. (CCFF 2399). Instead, Dr. Soderman's testimony demonstrated a fundamental misunderstanding of the function of vernier circuits and DLLs in the proposed SyncLink architecture.

2399. The SLDRAM Consortium relied on vernier circuits for data capture. (Lee, Tr. 11044). The Consortium did not add DLL circuits to assist in data capture. (*Id.* 11046). Instead, it added DLL circuits to achieve a purpose other than data capture. (*Id.*).

(E) Increase the Number of Pins.

2400. At higher rates of speed, it is necessary to use a mechanism to guarantee that whatever is capturing data captures it during the data valid window. (Jacob, Tr. 5438-39, 5442-43). If JEDEC had chosen to improve performance by increasing the number of data pins, it would not have had to speed up the memory bus at all. (Jacob, Tr. 5454). Because the bus speed would have relatively stayed the same, increasing the number of pins in order to improve performance would not have required on-chip DLLs. (*Id.*).

2401. Increasing the number of pins would have been an alternative to dual edged clocking and on-chip PLL/DLL. (Jacob, Tr. 5454).

2402. Increasing the number of pins would have required less power consumption than dual-edged clocking with on-chip DLL. (Jacob, Tr. 5454). Eliminating the DLL circuit from the DRAM would have simplified DDR SDRAM design and decreased the die size. (*Id.*).

(F) Rely on DQS Strobe.

2403. JEDEC could have relied on the DQS strobe to guarantee valid data capture. (Jacob, Tr. 5456). JEDEC did not need to perfectly align the read data with the system clock. (Jacob, Tr. 5442-43; Lee, Tr. 6662-63; Kellogg, Tr. 5161). In 1997, a majority of JEDEC members agreed that relying on the data strobe (or DQS) would have been sufficient for valid data capture. (Lee, Tr. 6682-83). It was not necessary to also include an on-chip DLL for valid data capture. (*Id.* 6682-83).

2404. The technical advantage of using a DQS strobe to ensure valid data capture is that the DQS strobe experiences the same propagation delays as the data because it travels with the data on the same signal path to/from the memory controller. (Kellogg, Tr. 5158-59). By

experiencing the same signal delays as the data, it will tell the memory controller to capture data during the data valid window. (*Id.*).

2405. In April 1997, Micron proposed an edge-aligned, bi-directional data strobe for DDR SDRAM. (CX0368 at 1). An edge-aligned strobe allowed implementation without DLL. (*Id.* at 4).

2406. In July 1997, Silicon Graphics proposed a unidirectional data strobe for read operations. (CX0370 at 3). Its proposal identified the following as a problem with current DDR SDRAM clocking proposals: “DLLs introduce instability, cut into dram core cycle time.” (*Id.* at 2).

2407. In 1997, SGI had experience implementing Craylink and XTALK. (CX0370 at 2). Both Craylink and XTALK were source synchronous interfaces that could operate at 800 MB/sec. (*Id.*).

2408. In November 1997, Micron advocated eliminating the DLL from several DDR SDRAM clocking ballots. (CX-2713 at 2; Lee, Tr. 6651, 6654).

2409. Dr. Soderman testified that the fact that DDR SDRAM uses both the DQS strobe and DLL shows that it would not have been feasible to rely on the DQS strobe. (Soderman, Tr. 9416). This testimony is contradicted by the weight of the evidence. (CCFF 2410).

2410. JEDEC included the DQS strobe in the DDR SDRAM standard because a majority at JEDEC wanted to use a strobe synchronous with the data in order to ensure valid data capture. (Lee, Tr. 6682). It included on-chip DLL to satisfy a minority of a few companies in JEDEC that did not want to use a scheme that relied on a data strobe. (*Id.* 6682-83). For those few companies, it was necessary to include a mechanism that aligned data with the system clock. (*Id.*).

(G) Read Clocks.

2411. In the 1995-1998 time period, JEDEC considered read clocks as an alternative to using DLL circuits in every DRAM. (Kellogg, Tr. 5159-60; Lee, Tr. 6663-65; JX0029 at 18-19).

2412. In January 1996, Micron proposed a new clocking scheme for future SDRAM that would use an echo clock to control the variation in data valid windows. (JX0029 at 18-19; Lee, Tr. 6655). The proposal recommended the scheme as a way to avoid the replication of PLL/DLL circuits in every DRAM in the system. (*Id.*). An echo clock is a read clock. (Lee, Tr. 6664-65, using the terms “echo clock” and “read clock” interchangeably).

2413. One of the advantages, in the 1995-1998 time frame, of read clocks versus data strobes was that read clocks required a significantly fewer number of pins to implement than data strobes. (Kellogg, Tr. 5160).

2414. Read clocks would not have required the lock time that DLL circuits require and they address more components of skew than on-chip DLLs. (Lee, Tr. 6665). Because read clocks would have eliminated DLL circuits, they would have decreased the cost and power consumption of present day DDR SDRAMs. (*Id.* 6665-66).

7. JEDEC Rules Prohibited Use of Patented Technologies Without a RAND Letter.

2415. If Rambus had disclosed that it had pending patent applications containing claims, or could have amended its pending applications to add claims, that covered the technologies in question and refused or failed to submit a letter promising to license the technologies on reasonable and non-discriminatory (RAND) terms, JEDEC would not have adopted Rambus's technologies into its SDRAM and DDR SDRAM standards. (Kelley, Tr. 2575, 2564-65; Rhoden, Tr. 350; Landgraf, Tr. 1714 ("If we knew in advance that they were not going to comply with the JEDEC patent policy, we would have voted against it.")).

2416. If Rambus had disclosed that it had pending patent applications containing claims, or could have amended its pending applications to add claims, that covered the technologies in question and refused or failed to submit a RAND letter, JEDEC rules would have prohibited it from adopting the technologies in question into the standard. (CCFF 347).

2417. JEDEC would not have knowingly adopted technologies subject to Rambus's patent application without a RAND letter. (Rhoden, Tr.350; Kelley, Tr. 2564-65). The ideal RAND letter would have offered patented technologies on a royalty-free basis. (Kelley, Tr. 2566). The next ideal RAND letter would have offered patented technologies on reasonable and nondiscriminatory terms. (*Id.*). If Rambus failed to submit a RAND letter, JEDEC would not have adopted Rambus's technologies into its SDRAM and DDR SDRAM standards. (Kelley, Tr. 2575, 2564-65; Rhoden, Tr. 350).

2418. Rambus would not have agreed to RAND terms. (CCFF 2419-2432).

2419. Agreeing to RAND terms would have been inconsistent with Rambus's existing business practices. (Diepenbrock, Tr. 6225-26; CX3129 at 488-89 (Vincent, Dep.) ("My best recollection is that standards bodies often said they wanted licenses under a reasonable, nondiscriminatory basis. And my best recollection is that Rambus licenses, that was not the basis for them.")). According to Mr. Diepenbrock, who served as Rambus's in-house patent counsel from 1995-1999, it was not clear to him whether Rambus had ever entered into an agreement that would have been consistent with RAND terms. (Diepenbrock, Tr. 6099, 6228).

2420. When requested to do so, Rambus refused to assure the IEEE that it would license on RAND terms. (CCFF 2421-2426).

2421. On December 13, 1995, Ms. Cheryl Rowden of the IEEE wrote Rambus's President, Mr. Tate, to inquire whether it might have patents that could apply to IEEE draft document P1596.4. (CX0487 at 1). She asked Mr. Tate to inform the IEEE by January 15, 1996, whether or not Rambus had applicable patents and, if so, to "advise whether or not your company will issue a letter of assurance, in accordance with IEEE Standards Patent Policy." (*Id.*). If Mr. Tate did not respond by January 15, 1996, Ms. Rowden informed him that IEEE would have to assume that Rambus had no applicable patents. (*Id.*).

2422. On Rambus's behalf, Lester Vincent prepared draft responses to the IEEE stating explicitly that Rambus would not agree to be bound by the IEEE's licensing terms. (CCFF 2423-2424).

2423. Mr. Vincent prepared a draft dated January 11, 1996 stating that Rambus believed it was "under no obligation to any standards body to license its intellectual property" or "to disclose its intellectual property in order to retain the right to enforce" it. (CX0853 at 1). The draft letter further stated that Rambus "reserves the sole right to decide whether or not to license its intellectual property, and if so, at what rate or rates." *Id.* The draft letter concluded, "Rambus will not . . . issue the letter of assurance that you have requested regarding a non-discriminatory license. Indeed, Rambus is offering no such license. Rambus reserves all rights to enforce its intellectual property on whatever terms Rambus decides." (*Id.* at 2).

2424. Mr. Vincent prepared a draft dated January 15, 1996 stating that Rambus wished to continue to license its technology on terms that are "consistent with Rambus's own business plan and that are not set by any standards body," and that Rambus therefore was "unable" to provide the IEEE with the letter of assurance that the IEEE sought. (CX0856 at 1).

2425. On January 15, 1996, Mr. Anthony Diepenbrock responded to Ms. Rowden of the IEEE. (CX0855). His letter did not promise to license on RAND terms. Rather, Mr. Diepenbrock's letter stated that Rambus would continue to license its technology "in accordance with its existing business practices." (CX0855 at 2).

2426. In a letter dated February 16, 1996, Cheryl Rowden of IEEE thanked Mr. Diepenbrock for making it clear to IEEE in an earlier letter that Rambus would license pertinent patents on reasonable and nondiscriminatory terms. (CX0490 at 1; Diepenbrock, Tr. 6223). Mr. Diepenbrock did not agree with Ms. Rowden's interpretation of his earlier letter to her. (Diepenbrock, Tr. 6223-24). Mr. Diepenbrock sent Ms. Rowden another letter in which he stated that, "Rambus has already licensed its technology and will continue to license its technology in accordance with its existing business practices." (CX0869 at 1; Diepenbrock, Tr. 6623-24).

2427. Rambus's standard license agreement was inconsistent with JEDEC's patent licensing policy because Rambus preserved the right to discriminate between those it would and would not license to. (CX3124 at 235 (Vincent, Dep.) ("Q What was it about the terms of Rambus's standard license agreement that was not consistent or may not be consistent where the JEDEC policy? A I don't really recall the terms of the Rambus license agreement. The one thing, though, would be that -- that would come to me now would be that Rambus would not be under an obligation to license somebody if they didn't want to.)).

2428. In draft versions of its withdrawal letter to JEDEC, Rambus made it clear that it could not comply with JEDEC's patent licensing policy. In developing a withdrawal letter to JEDEC, someone had suggested that Rambus inform JEDEC that it would not agree with the terms of JEDEC's patent licensing policy. (Crisp, Tr. 3384 ("Q. Now, someone had also suggested that Rambus tell JEDEC that Rambus would not agree to the terms of the JEDEC patent licensing policy. Isn't that right? A. Yes, sir, that's correct.))).

2429. In a draft withdrawal letter dated March 20, 1996, Mr. Crisp wrote: "As you are aware, Rambus Inc. is a technology developer with a primary source of revenue coming from licensing patents and collecting royalties from their use. Accordingly, Rambus Inc. cannot agree to the terms of the JEDEC patent policy as it limits our ability to solely control the dissemination and use of our intellectual property." (CX0873 at 1).

2430. In another draft withdrawal letter dated March 20, 1996, Mr. Crisp wrote: "As you are aware, Rambus Inc. is a high speed memory technology developer driving revenue from licensing fees and royalties. Rambus Inc. cannot agree to the terms of the JEDEC patent policy as it limits our ability to conduct business according to our business model." (CX0874 at 1).

2431. In its withdrawal letter to JEDEC, Rambus made it clear that it would license its technology according to its own terms which would not necessarily be consistent with RAND terms. (CX0887 at 1 ("Recently at JEDEC meetings, the subject of Rambus patents had been raised. Rambus plans to continue to license its proprietary technology on terms that are consistent with the business plan of Rambus, and those terms may not be consistent with the terms set by standard setting bodies, including JEDEC.)); CX3129 at 488-89 (Vincent, Dep.)).

2432. Rambus wanted to maintain the right to exclude companies from obtaining licenses to its technology. (CX3129 at 488-89 (Vincent, Dep.) (Rambus "did not necessarily have to license everybody, they could license who they wanted to.))). Further, Rambus wanted the freedom to license on whatever terms the market would bear. (*Id.* ("Q: And on terms that the market would bear? A: Right. On a mutual meeting of the minds in terms of a license.))).

8. JEDEC Likely Would Have Avoided Rambus Patents Even If Rambus Had Promised To License On RAND Terms.

2433. Even if Rambus had promised RAND terms, JEDEC members likely would have adopted alternative technologies. At JEDEC, there have been instances of disclosure where the disclosing company had agreed to RAND terms but JEDEC nevertheless chose to investigate and ultimately work around technologies that would have been patented. (Kellogg, Tr. 5046-48, discussing Cypress disclosure and Kentron disclosures). IBM personally experienced instances of disclosure which were followed by a RAND letter after which JEDEC chose not to pursue IBM's technology. (*Id.* 5049).

2434. Even if Rambus had disclosed its patent claims before 1996 and provided JEDEC with a RAND letter, JEDEC would have had the option to adopt alternatives to the four technologies at issue in this case. (Meyer, Tr. 378-39; Kelley, Tr. 2564-65)

2435. In other instances where JEDEC members suspected a technology under discussion might be covered by Rambus patents, JEDEC did not continue to pursue those technologies for standardization. (CCFF 2436-2440).

2436. In March 1997, NEC proposed a clocking scheme that used a looped-back topology. (Lee, Tr. 6694). The clocking scheme proposed by NEC was different from the one that was ultimately included in the DDR SDRAM standard. (JX0036 at 7; Lee, Tr. 6694).

2437. Some JEDEC members who were knowledgeable at the time about Rambus architectures expressed their concern that Rambus might have intellectual property that covered NEC's proposed clocking scheme. (JX0036 at 7; Rhoden, Tr. 527-28). Terry Lee stated that the bus topology NEC proposed for its clocking scheme looked similar to Rambus's '703 patent. (Lee, Tr.6694-95). Many people during the meeting strongly objected to further consideration of NEC's proposal for a DDR clocking scheme. (*Id.* 6695)("Many other people in the room also objected. There was a variety of comments from quite a few people from the committee who were -- strongly objected to the consideration of this proposal for the standard.").

2438. JEDEC members refused to consider using NEC's proposal "specifically because of the disclosure that had take place by others knowledgeable in the industry." (Rhoden, Tr. 527-28; *see also* Lee, Tr. 6695-96).

2439. In April 1997, Micron presented an alternative to NEC's proposal for a DDR clocking scheme that intentionally did not require the use of looped-back clocks. (CX0368 at 2; Lee, Tr. 6697-98). Micron's proposal noted that, "Loop back strobe could have intellectual property problems." (*Id.* 6699). The latter was a reference to the Rambus patent issues raised during NEC's clocking proposal. (*Id.* 6699). Micron wanted JEDEC to avoid the patent problems associated with NEC's clocking proposal. (*Id.*). Micron proposed using a bidirectional data strobe for reads and writes that did not use a looped-back technology. (CX0368 at 1-4; Lee, Tr. 6698-99).

2440. JEDEC ultimately adopted a bidirectional data strobe that did not use a looped back topology into its DDR SDRAM standard. (CX0234 at 164; Lee, Tr. 6681-82).

B. If Rambus Had Disclosed On A Timely Basis And JEDEC Wanted To Use The Technologies In Its Standards, JEDEC Members Likely Would Have Sought To Negotiate Acceptable Royalty Rates Before Becoming Locked In To Use of the JEDEC Standards.

2441. Even if JEDEC had still decided to adopt the four technologies at issue in this case after disclosure had occurred from Rambus before 1996, JEDEC members likely would have negotiated a lower royalty rate than they are able to negotiate today. (CCFF 2442-2464).

2442. DRAM manufacturers must be concerned about minimizing costs. (Appleton, Tr. 6277; CX2107 at 136 (Oh, Dep.)). The DRAM business is a commodity business which is characterized by a high degree of competition and low profit margins. (Appleton, Tr. 6280-81 (Micron, for example, has always had a policy to reduce costs because the selling price of DRAM can be so volatile.); CX2107 at 136 (Oh, Dep.)).

2443. DRAM customers require DRAM manufacturers to meet their performance requirements for as little cost as possible. (Polzin, Tr. 3960 (AMD “needed to make sure that whatever memory [they] chose in [their] systems for [their] microprocessors was a commodity and met the requirements at the lowest possible cost.”); Williams, Tr. 823-34 (During meetings with customers regarding Burst EDO, “Keeping the cost low of DRAM was the goal.”); CX2777 at 1 (“...the age old rule for DRAMs still apply. Customers will take as much performance as we can give them for absolutely no added cost over the previous technology. They will not pay extra for increased DRAM performance.”); CX1708 at 2 (“Compaq (Dave Wooten) like the others, stressed that price was the major concern for all of their systems. . . . Sun echoed the concerns about low cost. They really hammered on that point.”); Gross, Tr. 2302-03 (HP and Compaq have sometimes adopted memory that did not offer any performance improvement but did reduce costs.)).

2444. DRAM manufacturers and customers will forego a performance benefit in order to achieve lower cost. (CX2777 at 1 (In October 2000, Micron decided to vote against a proposed improvement to DDR II standardization efforts because it “add[ed] too much cost to be a standard feature and would jeopardize the success of DDRII if it were required.”); Sussman, Tr. 1441-42 (Sussman did not recommend RDRAM for PC main memory because it was too expensive even though it offered more performance per pin than SDRAM.); Crisp, Tr. 3008-09 (“Q. You understood that a customer might be willing to leave some performance on the table in order to achieve low cost? A. Yes, sir, that’s correct.”); CX0711 at 34).

2445. JEDEC members aim to keep the cost of implementing the standard for the next generation product as close as possible to the cost of implementing the standard for the previous

generation. (Kelley, Tr. 2476, 2526-27 (“The first requirement of a DRAM is low cost. If you cannot make a DRAM low cost, then you won't be in the business. DRAM low cost was paramount before our eyes [at JEDEC].”); CX0034 at 4; CX0711 at 1; CX2294 at 15);

2446. The pressure to reduce costs also drives the DRAM industry to avoid paying royalties whenever possible. (CCFF 107; Appleton, Tr. 6299 (Over the past ten years, Micron has focused on reducing its royalty expenses in order to further its general policy of reducing costs)).

2447. JEDEC members aim to avoid royalties whenever possible. (CX0838 at 1 (“I think that Samsung is on a path to do anything they can to get out of paying us royalties. . . .”); (CX2107 at 137 (Oh, Dep.) (open architecture was important to Hyundai “[b]ecause it means that it is adopted by JEDEC, and thus it requires no royalty or no fees at all.”); CX2294 at 15 (“Strong Points . . . Open architecture without royalties or fees”); CX0676 (“[Samsung] will think that 2% is high for a commodity (memories)”); CX2726 at 7 (“Why DDR Is Cost Effective No Royalties”)).

2448. Representatives of companies who participate in JEDEC testified that they would not have developed SDRAM and DDR SDRAM had they known there were royalties associated with those devices. (Bechtelsheim, Tr. 5813-14 (Had Mr. Bechtelsheim known that programmable CAS latency and burst length could potentially have royalties associated with them, he would have opposed their inclusion in JEDEC SDRAM standards.); CX2107 at 137 (Oh, Dep.) (Dr. Oh testified that Hyundai would not have developed DDR SDRAM if it had been known to have royalties associated with.)).

2449. When JEDEC members cannot avoid royalties, they seek to negotiate royalty rates down to acceptably low levels. (CCFF 2450-2454).

2450. DRAM manufacturers thought that royalties of 1-2% for technologies used in main memory were unacceptable. (Lee, Tr. 7047-48 (“[Rambus’s demand for royalties of] 2 percent, was larger than anything we'd ever heard of for an interface technology and certainly the largest thing we ever heard of for some sort of fee we'd have to pay to produce main memory.”); Appleton, Tr. 6337-39 (“[W]e thought the [2%] royalty rate was quite high. We thought the NRE package, the nonrecurring engineering charge, was high. To us it looked exorbitant. It was just pretty high cost.”); RX-855 at 1 (“0.1% royalty okay, 1-2% ridiculous); CX0711 at 61 (On March 23, 1995, Richard Crisp wrote: “Farhad . . . says their #1 issue with the Rambus business proposal is the royalty rate. They do not want to be straddled [sic] with 3% royalties.”); Lee, Tr. 6614 (Micron did not take a license with Rambus in 1995 because the cost “combined with the royalty for doing that product was unacceptable.”); CX2078 at 139-42 (JEDEC members considered TI’s offer of a 1% royalty rate on a packaging technology to be unreasonable and therefore rejected TI’s technology as a standard.)).

2451. During negotiations with Rambus over licensing terms and royalty rates for RDRAM, many companies sought better terms. (RX0829 at 1-2 (Micron considered ways to negotiate a lower royalty rate from Rambus in 1997.); CX0913 at 1 (On December 3, 1996, David Mooring wrote: “Steve, Jeff, and I met with more than a dozen IBM DRAM apps... They have all TI’s IP concerns, but worse. . . They asked lots of suspicious questions on our IP, patent pooling, and biz model. . . He assured me that they are seriously considering Rambus. But the IP thing is a real dilemma.”); CX0974 at 1 (On December 1, 1997, Geoff Tate wrote: “On royalty reduction we tried several trial discussions with major dram partners and NONE were willing to trade royalty reductions for CHANGES IN BEHAVIOR: all said give me lower royalty and I’ll be more motivated, but weren’t willing to commit [] to specific commitments...”)).

2452. DRAM manufacturers might have considered a royalty rate of substantially less than 1% for a main memory device to have been acceptable. (RX-855 at 1 (“0.1% royalty okay, 1-2% ridiculous)). Intel sought to persuade Rambus to offer a 0.5% royalty rate to those DRAM partners that produced a sufficient volume of RDRAM. (CX0952 at 2 (“[Intel] want[s] us to have license deals that...have long term reduction of royalty based on volume going to less than ½% for rdrams (at this point I choked/gasped.”)).

2453. DRAM manufacturers were particularly concerned with royalty rates once production reached high volume. (CX0768 at 1 (in order to secure a contract with Samsung, Rambus agreed to a 0% royalty rate five years after the date on which Samsung had shipped the 500,000th unit of RDRAM)).

2454. Intel was concerned that if Rambus did not offer a lower royalty rate, many DRAM companies would spend millions to develop alternative technologies that would have enabled them to avoid paying royalties to Rambus. (CX0952 at 2).

2455. Had Rambus disclosed, companies likely would have negotiated rates for SDRAMs and DDR SDRAMs aggressively at the time they negotiated RDRAM licenses. (CCFF 2456-2457).

2456. In 1994, Samsung had insisted upon rights to use Rambus technology in non-Rambus products as part of any RDRAM license. (CX0768 at 1 (“[W]e had to make some major concessions to win this one.”; Rambus could not sue Samsung “for patent infringement on any non-Rambus memories UNLESS they are intentionally using Rambus Technology to compete with Rambus DRAMs.”)).

2457. In 1995, Hyundai insisted upon an “other use” (or “other DRAMs”) clause in its RDRAM license in response to the possibility that Rambus might have patents relating to SyncLink. (CCFF 1548-50). Hyundai likely would have negotiated more aggressively for lower royalty rates if it had not viewed the “other DRAMs” provision to be “just an insurance

program.” (CX2107 at 99 (Oh, Dep.) (“At the time you entered into this license agreement, did you think that Hyundai would have to pay 2.5 percent royalties for Other DRAMs as specified in paragraph 5.3(a)(ii)? A: This is just an insurance program.”)).

2458. In the mid-1990's, Micron, Infineon, and others would have had the opportunity during the course of negotiations for RDRAM licenses to negotiate aggressively with Rambus for rights to use Rambus technology in SDRAMs and DDR SDRAMs. (CCFF 2459-2464).

2459. In the 1995-1997 time frame, Micron and Rambus had been involved in a series of license negotiations. (Appleton, Tr. 6335-37; Lee, Tr. 6612-15).

2460. In 1997, Rambus and Siemens had been involved in contentious license negotiations. (CX0937 at 2 (On July 11, 1997, Mr. Mooring wrote, “In summary, Siemens’ today is fiercely oppositional. After they sign the contract and we have started to support them, they should become at least neutral.”). On July 23, 1997, Rambus and Siemens entered into an RDRAM license agreement. (CX1617 at 22).

2461. In the mid-1990s, Rambus likely would have considered seriously demands of negotiating partners for “other use” clauses in RDRAM licenses. (Farmwald, Tr. 8324 (“Well, a number of companies had been approaching us all along about nonconforming uses of Rambus, noncompatible uses of Rambus, so I believe we were starting to take it more seriously that that's something that we should consider pretty seriously. Intel was also pushing us pretty hard that they wanted a license to Rambus technology for nonconforming uses and we had to take them very seriously.”)).

2462. During the early and mid-1990's, Rambus was willing to make, and often made, concessions to potential RDRAM partners in order to conclude licensing agreements. (CX0543A at 23 (Draft Business Plan: “Of course the terms are negotiable. Rambus is willing to make concessions for additional commitments on the part of the IC licensee regarding press, or high visibility/high volume logic chips etc.”); CX0711 at 61-62 (Crisp email proposing a DRAM royalty rate for Hyundai “declining to 1.25% after 50 million cum units ship”); CX0782 at 1 (Crisp email: “The issue that was raised by GM Han was that they felt our price was too high. . . I explained to them that they could make us a counter proposal telling us what they would like.”); CX0765 at 1 (Tate email: “[W]e cannot get a samsung deal without something like the IP compromise we gave them. . . . I don't like the compromise but it's what we can get.”)).

2463. Indeed, during the early-to-mid-1990's, when Rambus was facing financial pressures, Rambus even considered the possibility of licensing its technologies for use in SDRAMs for a flat cash payment. (CX0543A at 42 (“There are many potential deals we can do with current and future licensees to generate cash if we had a significant need As a final example, we could approach manufacturers of Sync DRAMs with our patent portfolio and

negotiate for a cash license payment.”); *see also* CX0757 at 1 (“I wonder if we can play a game of getting NEC to belly up some dollars by negotiating an ‘other use’ license and get some bucks out of the deal in license fees and royalties.”)).

2464. During the early and mid-1990's, Rambus likely would have had to accept a significantly lower royalty rate in exchange for JEDEC members knowingly incorporating technologies potentially subject to Rambus patent rights in the JEDEC SDRAM and DDR SDRAM standards. (CX1941 at 1 (Advising JEDEC of patent application . . . would license @ 1% royalty.”)).

2465. Paragraphs 2465 - 2499 are unused.

XII. Industry Participants Are Now “Locked In” to the JEDEC Standards.

2500. The DRAM industry, the industries that make components that work with DRAMs, and those that use DRAMs in their own products, are committed to both the SDRAM (CCFF 2501-505), and DDR SDRAM (CCFF 2506-526) standards. No individual DRAM manufacturer can switch from the current JEDEC standards for SDRAM or DDR SDRAM (CCFF 2527-562). The entire industry could eventually switch through JEDEC, but to do so would be costly and take years (CCFF 2563-584).

A. The Industry Is Already Committed to the JEDEC Standards, and the Presence of the Technologies in Those Standards Is the Cause of Rambus Market Power.

1. The Industry is Committed to the SDRAM Standard.

2501. DRAM manufacturers were developing SDRAM by the mid-1990s. For example, Hyundai began its first SDRAM design in late 1992, and by 1994 had two different design teams working on 16M and 64M SDRAM designs. (CX2107 (Oh, Dep.) at 23, 34-35). Micron began design work on SDRAM by . (Shirley, Tr. 4209-11, *in camera*). Infineon began selling SDRAM in the mid-1990s. (Peisl, Tr. 4384-85). By 1999, SDRAM was nearly 80% of the worldwide DRAM market. (CX2747 at 31; McAfee, Tr. 7226-27; see DX141).

2502. Computer and system companies began committing themselves to SDRAM by 1996. For example, Compaq computer began using SDRAM in 1997. (Gross, Tr. 2275). Hewlett Packard began work on the memory subsystem for the “Superdome” Server in 1996. That server which uses up to 128 CPUs and took over 5 years to design. HP’s Superdome server uses SDRAM. (Krashinsky, Tr. 2778-81).

2503. Changing the memory subsystem, even in 2000, in response to changes to the SDRAM standard would have been “disastrous” for HP. (Krashinsky, Tr. 2782-84).

2504. Companies using SDRAM other than computer and system companies have also committed themselves to SDRAM. For example, approximately 80% of the DRAM used by Cisco for its network switches is currently JEDEC-compliant SDRAM. (Bechtelsheim, Tr. 5861-62).

2505. If the DRAM manufacturers had chosen to redesign SDRAM in response to the Rambus lawsuits, the cost to Cisco alone to adapt to that change would be in the range of \$1 billion. (Bechtelsheim, Tr. 5881-82). It would have taken Cisco at least a year to make the transition to the new DRAM standards once those standards had been established. (Bechtelsheim, Tr. 5884 (“[W]e can only start the work once we know what the specification is.”)).

2. The Industry Is Committed to the DDR SDRAM Standard.

2506. The industry is phasing out SDRAM in favor of DDR. (McAfee, Tr. 11227; Rapp, Tr. 10161; *see*, Gross, Tr. 2275; DX-0219).

2507. Currently, only 20% of the DRAMs that HP buys are SDRAM. (Gross, Tr. 2274). Because SDRAM is phasing out as the dominant standard DRAM, HP procures SDRAM only for mature products. (Gross, Tr. 2275 (“Our newer models incorporate DDR”)).

2508. Today, 80% of the DRAMs purchased by HP are DDR SDRAM. (Gross, Tr. 2274-75). As one of the largest PC manufacturers in the world, HP procures between 12 and 15 percent of the world’s output of DRAM. (Gross, Tr. 2272-75). HP will spend approximately \$3 billion on DRAM in 2003. (Gross, Tr. 2277). Approximately 95 percent of the DRAM purchased by HP is for computers. (Gross, Tr. 2272). However HP also procures DRAM for other products such as printers, cameras and camera accessories. (Gross, Tr. 2273).

2509. DRAM manufacturers and other firms have been preparing to manufacture and use DDR SDRAM since at least 1997. By the end of 1998, 64-megabit DDR SDRAM was available from 8 DRAM suppliers, 128-megabit DDR SDRAM was available from one supplier, and 256-megabit DDR SDRAM was available from 2 DRAM suppliers. (CX0303 at 9).

2510. IBM began design work on its first DDR SDRAM chip in late 1996 or early 1997. (G. Kelley, Tr. 2589). Although the standard was not yet completed, DRAM designers were designing the basic architectures of their DDR SDRAM chips and adding features as information regarding those features became available from JEDEC. (G. Kelley, Tr. 2591).

2511. Micron has been designing DDR SDRAM chips since . (Shirley, Tr. 4209-11, *in camera*). By March of 1998, Micron had already planned production of DDR SDRAM chips for the fourth quarter of 1998. (CX2718 at 26; Lee, Tr. 6721-22). By May of 1999, Micron was ramping production of its first generation 64-megabit DDR SDRAM. (CX2737 at 46). By the time that Rambus began suing the DRAM manufacturers, Micron had already made considerable investments in both SDRAM and DDR SDRAM. (Appleton, Tr. 6386).

2512. Once Micron became committed to the standards it is virtually impossible to change to another standard. Micron would have to incur costs to change from the current standard to a new standard, and changing the standard would require that the DRAM manufacturer’s customer base change from the current standard. (Appleton, Tr. 6386-87, 6399-6400 (“It’s virtually impossible to make that kind of a change after you go through the development and the investment.”)).

2513. Infineon began design of its first DDR SDRAM product in early 1998. (Peisl, Tr. 4377-78). By March of 2000, Infineon was ramping up volume production of its first DDR

product. (Peisl, Tr. 4454).

2514. In 2000, Infineon was not capable of removing the technologies claimed by Rambus from DDR SDRAM. (Peisl, Tr. 4444 (“In 2000, ... it would have been very hard and very costly and I would say near impossible to go back and to implement any changes back in the 2000 time frame.”)).

2515. Hyundai has been designing DDR SDRAM chips since 1997. (CX2107 at 122-123 (Oh, Dep.)). By April of 1999, a Hyundai 64-megabit DDR SDRAM chip had finished successful testing in customer systems. (CX2334 at 22; Tabrizi, Tr. 9211). That chip had engineering samples by November of 1998, and was in mass production by March of 1999. (CX2334 at 20). Design work on Hyundai’s 256-megabit DDR SDRAM product began by August of 1999. (CX2108 at 202 (Oh, Dep.)).

2516. Once customers started to use DDR SDRAMs, it was too late for Hyundai to change its DRAMs to avoid the Rambus patents. (CX2108 at 231-32 (Oh, Dep.) (“[I]t’s impossible, almost impossible.”)).

2517. AMD had made the decision to design its chip-sets for DDR in early 1999. (CX2158 at 2). At that time, AMD could have implemented alternatives to the Rambus claimed technologies. (Polzin, Tr. 4042). However, by the time AMD was approached by Rambus in 2000, AMD was already in the middle of the product launch for its DDR-compatible chipset. (Polzin, Tr. 3989-990 (“[The Rambus patents] were pretty simple things to work around if we had known about them a long time ago, but we were in the middle of ramping up an infrastructure. This was just when we were trying to get ... the first DDR motherboards out the door.... The work arounds that were obvious required some big changes to the device, to the chipsets, to the motherboards, et cetera.... The bottom line is any change when you are trying to do a production ramp is extremely difficult....”)).

2518. By September of 1999, most leading graphics controllers either were supporting or planned to support DDR SDRAM. (CX2747 at 58, 65).

2519. By September 2000, ATI had graphics cards already shipping that included DDR SDRAM. (CX1383 at 49, *in camera* (Macri, Tr. 4756, *in camera*)). Changing its products was not a reasonable possibility. (See, e.g., Macri, Tr. 4767, *in camera* (“[T]he cost to the company in terms of engineering resources would have affected our product plans well into the future, as well as disrupting the current products we were shipping. I mean, it would have been ... very chaotic to our business and the expense would have been huge.”)).

2520. Graphics cards using DDR-compatible graphics processors from graphics chip designer NVidia began to ship in the fall of 1999. NVidia began work on those chips

approximately two years earlier in 1997. (Wagner, Tr. 3840-41). Currently, nearly all graphics cards used with NVidia's processors ship with DDR. (Wagner, Tr. 3844).

2521. By the time Rambus began suing the DRAM manufacturers for the use of the technologies in the JEDEC standards, it was too late for NVidia to remove those technologies from its own products. (Wagner, Tr. 3862-63 ("We were trying to launch products into the market and if the standard was going to change, that meant we had to change our development plan and go change to something new that was yet undefined. For us it's a painful process to go through and not be able to release a product that's basically ready to be released and have to start over again.")).

2522. IBM began development of memory interface units designed to be used in their servers with DDR SDRAM in the third quarter of 1997. (Kellogg, Tr. 5015). IBM began selling the p-Series servers, using DDR SDRAM, in December of 2001. Development on those servers began approximately three years earlier. (Kellogg, Tr. 5014-15). IBM was making inquiries to DRAM manufacturers regarding their 256-megabit DDR SDRAM chips as early as April of 1998. (CX2306), and was stating a preference of using DDR SDRAM in servers to DRAM manufacturers as early as November of 1997. (CX2264 at 2; Tabrizi, Tr. 9159-63).

2523. By August of 1997, a number of firms, including VIA, ALi and AMD were considering the development of DDR-compatible chipsets. (CX2297 at 76; CX2747 at 65). By February of 1998, Hyundai expected chipset support for DDR for main memory in high-end workstations and servers from IBM, HP, DEC, Sun and SGI. Additionally, Hyundai expected chipset support for DDR for main memory in PCs from VIA, AMD, SIS, ALi, and Opti. Hyundai expected chipset support for DDR in graphics memory from S3, Trident, ATI, and Intel's Chips and Technology division. (CX2303 at 19).

2524. HP was expressing interest to DRAM manufacturers in DDR SDRAM for its servers and high end workstations as early as July of 1997. (CX2294 at 11). HP had prototypes of a "four way" server, code-named Everest available in the third quarter of 2000. That product used DDR SDRAM. (Krashinsky, Tr. 2793). Work on that project began at HP prior to 2000. (Krashinsky, Tr. 2817).

2525. In 2000, HP did not support changes to the DDR standard to avoid the Rambus patents due to the costs such changes in the DRAM standard would have imposed on HP. (Krashinsky, Tr. 2794-95 ("[T]here was already a standard ... that was adopted at JEDEC and we were counting on it, and therefore we didn't support any changes again because HP does not want to support changes that will cause a lot of expenses to HP.")).

2526. Approximately 15% of the DRAM used by Cisco for its network switches is currently JEDEC-compliant DDR SDRAM. (Bechtelsheim, Tr. 5861).

B. No Individual DRAM Manufacturer Can Switch from the Rambus Claimed Technologies in Response to a Change in the Price of Those Technologies.

2527. For any individual DRAM manufacturer, changing its DRAM designs and manufacturing the new DRAM design would have been a costly and time consuming process. (CCFF 2528-540). Even if a DRAM manufacturer did attempt to switch, it would not be able to sell the new DRAM to most large DRAM customers unless that DRAM were produced by other DRAM manufacturers as well. (CCFF 2541-549). Finally, even if a number of DRAM manufacturers switched, they would not be able to sell their new DRAMs unless other firms, which manufacture complimentary components, agreed to switch as well. (CCFF 2550-562).

1. Changing the Designs for SDRAM and DDR SDRAM Products Would Be Expensive and Disruptive.

2528. Any attempt to change SDRAM and DDR SDRAM products in 2000 to work around Rambus's patents would have required changes to the product designs, followed by layout, tape out, simulation and verification, the creation of a new mask set, manufacture of initial silicon, validation and qualification, and ramp up to full production. (*See* CCFF 46-65).

2529. Any attempt to change the design of SDRAM and DDR SDRAM products to work around Rambus's patents in 2000 would have involved major expense and delay. (CCFF 66-77, 2530-540).

2530. In addition to the costs of the redesign itself, the additional costs of a revision design can be broken down into three primary types of costs: out-of pocket-costs, inventory costs, and opportunity costs. (Shirley, Tr. 4170).

2531. A revision design involves taking an existing design and changing certain circuitry in that design. A revision design usually occurs only when a DRAM manufacturer has found something fundamentally wrong with a DRAM design project that has already made it to silicon. (Shirley, Tr. 4168).

2532. Out of pocket costs of a revision design involves the actual expenditures that a DRAM manufacturer must make in order to accomplish a revision design, particularly the costs of additional mask sets. (Shirley, Tr. 4170). Revision designs require a new set of masks. (Shirley, Tr. 4264). For Micron, as of the fourth quarter of 2002, the cost of a mask set for a DRAM currently in production is in the range of _____, corresponding to a range of _____ micron process technologies. (Shirley, Tr. 4231-35, *in camera*; see DX40-DX41, *in camera*).

2533. For Micron, as of the fourth quarter of 2002, the total cost of mask sets required to fabricate SDRAM and DDR SDRAM was approximately _____. (Shirley, Tr. 4234-35,

in camera; see DX40-DX41, *in camera*). In mid-2000, Micron had mask sets, including SDRAM mask sets and DDR SDRAM mask sets. The total cost of those mask sets to Micron was approximately . (Shirley, Tr. 4239-40, *in camera*).

2534. The inventory costs of a revision design relates to the DRAMs already produced, or those in process of being produced when the problem that led to the revision design was discovered. As a result, inventory costs include DRAMs that cannot be sold because of the problem, and the magnitude of those costs depend on the quantity of such DRAM. (See Shirley, Tr. 4206-7, *in camera*).

2535. In the fourth quarter of 2002, Micron finished DRAM chips per day, of which approximately were SDRAM and were DDR SDRAM. (Shirley Tr. 4237-39, *in camera*; see DX42, *in camera*). In mid-2000, Micron finished SDRAM chips per day. (Shirley Tr. 4241, *in camera*). It takes between 45 days and 55 days for a DRAM to go through the entire fabrication process, so DRAM manufacturers have between 45 and 55 days worth of “work in progress” inventory at any given time. (Shirley Tr. 4153, 4170). Micron also maintains an average of of inventory on hand at any given time. (Shirley Tr. 4238, *in camera*).

2536. The opportunity costs of a revision design are the delay caused to other projects when a DRAM design team is pulled from their current project to work on the revision design. (Shirley Tr. 4207, *in camera*).

2537. Changing their production in order to introduce DRAMs that wouldn’t infringe Rambus’s patents would have required DRAM manufacturers to dedicate a substantial amount of resources from projects intended to improve their products. (Appleton, Tr. 6399-400, 6402-03 (“All companies have limited resources, and we have to apply those resources to the most productive path that we can. Simply taking those resources and applying them to do a technology that doesn’t provide any additional advantage to the current technology that’s being produced is an enormous cost.”); Appleton, Tr. 6402-403; Heye, Tr. 3811-13)). In one case at Micron, the opportunity costs alone of a revision design were in the neighborhood of (Shirley Tr. 4208-9, *in camera*).

2538. Trying to redesign SDRAM and DDR SDRAM products to work around Rambus’s patents at the same time that other design changes would not have been feasible because of the time required for the design changes and the added complexity of trying to combine a redesign with a shrink or a density change. (CCFF 2539-540).

2539. A DRAM manufacturer normally does not attempt to do two different types of changes at the same time. (Reczek, Tr. 4304-305; CX2108 at 257 (Oh, Dep.) (“We normally don’t [redesign some of the internal circuitry at the time of a shrink] unless . . . [the part] has a big problem, if it does not work, then we do, but normally we don’t do that.”)). For example,

when a DRAM manufacturer does a shrink, it does a shrink on a product that already exists so that there are fewer changes to track. (Becker, Tr. 1157-58 (“[F]or instance, when we went from .24 [micron] to .20 [micron], we did that with the same 64-meg SDRAM. So, we did all of our product learning at 0.24 [micron], we had to do all of our process and technology learning at 0.2 [micron], but we did it with a product we already knew.”); CX2108 at 254 (Oh, Dep.) (when doing a shrink, “You don’t change anything” on the inside of the DRAM, “It has nothing to do with the circuit. No circuit change at all.”), CX2108 at 257 (Oh, Dep.) (Hyundai’s practice was not to modify its design at the time it did a shrink)).

2540. Trying to combine a redesign with a shrink or a change in density adds complexity to the effort because multiple changes makes it difficult to determine what has gone wrong if the DRAM has a defect. (Reczek 4304-4305 (“So, in the case you take two steps at one time, so this might lead to very big problems, and for example, if something is not working, you don’t know whether the technology is not working or the design is not working. So, its very difficult to figure out what’s really going on, what’s really going wrong there.”)).

2. Changes to the SDRAM and DDR SDRAM Standards to Avoid the Rambus Patents Would Lead To Products That Were Not Compatible with the Current Standards or with Other Components.

2541. A DRAM has value only if it is compatible with the other components in the products that include the DRAM. (Peisl, Tr. 4410 (“Interoperability [means] that the DRAM works flawlessly together with all the components in the system. It’s not only one chip that the DRAM is interfacing with but all the other components on the motherboard, ... other components on the modules, for instance, like registers. You have to make sure your part is fully compliant with all the specifications of the other chips.”)).

2542. When Rambus began suing DRAM manufacturers, systems manufactures were concerned that DRAM manufacturers might attempt to change the existing SDRAM and DDR SDRAM standards because new standards might not have been compatible with the systems sold by those system manufacturers. (Heye, Tr. 3733-34 (“So, the concerns around that would have been first, it would have taken time to establish the new standards; depending on what they were, you would have had to change the memory component, the north bridge, possibly both, you would possibly have to change the motherboard. You may possibly have to change the [DIMM], once you’ve made all those changes, you would have to implement them,...”)).

2543. Changing the SDRAM standard now to avoid the Rambus patents would lead to DRAM chips that are incompatible with some systems using the existing DRAM infrastructure. (Jacob, Tr. 5567-74 (“If one were to build a DRAM using one of the alternatives highlighted in red, you would produce a DRAM that’s incompatible with present JEDEC-compliant systems. If one were to use one of the other alternatives that are not highlighted in red, you would produce a part that may or may not be compatible with existing JEDEC-compliant systems, and

it would depend upon the system in question.”); *see also* DX0106-0107).

2544. Changing the DDR SDRAM standard to avoid Rambus’s patents on dual-edged clocking now would lead to DRAM chips that are incompatible with all systems using the existing DRAM infrastructure. (Jacob, Tr. 5574-75 (“[I]n this instance all of the alternatives would produce parts that would be incompatible with JEDEC-compliant systems of today.”); *see*, DX0108). The least disruptive of the alternatives, doubling the clock frequency, would require changes to the system clock and the memory controller. (Jacob, Tr. 5575-76).

2545. Changing the DDR SDRAM standard now to avoid the Rambus patents on on-chip PLL/DLL would lead to DRAM chips that are incompatible with some systems using the existing DRAM infrastructure. (Jacob, Tr. 5576-79 (“So those highlighted in red, alternatives 1, 2, 3 and 4, would produce parts that are incompatible with existing systems, and alternative 5 would produce a part that may or may not be incompatible with existing JEDEC-compliant systems, and it would depend on the system in question.”); *see also* DX0109)

2546. Changing the DDR SDRAM standard now to avoid all of Rambus’s patents on the standard would lead to a DRAM that would not be compatible with any JEDEC-compliant systems. (Jacob, Tr. 5579-80 (“If one were to replace all of the technologies in dispute with one of the alternatives, you would produce a DRAM part that would fail to be compatible with any existing JEDEC-compliant system.”); Heye 3742-43).

3. Because SDRAM and DDR SDRAM Are Commodity Products and Customers Require Multiple Sources, No Individual Manufacturer Can Switch from the Rambus Claimed Technologies.

2547. Individual DRAM manufacturers could not remove the Rambus-claimed technologies from the standards without agreement from their customers. (Appleton, Tr. 6400 (“[t]he product that actually gets consumed in the marketplace is not determined by Micron, its determined by the customer base. The customer has developed product platforms based on these standards,... and until the customer decides that they’re no longer going to buy this product, then Micron really cannot make a change in its product portfolio, and we have to continue just to provide the product that we have been providing for some time.”); Peisl, Tr. 4451-52 (“The impact on the customers on changing of standards are huge.... So the customers’ main concern was of course that standards are not being changed and they’re not deducted any features going out of the standard”); CX2108 (Oh, Dep.) at 232. (“Of course, customers will not change it. I mean, they – it’s – it cost a lot to change the design. You have to – changing means that changing all the usage of customer, I mean, the computers. You have to change the – their customer’s mind. It means – it’s impossible, almost impossible.”); Peisl, Tr. 4449 (“It would be very painful – Infineon couldn’t do anything in changing parameters or changing anything on the standards side because we ... are only a part of the industry...”)).

2548. An individual DRAM manufacturer cannot deviate from the JEDEC standards in order to work around Rambus's patents in part because DRAM customers require multiple sources of commodity DRAM. (CX1075 ("... everyone wants multiple-sourced DRAMs, so to make DELL happy, you need multiple suppliers of DRAMs, modules, connectors, and clock chips"); CX1354 at 5 ("DRAM Industry: commodity business, Customers want multiple sourced, compatible DRAMs."); Williams, Tr. 763 ("for Micron, they make memory products that are used in the industry. Their customers are mainly computer customers who require that they are able to buy products from multiple sources ..."); Gross, Tr. 2307-08).

2549. An individual DRAM manufacturer could not change its SDRAM and DDR SDRAM designs if that would cause the critical parameters of its designs to differ in any way from those of other DRAM manufacturers. (*See* Lee, Tr. 6859 ("[I]n our business, we have to have perfectly substitutable products from other suppliers, so there needs to be multiple sources of the same part."); Peisl, Tr. 4448-49 ("Infineon couldn't do anything on their own in changing parameters or changing anything on the standards side because we were – we wouldn't – we are only a part of the industry . . ."); Polzin, Tr. 3943-44, 3952-53; Appleton, Tr. 6280; Bechtelsheim, Tr. 5788; *see also* CCF 25-28).

4. DRAM must Be Compatible with Other Components and Switching to Alternatives to the Rambus Claimed Technologies Would Require Changes in Other Components to Ensure Compatibility.

2550. Even if a group of manufacturers were able to design and build a new DRAM that avoided Rambus's patents, they would not be able to sell those DRAMs unless they were supported by other components. (CX1075 ("A phone or computer that is almost compatible is one that doesn't work. If people build parts 99% compatible, the systems companies won't buy them"); Polzin, Tr. 3954 ("It gets back to just because you have a DRAM doesn't mean you are able to build a computer. You need a lot of support components around it to make a fully functional computer and its critical that in the commodity market you have multiple suppliers of all these components that all agree on the same specification and build compatible parts.")).

2551. Efforts to transition to a new DRAM standard often encounter a "chicken and egg" problem. (Macri, Tr. 4625-29). Industry acceptance of a new DRAM standard requires the existence of additional compatible components, including particularly memory controllers. Those same considerations dictate that sales of a memory controller depend on the existence of compatible DRAMs. In both cases, unless one is available, the firms making the other will be hesitant to produce their component. (CX2315 at 1 ("It is a chicken and an egg problem..... The vendors won't line up to produce the device unless there are users.... but the users won't consider the part unless the suppliers/infrastructure is in place."); Polzin, Tr. 4012; Macri, Tr. 4619-20).

2552. Changing either the SDRAM standard or the DDR SDRAM standard in 2000 to

avoid Rambus's patents would have required manufacturers of components such as controllers, motherboards and modules to redesign, test and reissue their products. (Peisl, Tr. 4457 ("It would not have affected only us as a DRAM supplier; it would have affected all the other suppliers as well. Motherboards would have to be redesigned, controllers would have to be reissued and BIOS would have to be rewritten. It's all a very costly issue.")).

2553. By 2000, the entire industry had implemented the JEDEC standards to such a degree that it would have been extremely difficult and costly for all industry members to change their respective designs to avoid Rambus's patents. (Peisl, Tr. 4444 ("In 2000, the advancements of the SDR and DDR specifications had already reached a degree that the complete industry, the DRAM industry, motherboard industry, the components industry, the module industry, and the controller industry, has reached – had reached a level of implementation of the JEDEC-related standards that it would have been very hard and very costly and I would say near impossible to go back and to implement any substantial changes back in the 2000 time frame."); *see also* CX1340 at 25 ("Setting a new standard is hard ... Compelling benefits over existing standard ... Critical mass of suppliers and users")).

2554. Customers such as HP would only change the type of DRAM it purchased if the new type of DRAM reduced cost, avoided a perceived customer detriment, or provided an improved performance in some way. (Gross, Tr. 2302 ("I can't think of a significant transition we have made that did not also come with performance improvements.")).

2555. A change to the type of DRAM that HP purchases would typically occur only in response to the emergence of new processors or chipsets that can provide additional features to HP's customers. (Gross, Tr. 2286-87 ("Generally our product development teams in developing the next new product would consider microprocessors and chipsets and the features that they would enable for a customer, and that processor and chipset combination that is decided upon dictates the type of memory that needs to be used in combination.")).

2556. In the longer term, firms such as Intel and AMD dedicate substantial resources to ensuring that DRAM and the other components develop such that compatible components are available when the PC-OEMs are assembling their computers. It can take a number of years and substantial expense to support the development of these components. (MacWilliams, Tr. 4818-19 ("It typically takes two to four years to do something new in the DRAM industry and something similar to do something new in the chipset, depending on the amount of the change. . . . Basically, it is the latency for designs.")).

2557. One of the results of that transition period was that Intel, when it selected RDRAM, believed it needed to choose a technology that could be a standard in the industry for approximately five years. (RX0904 at 7; MacWilliams, Tr. 4802 (" . . . [I]t was important that we pick a technology that would allow some stability and longevity because we were going to ask the industry to go through a major transition in terms of the infrastructure. The connectors,

the boards, the modules would all need to change, and that's not something you can change on a yearly or every-other-year basis....Just the amount of investment to make the changes, to validate the changes are correct, to optimize the results based on the feedback you get from the first designs, will take longer than one year...").

2558. AMD also must ensure that it develops the infrastructure, or what it terms a "virtual system" of components, that would all function together with AMD's processors. (Heye, Tr. 3662-63 ("What we have to do is establish an industry-wide business model with many, many partners, and those partners, based on the business model would go off and design north bridges, BIOSes, motherboards, clock chips, VRMs, ... it's a virtual system.")). It took AMD about two years to develop the infrastructure to support the K-7 microprocessor. (Heye, Tr. 3673).

2559. One of the things that AMD must do in order to establish its infrastructure is to determine what the commodity DRAM will be when their CPU is ready to launch. (Heye, Tr. 3666 ("You always want to make sure you're riding the commodity curve. You don't want to be different from what I call the Intel-based systems.")).

2560. The costs of modifying complementary components after a DRAM standard has been adopted by the industry are substantial. For example, the costs to the manufacturers of chipsets if the DRAM standard is changed late in the process can be high, because chipset manufacturers must design a chipset to interface with a specific memory product up to two years prior to the shipment of the chipset. (Heye, Tr. 3678:13 ("from the time you start thinking about a chipset to implementing it, especially when it's brand new like the one for AMD, it's about two years prior to shipping.")).

2561. AMD developed a faster front side bus and a new chipset so that its K7 (or Athlon) CPU would be compatible with a number of different speed SDRAMs and DDR SDRAMs. (Polzin, Tr. 3998- 4005, *see* DX0031). A number of AMD's infrastructure partners also had to make investments to accommodate those faster systems. (Polzin, Tr. 4049-50 ("Our chipset partners needed to design faster circuitry in their chipsets and our motherboard partners needed to adhere to stricter design rules in their manufacture of their motherboards.")).

2562. AMD's chipset partners supported AMD's moves to faster front side busses in order to be able to get better prices for their products. (Polzin, Tr. 4050 ("Why they manufacture our chipsets for the faster front-side buses? That's the question? They want to keep up with the latest technology. They can get higher prices for more advanced chipsets. A chipset that supports DDR 333, for example is worth more than a chipset that supports DDR200.")).

C. The Entire Industry, Including Manufacturers of Complementary Products, Can Only Switch from the Current JEDEC Standard by Changing the JEDEC Standard.

1. It Is Unlikely That a Standard Can Be Created Outside of JEDEC, Which Is the Body That Has Traditionally Determined Standards in the DRAM Industry.

2563. Each new generation of commodity DRAM, from page mode through fast page mode, EDO, SDRAM and DDR SDRAM, has been a JEDEC standard. (Prince, Tr. 9020-21). The DRAM industry's penchant for standardization was well known to Rambus executives from the company's earliest days. (CX0533 at 9 ("The DRAM industry's penchant for standardization combined with the RamBus marketing strategy of licensing all the major vendors make it extremely unlikely that any potential competitor would be able to gain critical mass enough to challenge an already established and ubiquitous RamBus chip.")).

2. Changing the Prevailing DRAM Standard So That Individual Firms Could Switch from the Rambus Claimed Technologies Would Take Years.

2564. It typically takes two to four years to do something new in the DRAM industry. (MacWilliams, Tr. 4818 ("It typically takes two to four years to do something new in the DRAM industry and something similar to do something new in the chipset, depending on the amount of the change."); CX0711 at 184 (changes to a new technology standard, when they occur, require "fundamentally long lead time efforts," because of "the sort of things that must be done . . . to make . . . technology usable from a deployment perspective (silicon infrastructure, models, modules, etc."))).

2565. The standard setting process alone can take two to three years. (CX0302 at 22 ("DRAM subsystem standardization. Complete process may take 2-3 years")). Generally, it is the engineering time to solve the problems that takes up most of that time. (Rhoden, Tr. 414 ("[W]hat we've done is we've removed the process itself from the bottleneck, and now the bottleneck is actually the engineering itself.")).

2566. JEDEC began considering the SDRAM standard in 1991. The 42.3 committee completed work and it became a standard in 1993. The SDRAM standard only began to become widely adopted in the industry in 1996-97. (CCFF 577; *see*, DX0141).

2567. JEDEC began considering the technologies that became part of the DDR SDRAM standard at the same time it was developing the SDRAM standard as part of its consideration of what technologies should be in that standard. (CCFF 578-584). The 42.3 committee completed work and DDR SDRAM became a standard in 1999. (CCFF 649-652). Although DDR

SDRAM was already being used in 1999 by graphics card manufacturers, the DDR SDRAM standard only began to become widely adopted in the industry in 2001-2002. (CCFF 2520; McAfee, Tr. 11344; *see*, DX0141).

2568. JEDEC began considering the DDR-2 SDRAM standard in April of 1998 when the first meeting of the “Future DRAM Task Group” met. (CX0376A; CX0379A; Macri, Tr. 4582-83; Lee, Tr. 6769). The DDR-2 standard has only recently been completed and has been adopted by firms in the graphics card industry. Graphics chip designers were among the earliest adopters of DDR-2. NVidia was working on designs for a graphics chip intended for use with DRAMs based on the DDR-2 standard in late 2000 to early 2001. (Wagner, Tr. 3838-839). ATI uses both GDDR-2 and GDDR-2m in current products. (Macri, Tr. 4579). GDDR-2m, like GDDR-2 is a variant of the DDR-2 standard. (Macri, Tr. 4577-78).

2569. When transitioning to a new DRAM standard, the industry prefers evolutionary rather than revolutionary change, changing as little as possible between standards to obtain the needed performance increase for the new standard. (*See* CCFF 127-128).

2570. Because evolutionary change reduces risk during the introduction of the new standard it also eases the introduction of the new DRAM standard. (MacWilliams, Tr. 4823 (“The problem with revolutionary technologies is they're risky. They take a lot of work to get right and time. You have to go through multiple iterations typically.”); CCFF 127-128, 3246-250).

2571. The SDRAM standard was an evolutionary change from the previous standard, EDO. (MacWilliams, Tr. 4822 (“So SDRAM was perceived to be somewhat evolutionary in that it preserved the same pins as the old EDO memory but added the clock.”); Sussman, Tr. 1377).

2572. The DDR SDRAM standard was an evolutionary change from SDRAM, . (Rhoden, Tr. 408; Sussman, Tr. 1428; Peisl, Tr. 4378-79, 4429; MacWilliams, Tr. 4822 (“DDR is perceived to be evolutionary in that it added some strobes for the data bus but preserved most of the paradigms of SDRAM”), 4882; Gross, Tr. 2291).

2573. The DDR-2 SDRAM standard was an evolutionary change from DDR SDRAM. (Macri, 4611 (“Well, we wanted to -- we didn't want to start with a clean sheet of paper. We wanted to evolve a current DRAM so we could take that user base and move them as seamlessly as possible into the future. So, we needed to pick the DRAM we would start with and then evolve it.”); Rhoden, Tr. 408; Kellogg, Tr. 5190 (“DDR-II is what became the name of the evolutionary memory device that followed DDR, or DDR-I as it became known.”)).

3. Even if JEDEC Were Able to Change the Standard, There Is No Guarantee That the New Standard Would Be Able to Displace the Current Standard.

2574. DRAM manufacturers fabrication plants cost over a billion dollars. (CCFF 31). In addition, the inventory of a DRAM manufacturer can be worth hundreds of millions of dollars. (CCFF 2534-535). As a consequence, DRAM manufacturers that lose to Rambus would have the incentive to agree to license the technologies from Rambus in order to be able to continue to manufacture DRAM. (McAfee, Tr. 7443-44 (“This goes back to the basic economics of the DRAM industry, which is you want – the plants are enormously expensive and you want to run them full out, that is, 24/7, as they say, ... you want to run them full out constantly, and so until you’ve actually ramped up production, you’ll be producing the infringing product and paying royalty.”)).

2575. DRAM customers are only willing to switch from an existing standard or generation of commodity memory to a new standard when cost or performance justifications exist. (Gross, Tr. 2302-303 (“I can’t think of a significant transition we have made that did not also come with performance improvements.”)). Suppliers of components that constitute the DRAM infrastructure are willing to develop products compatible with a new standard only if they are able to obtain an economic benefit from that change. (See CCFF 2562).

4. Reaching Consensus Within JEDEC As To How To Change The Standards Would Be Extremely Difficult.

2576. Because of the amount of work involved and the number of different types of firms at JEDEC, it can take years to change a standard. (CX0302 at 22 (“Complete process may take 2-3 years”); Polzin, Tr. 3977 (“JEDEC is open to any and all parties, so any and all parties have an opinion and can contribute or delay, or everybody has a vote, so it's not always the most straightforward thing to get a technical specification through. It's sometimes long, laborious, and you have to argue your points endlessly, probably much like Congress down the road, but it's successful and it works.”); Peisl, Tr. 4453 (“JEDEC is traditionally a very slowly moving consortium, and there's a reason for that, because there's so many companies involved, it's basically the whole industry that produces parts for the PC and the laptop and the server business, so to try to reach consensus at JEDEC, based on my experience, have been incredibly hard and tough. In the last decade, essentially there were only two standards that emerged for SDR and DDR”); Soderman, Tr. 9511 (“It takes time to have a good engineering standard developed, yes.”)).

2577. The amount of time it takes develop to a new standard to work around the Rambus patents is one of the reasons for the JEDEC patent disclosure rule. (CX0449 at 3 (“The reason for requiring early disclosure is to give the formulating committee as much time as possible to decide whether to include the patented technology in the standard, to work around

the patented technology, or to evaluate other options. Developing a standard can take months or years.”); Williams, Tr. 772-73 (“nine months from the time that you introduced an item to the earliest time that it typically could be sent to ballot and voted on.”)).

2578. The amount of time it takes JEDEC to complete a standard is the main reason that JEDEC starts standards years before the standards are expected to be needed in the marketplace. (Sussman, Tr. 1402; Macri, Tr. 4607-608) (Regarding DDR-2, “[t]he design cycle was long, so we needed to do this very early so that systems could be started to be designed – DRAMs could be designed such that when the DDR1 standard,... ended its life, the DDR2 standard and its systems would be ready to take over in a seamless fashion...[W]e needed to be proactive purely because you can’t build these things in a day. It takes quite a bit of time.”)).

2579. Changing the JEDEC standard by removing the allegedly infringing technologies would have been particularly difficult. (Peisl, Tr. 4451 (“Any change, particularly any deduction of standard, if you -- it's very hard to change the rules in the middle of the game. When you have offered certain options, certain features set to the customers, we have no control which customer is using which feature.”)).

2580. One example how a change in the standard to remove the allegedly infringing technologies would harm the industry is the potential replacement of programmable burst length with fixed burst length. (Peisl, Tr. 4452 (“Removing of features, for instance, as the flexibility of choosing the burst length. As we know, that, for instance, AMD and Intel-based controllers are using different burst length, so removing one would disadvantage one of the companies, which would ... create a noncompetitive situation.”)).

2581. Had the industry adopted a fixed burst length of four for the original SDRAM standard, then AMD would have used that burst length. However, since the standard allowed the use of burst lengths of eight, the company optimized their processors to work with a burst length of eight and would now be harmed by a move to a burst length of four. (Polzin Tr. 3994 (“Fixed burst length would have been very, very bad for AMD. AMD designed its microprocessors to have its natural burst length to be 64 bytes, which is eight cycles of data. Knowing that the DRAMs had that capability, we decided to take advantage of that capability for performance reasons. If the work-around was to fix the burst length, the most likely burst length chosen would have been an Intel-compatible burst length or a burst length of four cycles or 32 bytes. That would have been very bad for us. A, it would have required lots of redesign in the memory controllers and also caused us a performance hit.”)).

2582. Another example how a change in the standard to remove the allegedly infringing technologies would harm the industry is the potential replacement of on-chip PLL/DLL and dual-edged clocking with alternatives that would have removed those features from the DDR-2 standard. (CCFF 2583-584).

2583. Removing the DLL from the DDR-2 standard would have led to the problem of requiring that firms that had been either designing DDR-2 SDRAMs, or designing products to be compatible with DDR-2, to redesign their systems. (Macri, Tr. 4649) (“[basically the earliest adopters would have had to go back to the design stage. Clocking is not something they can change in a trivial manner.... So, I mean, it’s not something you want to go change at that point in time. You really need a gun to your head.”)).

2584. Changing the DDR-2 standard to use single-edged clocking rather than dual-edged clocking would have led to the problem of requiring that firms that had been either designing DDR-2 SDRAMs, or designing products to be compatible with DDR-2, to redesign their systems. (Kellogg, Tr. 5201 (The proposal to eliminate dual edged clocking from the DDR-2 standard “was a significant change to the DDR-II data capture structure, and IBM was already moving down the path of designing our first DDR-II memory controller at this time.”); (Macri, Tr. 4649-51); (Wagner, Tr. 3869) (“[They would have,... brought in suggestions to change the technology and we would have said, we already have a standard, we don’t really want to change, or we’re on a development cycle that cannot tolerate the schedule hit.”); Peisl, Tr. 5545-55); (Kellogg, Tr. 5205 (“One [potential impact of Micron’s proposal to eliminate dual-edged clocking from DDR-2 on IBM] is our DDR-I controller or interface chip that also included DDR-II would very likely see measurable schedule delay due to the significance of the changes.”)).

2585. Paragraphs 2585 - 2599 are unused.

XIII. Through its Conduct Rambus Obtained a Monopoly in Several DRAM Technology Markets.

A. Relevant Economic Characteristics of the DRAM Industry.

1. The Basic Economics of the DRAM Industry Tend to Drive the Industry to a Single Standard.

2600. The DRAM industry is characterized by large capital requirements, interoperability requirements, and commodity pricing to price sensitive customers. (CCFF 2602-617).

2601. Because the DRAM industry is characterized by large capital requirements, interoperability requirements, and commodity pricing to price sensitive customers, it tends to be driven to a single dominant commodity standard. (CCFF 2602-617; McAfee, Tr. 11228-229).

2602. The DRAM technologies at issue are used by DRAM manufacturers as well as by the manufacturers of DRAM-related logic like chip sets. (McAfee, Tr. 7183; *see* DX0132).

2603. Manufacturers of DRAMs and controllers sell products incorporating the DRAM technologies at issue to firms like PC-OEMs that sell their products to consumers. (CCFF 11-16; McAfee, Tr. 7183-84; *see* DX0132).

2604. DRAM customers include PC-OEMs, server-OEMs, manufacturers of workstations, printers, routers, and supercomputers. (McAfee, Tr. 7185-86; *see* DX0133). The largest component of DRAM demand is personal computers, which takes in excess of 60% of DRAM demand. (CCFF 25; McAfee, Tr. 7185; *see* DX0133).

2605. In general, the same types of DRAM devices are used in each of the products made by DRAM customers. (*See* CCFF 2507-508; McAfee, Tr. 7186). Some older products still use older DRAM technologies and some performance sensitive products use technologies that are newer than the current dominant technology. (McAfee, Tr. 7186).

2606. The reason the same types of DRAM devices are used in a wide variety of products stems from the basic economics of the DRAM industry. (CCFF 2607-617; McAfee, Tr. 7186-87).

2607. There are large capital requirements to manufacturing DRAMs. (McAfee, Tr. 7187-88; *see* DX0135). The cost of building a DRAM manufacturing facility is in excess of \$1.5 billion. (*See* CCFF 31; McAfee, Tr. 7187-88; *see* DX0135).

2608. Large capital requirements, like those seen in the DRAM industry, leads to

increasing returns to scale in the sense that increasing production leads to reduced cost of production because the large fixed investments can be spread over a larger amount of production. (CCFF 104; McAfee, Tr. 7189).

2609. Increasing returns to scale tends to create a single dominant standard product and makes it difficult to displace an existing standard product because that product will tend to be the lowest cost. (McAfee, Tr. 7472-73).

2610. Interoperability between DRAM chips and other components is important in the DRAM industry. (CCFF 25-28, 2541-542, 2550-562; McAfee, Tr. 7189-90). Interoperability refers to the need for DRAM to work with other components in the system. (CCFF 26; McAfee, Tr. 7190; *see* DX0030).

2611. Interoperability leads to a type of network externality. (McAfee, Tr. 7191). The need for interoperability between DRAM and other components means that as more of a particular type of DRAM is made, more compatible components become available, or become cheaper. The availability of compatible components makes it easier to use that type of DRAM, which increases the production of that type of DRAM. (CCFF 2550-562; McAfee, Tr. 7609-10; 11212-213). This type of network externality is sometimes called “indirect” network effect. (McAfee, Tr. 11212-213).

2612. Network effects have “the effect that, ... the choice of the technology by the marketplace or dominant share of the technology in the marketplace can lead to lock-in and hence confer market power on the technologies incorporated in the standard.” (McAfee, Tr. 11216-217)

2613. DRAM customers are price sensitive. (CCFF 99; McAfee, Tr. 7192-93). Because PC-OEM customers are generally unwilling to pay increases in price for DRAMs with a higher performance, that makes the PC-OEMs generally unwilling to agree to pay higher prices as well. (McAfee, Tr. 7192). Evidence of the sensitivity of PC-OEM customers to changes in DRAM prices is that when DRAM prices fall, PC consumers buy a large amount of DRAM to upgrade their current computers. (McAfee, Tr. 7193).

2614. DRAMs are generally commodities. (CCFF 93-94, 2548-549; McAfee, Tr. 7200-201). Products that are commodities are perfect substitutes for each other. (McAfee, Tr. 7200). DRAM is nearly a perfect commodity in the sense that the standardized DRAM from any manufacturer is supposed to work in any application that can use that standardized DRAM. (CCFF 2548-549; McAfee, Tr. 7201).

2615. It is well understood in the industry that standardized DRAM is a commodity. (CCFF 93-94)

2616. Because DRAM is a commodity DRAM customers are able to buy DRAM from multiple sources. That allows them to achieve price competition and reduce risk. (CCFF 117-118, 2547-549; McAfee, Tr. 7201). Another implication is that final consumers are more likely to be able to upgrade their computers. (McAfee, Tr. 7201).

2617. Additionally “given the value that's placed on the commodity nature of DRAM, the process by which technologies are selected put an emphasis on standards that applies to all companies that are in the marketplace.” (McAfee, Tr. 7202).

2. The Economics of DRAM Production Can Lead to the Dominance of the Industry by a Single Type of Product.

2618. Reducing cost per bit to manufacture DRAM is one of the most important factors relating to the success of a DRAM manufacturer. (CCFF 95-98). DRAM manufacturers reduce costs by various methods, including die shrinks and increasing wafer size. Each of these methods have the effect of encouraging a single product to be the dominant product. (CCFF 2619-2624).

2619. One method that the DRAM industry has of reducing costs is through “die shrinks,” which lead to increased production for a DRAM being produced on a wafer of a given size. Once the die size has been reduced, more DRAM chips can be produced on the wafer. (CCFF 103-106; McAfee, Tr. 7217).

2620. Because of the high fixed costs of doing a die shrink, DRAM manufacturers will apply die shrinks to the highest volume DRAMs, leading those DRAMs to be low cost relative to the other DRAMs on the market, which increases the sales of that DRAM. (CCFF 105-106; McAfee, Tr. 7218).

2621. The current high volume DRAM product is always the first to experience cost reduction efforts by the DRAM manufacturers. (McAfee, Tr. 7217; CCFF 105-106).

2622. The emphasis of the industry to reduce costs in this way encourages a single product to be the dominant product. (McAfee, Tr. 7225).

2623. Another method that the DRAM industry has of reducing costs is through increasing the wafer size. That method also reduces marginal costs by the application of substantial fixed investments. (McAfee, Tr. 7218).

2624. Regarding the implications of increasing wafer size, “...it's the feedback effect that's important from an economist's perspective. That is to say, we apply our cost reduction to our majority product and that has a feedback effect of lowering the cost of that product which then through the marketplace leads that product to even grow even larger as a proportion of the

total demand.” (McAfee, Tr. 7218-19).

3. The Economics of DRAM Demand Tend to Lead to a Single DRAM Standard.

2625. Large DRAM customers require multiple sources for the DRAM that they buy. (CCFF 2626). This has the effect of encouraging a single product to be the dominant standard. (CCFF 2627- 630).

2626. PC-OEMs as well as other large DRAM customers require that the DRAM that they buy have multiple sources. (CCFF 116-118, 2547-549).

2627. Multiple sourcing reduces risk and ensures price competition among DRAM suppliers. (CCFF 116-118; McAfee, Tr. 7220).

2628. The use of multiple sources by PC-OEMs tends to encourage a single product or not very many products to be a dominant standard. (McAfee, Tr. 7225-226).

2629. An implication of the cost sensitivity of the final consumer is that PC-OEMs are also cost sensitive. As a result, DRAM manufacturers are driven to reduce costs. (CCFF 99-100; McAfee, Tr. 7222).

2630. When design, testing and qualification costs are large, firms want to try to use a single or not too many different flavors or varieties of DRAM so that they don't have to go through the whole design, testing and qualification process over and over and over again. This creates more pressure for having a single, dominant flavor of DRAM. (McAfee, Tr. 7223).

4. The Importance of Standards to the DRAM Industry.

2631. Standards are an essential element in the competitive landscape of the DRAM industry because standards facilitate the use of multiple suppliers, interoperability of DRAMs with other components, and the achievement of economies of scale, all of which tends to lower the total cost to the industry of meeting consumer demand. (McAfee, Tr. 7230; CCFF 2632-639).

2632. Because they allow for multiple suppliers, standards are very important for minimizing the total cost of products that use DRAMs. (McAfee, Tr. 7231; CCFF 117).

2633. Because they allow for interoperability, standards are very important for minimizing the total cost of products that use DRAMs. (McAfee, Tr. 7231; CCFF 114-115).

2634. Because they allow for leveraging the costs of the design, standards are very

important for minimizing the total cost of products that use DRAMs. (McAfee, Tr. 7231; CCFF 119, 121).

2635. By setting a common design, an advantage to the marketplace as a whole of standards is that DRAM customers benefit from price competition. (McAfee, Tr. 7231-32; CCFF 116-117).

2636. Formal standardization can reduce costs by allowing for the achievement of economies of scale. (Rapp, Tr. 10055).

2637. Achievement of economies of scale is a benefit of formal standardization in the case of JEDEC's SDRAM standards. (Rapp, Tr. 10055).

2638. Standards in the DRAM industry serve to define the characteristics of the DRAM in such a way that compatible component manufacturers know enough about the DRAM to know how to design their products. (McAfee, Tr. 7234; CCFF 115).

2639. A benefit of formal standardization is that it helps to create a market consensus about which technology to use. (Rapp, Tr. 10054).

5. Economic Factors Influencing the Success of DRAM Standards.

2640. The success of DRAM standards is influenced by a number of factors, including the cost of the standardized DRAM, the use of consensus based standard-setting to arrive at the standard, and the use of evolutionary technologies in the standard rather than revolutionary technologies. (CCFF 2641-649).

2641. One factor important in determining the success of a DRAM standard is its cost compared to the current standard. The way standards tend to succeed each other in the DRAM market is that newer products tend to be higher priced and be used in niche applications that demand higher performance. Over time the cost of production of the new DRAM falls as more of it is produced. Eventually, the industry “tips” toward the newer DRAM as its cost falls in relation to the older DRAM. (McAfee, Tr. 7229-30; CCFF 105-106, 125-126).

2642. The DRAM industry experiences periods where there is a dominant standard and periods where there is a transition between dominant standards. For example, in 1994, fast page mode was at 95 percent market penetration and was the dominant standard. (McAfee, Tr. 11227; *see* DX0141). After that, a transition took place from fast page mode to EDO and then from EDO to SDRAM, and, in the latter part of the relevant time period, another transition from SDRAM to DDR took place. (McAfee, Tr. 11227; *see* DX0141; CCFF 85-89).

2643. Dr. Rapp agrees that the DRAM industry is an industry that one generation after

another has tended in the 1990s to select one standard to the exclusion of others. (Rapp, Tr. 10106).

2644. The DRAM industry experiences a coordination problem regarding the adoption of new DRAM standards. This problem can hinder investment in a developing standard. (McAfee, Tr. 7241-42 (“In making investments in a technology one very much wants to forecast which technology will be successful; that is to say, you don't want to make investments in, say, supporting a product that won't ultimately be used by the market.”)). For example, in the late 1990s, it was unclear whether the DRAM industry would follow SDRAM with DDR SDRAM or with RDRAM. This made it difficult for firms in the industry to forecast and make appropriate investments. (CCFF 115).

2645. By involving more market participants, an open, consensus-based process has the advantage of improving the accuracy of the forecast by more of the potential users of the standard. That improves the chances that the standard will ultimately be successful. (McAfee, Tr. 7241-42; CCFF 120).

2646. One benefit of the fact that there is a diverse group of firms at JEDEC, with diverse interests is that the outcome of the process is more likely to result in a consensus that addresses the needs of the different users of DRAM. (McAfee, Tr. 7251-53; CCFF 120).

2647. Royalties have an influence on the success of standards because they are charges for the use of the standard, and so insofar as the standard requires royalties, it's less likely to be successful. And the higher the royalties, the less likely the standard will be successful, other things equal. (McAfee, Tr. 7243; CCFF 107-109).

2648. Other things equal, an evolutionary approach to DRAM standards will tend to be more successful than a revolutionary approach. (McAfee, Tr. 7245). One reason is that an evolutionary approach has an advantage of reusing knowledge. The implementation costs will tend to be lower. The risks will tend to be lower with an evolutionary approach. (McAfee, Tr. 7245; *see* DX0146; CCFF 127-128).

2649. "Evolutionary" means built on the existing product or existing knowledge base as opposed to a dramatic change from the existing product or knowledge base. "Revolutionary" is a radical departure, a major departure from the existing technologies and products. (McAfee, Tr. 7245-46).

6. JEDEC's Standard Setting Process.

2650. JEDEC is a consensus-based organization. As a result, JEDEC standards will generally be the result of compromise between JEDEC members rather than the best standard in some abstract sense. ((CCFF 2651). Also, because of the need for timely standards in the

DRAM industry, JEDEC “satisfices” in choosing technologies to incorporate into the standard. Because JEDEC satisfices, when it chooses technologies, the standard chosen might not have been the best possible standard. (CCFF 2652-2658).

2651. The outcome of the JEDEC process is a consensus product that strikes a balance between the needs of a diverse set of industry participants. (McAfee, Tr. 7252-53; CCFF 206, 211-213, 242-249, 251, 254).

2652. Completing standards in a timely manner is important to JEDEC. (CCFF 122-124).

2653. The importance of having a standard completed rapidly is more important in this industry than in other industries. (McAfee, Tr. 7253 (“There's been a great deal of technical change, technological change, and as a consequence, time to market is more important here than in, say, the automobile industry.”)).

2654. The result of the need for timely standards is that there is a stronger incentive for timely decisions than there would otherwise be. (McAfee, Tr. 7253-54 (“It tends to put pressure on a fast decision over, say, the perfect decision.”)).

2655. The speed at which the industry moves makes intellectual property more important than it otherwise would be. (McAfee, Tr. 7254-55 (“And I should say the speed at which this industry moves perhaps makes IP more important, again, than in some other industries. Just there's more technological change, more technological advance, in this industry than in many industries.”)).

2656. The term “satisficing” is an economics term that describes the decision-making process of JEDEC in its choices of features and technologies. (McAfee, Tr. 7255). Satisficing refers to the process by which an organization like JEDEC will choose an adequate solution to a problem it faces rather than expending the effort to find the perfect solution. (McAfee, Tr. 7255-56; CCFF 124).

2657. Satisficing behavior is driven, in part, by the need for timely standards. (McAfee, Tr. 7256).

2658. One implication of satisficing behavior is that while the technologies actually chosen may have been thought to solve the problems faced by JEDEC, there is no reason to believe that the standard actually chosen was the best standard. (McAfee, Tr. 7256 (“[I]ts importance in terms of the economic analysis is that this says generally you can't conclude from the very choice of the technology that it was necessarily even the best of the available alternatives. It just means it was in the top set or the top group. It had good qualities.”)).

7. Lock-In and Hold-Up.

2659. A firm can be held up if that firm is better off paying higher prices to use the investments that it is locked in to rather than switching to new investments. Hold-up for the use of a standard can occur if firms become locked in to the technologies in the standard. (CCFF 2660-673).

2660. The hold-up problem arises in general because investments that are specific to another party are vulnerable in renegotiation -- the other party can extract some or all of the value of the investments. The value of specific assets -- those specific to a relationship with another party -- are vulnerable to expropriation by that other party because the assets have low or no value without the other party's participation. (McAfee, Tr. 7258; *see* DX0148).

2661. A specific investment or a specific asset is one that has low or no value unless another party participates or does something. That is, it requires another party to behave in a certain way. (McAfee, Tr. 7259).

2662. Once a specific investment is made, the economic actor that made the investment is locked into that investment if it is more economical to continue to use the investment or the asset than to switch to an alternative. For example, a power plant operator can become locked in to investments that are required to locate its power plant near a particular coal mine. (McAfee, Tr. 7260- 67; *see* DX0149-154).

2663. Hold-up occurs if the other party changes its prices after the firm becomes locked in by its specific investments. For example, a coal mine operator has an incentive to increase the price of its coal to a power plant operator after the power plant operator has sunk investments by locating its power plant near the coal mine to lower transportation costs. (McAfee, Tr. 7260- 67; *see* DX0149-154).

2664. One way that parties avoid the possibility of being held-up is to contract in advance of making investments that would make them vulnerable to hold-up. This is sometimes called "*ex ante*" contracting. For example, a power plant operator could sign a contract with a coal min prior to making investments necessary to locate the power plant near the coal mine. (McAfee, Tr. 7267-68; *see* DX-0153-55).

2665. The assertion of IP rights on a standard after lock-in is a classic case of economic hold-up. After lock-in to the standard occurs, it becomes possible for the owner of a patented technology to hold up the industry and expropriate some portion of the specific investments that have been made into the technology. (McAfee, Tr. 7439).

2666. The nature of the expropriation is the charging of royalties that exceed the *ex ante* value of the technology, and instead, are conditioned on the specific investments that have been

made in reliance on the standard. (McAfee, Tr. 7307).

2667. The risk of hold-up in standard-setting depends on the size of the specific investments made with respect to a particular standard, the cost of changing the standard, and the importance of intellectual property in the industry. (McAfee, Tr. 7270; *see* DX0157).

2668. Specific investments include those investments made by firms to make components that are compatible with the standard. (McAfee, Tr. 7296-97; *see* DX0164).

2669. Firms, in the standard setting context, when hold-up is made possible by the existence of IP, contract for IP in advance of the standard being set. This is a type of *ex ante* contracting. (McAfee, Tr. 7272-73; *see* DX0158).

2670. One method of *ex ante* contracting to avoid hold-up in the standard setting context is a requirement for firms to disclose their IP. (McAfee, Tr. 7273). The disclosure of IP might help the standard-setting organization avoid hold-up by ensuring that if IP was included in the standard, it was done in a conscious and deliberate manner. (McAfee, Tr. 7273).

2671. Another method of *ex ante* contracting to avoid hold-up in the standard setting context is a requirement for firms to make some sort of licensing commitment regarding their IP prior to the inclusion of the implicated technologies in the standard. (McAfee, Tr. 7273-74).

2672. There is more than one type of potential licensing commitment that can be used by standard setting organizations to mitigate the risk of hold-up. (McAfee, Tr. 7274).

2673. One type of licensing is a commitment for a free license. Another type of licensing commitment is for a RAND or “reasonable and nondiscriminatory” license. (McAfee, Tr. 7274). A requirement of a RAND letter will not eliminate the risk of hold-up, but it mitigates or reduces that risk. (McAfee, Tr. 7274).

2674. Dr. Rapp agrees that standard-setting can create market power by making otherwise close substitutes inferior and thereby increasing the royalty rate (price) a technology can command. (Rapp, Tr. 9972).

2675. In settings where compatibility requirements are high, the choice of a standard may virtually eliminate, not merely disadvantage, competing technologies. (Rapp, Tr. 9966-67).

2676. Formal standard setting creates market power whenever the standard-setting body is faced with several more or less equivalent technologies in terms of cost and performance, and the standard-setting body incorporates one of those technologies into a standard. (Rapp, Tr. 9799). The technologies that are not chosen become inferior alternatives. (Rapp, Tr. 9800).

2677. In the context of formal standard setting, the “price of the chosen technology can change after the standard is determined if the technology owner attempts to extract the value added by the standardization process in royalty fees for the standard technology.” (Rapp, Tr. 9973-74).

2678. “In the absence of knowledge about proprietary IP rights in the technologies under consideration, manufacturers may find themselves the victims of opportunism after the standard has been set. That is, the patent holder may charge a royalty that reflects a premium arising from irreversibility, the cost of revising the standard to save the cost of royalty. A patent holder may charge such a premium when the patent emerges after manufacturers have made sunk investment in the patented feature of the standard without have predetermined the license fee. Avoiding a license entails new investment cost if the old (potentially infringing) investments cannot be modified to evade the patents.” (Rapp, Tr. 9975-76).

2679. “Once the patented technology is adopted as a standard,... firms may commit to the standard and invest in complementary assets needed to make and produce the newly standardized products.... *Ex post*, the cost of switching to the patented alternative may now be much greater as the industry is ‘locked-in’ to the patented standard.” (Teece, Tr. 10509-10).

2680. Once firms have committed to a standard and have made the requisite investment in complementary assets to manufacture and sell the standardized product, switching to an alternative may be much less feasible for three reasons. The first reason relates to the presence of sunk costs. The second reason relates to the need for compatibility, especially backwards compatibility, with the existing installed product base. The third reason is that there is often a significant coordination problem in getting all interested parties to switch to an alternative. Coordinating the necessary changes may make it impracticable to switch away from the patented standard. (Teece, Tr. 10489-92; *see* DX0355).

2681. “The asymmetry between the low *ex ante* cost of choosing an alternative proposed standard and the higher *ex post* cost of abandoning an existing standard in favor of a new standard causes concerns about the prospect for ‘lock-in.’” (Teece, Tr. 10500-501). For purposes of analyzing the issues in this case, *ex post* means the time period after a standard is adopted. (Teece, Tr. 10490).

8. Lock-in and Hold-up Concerns in the DRAM Industry.

2682. DRAM industry standards are characterized by hold-up. Both the rules of JEDEC and the characteristics of production in the DRAM industry illustrate the lock-in and hold-up concerns in the industry. (CCFF 2683-2756).

2683. If JEDEC has a preference to avoid patents, that can be seen as an expression of an interest on the part of JEDEC to avoid the hold-up problem. (McAfee, Tr. 7277).

2684. JEDEC has a strong preference to avoid the presence of patented technologies in the JEDEC standards. (CCFF 301-304).

2685. If JEDEC has a preference for early disclosure that would also be an expression of an interest in avoiding hold-up because, as an economic matter, the earlier information is obtained, the better decisions will tend to be. (McAfee, Tr. 7277, 7301-04).

2686. JEDEC has a strong preference for early disclosure of patents or patent applications in the standardization process. (CCFF 339-345).

2687. In the absence of a search requirement, one way of minimizing the potential for hold-up would be a good faith requirement to provide as much information as a member has access to, and to not try to change the outcome of the process by manipulating it. (McAfee, Tr. 7278).

2688. There is a good faith requirement at JEDEC. (CCFF 310-314).

2689. A requirement of a standard setting organization that firms disclose patent applications as well as patents is consistent with an interest in avoiding hold-up. (McAfee, Tr. 7278-79).

2690. JEDEC has a requirement that firms disclose patent applications as well as patents relating to the standard-setting work under discussion. (CCFF 318-320).

2691. Dr. Rapp agrees that "for [lock-in] to be a concern, the proprietary technology must be essential to the standard or else it could simply be omitted.... [a]n attempt by the patent owner to charge opportunistic royalties would result in manufacturers leaving that particular technology out of the final product." (Rapp, Tr. 9980-981; *see* DX0323).

2692. Dr. Rapp agrees another condition for opportunism to be a concern would be that the costs of changing the standard or manufacturing process must exceed the royalty demanded for the use of the standard. (Rapp, Tr. 9982; *see* DX0323).

2693. Dr. Rapp agrees another condition that he believes must be met or must be satisfied for opportunism to be a concern is that there must be alternatives to the chosen patented technology that could plausibly have been adopted had disclosure taken place. (Rapp, Tr. 9982-983; *see* DX0323).

2694. Dr. Rapp agrees that to determine whether these three propositions apply in a real-world example would require a careful assessment of the relevant facts. (Rapp, Tr. 9984; *see* DX0323).

2695. Dr. Rapp reviewed no Rambus business records other than Toshiba license agreement and a license term synopsis prepared by his staff. (Rapp, Tr. 9991; *see* DX0324).

2696. Dr. Rapp reviewed no third-party business records. (Rapp, Tr. 9992; *see* DX0324).

2697. Dr. Rapp reviewed no deposition testimony. (Rapp, Tr. 9993; *see* DX0324).

2698. Dr. Rapp reviewed no JEDEC materials/minutes other than two technical specifications. (Rapp, Tr. 9994; *see* DX0324).

2699. Dr. Rapp reviewed no notes/reports on JEDEC activities. (Rapp, Tr. 9995; *see* DX0324).

2700. Dr. Rapp reviewed none of the Rambus / JEDEC / third-party records cited in McAfee's report. (Rapp, Tr. 9999; *see* DX0324).

2701. Dr. Rapp agrees that "[t]he reliability of any example of economic reasoning depends, in part, on the quality of its underlying assumptions. All assumptions are not equal. Reasoning which rests on baseless assumptions is less reliable than reasoning based on assumptions that are well-founded in facts and evidentiary materials." (Rapp, Tr. 10004 ("Not only do I agree with it, I think they are words to live by."); *see* DX0325).

2702. Dr. Rapp agrees that it is important for an economist to try to ensure that his or her assumptions and conclusions are well-founded in evidentiary materials. (Rapp, Tr. 10007 ("And may I just add that that refers to the connection between the foundations for assumptions and the specific subject matter that the economist is addressing, not the universe of subject matter.")).

2703. Hold-up may be a concern in the DRAM industry if the following circumstances are true: The amount of specific investments into the standard are substantial, the costs of changing standards is high, IP is important in the industry, and it is difficult to reach agreements to change the standard once set. (McAfee, Tr. 7407; *see* DX-0160).

2704. The ease of reaching agreement reflects on how difficult it would be to avoid hold-up by changing the standard and can be seen as a cost of changing the standard. (McAfee, Tr. 7411).

2705. Based on the evaluation of those factors, hold-up is a problem that arises in the context of the DRAM industry. (McAfee, Tr. 7288; CCF 2710-756).

2706. There is substantial potential for lock-in in the DRAM industry, and, as a result,

there is potential for the creation of monopoly power by incorporating technologies into DRAM standards. (McAfee, Tr. 11304; CCF 2710-756).

2707. Lock-in is a major feature in the DRAM industry, and, as a consequence, the bargaining power of a licensor of proprietary technology that is in the standard grows over time and it becomes ever more difficult for the industry to get out from under patented technology. (McAfee, Tr. 11370).

2708. Incorporation of a technology in JEDEC standards is highly likely to lead to dominance of that technology in the marketplace. (McAfee, Tr. 11224).

2709. The deployment of resources that locks in an industry to a particular standard increases the value of the technology that is incorporated in the standard. (McAfee, Tr. 7438).

(A) Specific Investments Are Substantial.

2710. Hold-up in the context of DRAM standardization occurs when the industry learns that the technology that it chose to incorporate into a standard is subject to a patent, and the industry learns this fact after it has already made substantial specific investments into the standard. (McAfee, Tr. 7305-06).

2711. Those specific investments may take the form of investments in plant and equipment, complementary goods, and other investments that are specific to the technology. (McAfee, Tr. 7306).

2712. A substantial amount of investment in the DRAM industry is specific to the DRAM technology and so is specific to the standard that is at issue. (McAfee, Tr. 7407; CCF 2501-2526, 2528-2540).

2713. In the DRAM context, once a standard is issued and adopted over time, there is an increasing level of investment in the standard by manufacturers producing to the standard, including investment by manufacturers of complementary components such as modules, graphic cards, and chip sets. (McAfee, Tr. 7436; *see* DX0221; CCF 2550-2562).

2714. Such investments by DRAM manufacturers and by manufacturers of complementary components contributes to lock-in. (McAfee, Tr. 7437).

2715. As specific investments in a standard are made, the industry becomes progressively more locked into the standard. (McAfee, Tr. 7435). The switching costs grow over time, and there comes a point when the technology incorporated into the standard obtains monopoly power because the alternatives are no longer commercially viable. (McAfee, Tr. 7435). This phenomenon has occurred in the DRAM industry. (McAfee, Tr. 7435).

2716. Industry-wide coordination and resource commitment is part of the specific investment in the DRAM standards that makes the industry locked in to a DRAM standard over time. (McAfee, Tr. 7436-37; *see* DX0221; CCF 2547-2562).

2717. Because of the scope and the size of the investments into a standard, there is a relatively large amount of lock-in in the DRAM industry to a standard that has been deployed in volume. By the time that DRAM ramp-up occurs, lock-in has been accomplished, particularly because of the specific investments made in goods that are complementary to the standard. (McAfee, Tr. 7444-45 (“Because in order to deploy the standardized product in volume, it requires those complementary goods. Things like chipsets and the like are also being produced.”)).

2718. If compatibility requirements are high, there will typically be a dominant product standard. (McAfee, Tr. 11218).

2719. Compatibility requirements refers to the requirement that a product be compatible with other products that work with them. (McAfee, Tr. 11210-11).

2720. In qualitative terms, compatibility requirements are high in the DRAM industry. (McAfee, Tr. 11211; CCF 25-28, 2550-562).

2721. Parts compatibility refers to a requirement that parts inside a system work with other parts. (McAfee, Tr. 11211). Parts compatibility plus a significant range of complementary products leads to high compatibility requirements. (McAfee, Tr. 11212).

2722. High compatibility requirements have the effect of creating significant lock-in to the existing standards or existing technologies. (McAfee, Tr. 11211) .

2723. In the DRAM industry, high compatibility requirements have led to lock-in and resulting monopoly power in the technologies incorporated into DRAM standards. (McAfee, Tr. 11211).

2724. If the cost of modifying compatible complementary products is substantial so that when the standard is changed, costs would have to be incurred by makers of complementary products to match the new, then significant network effects are present. (McAfee, Tr. 11216).

2725. The long lead times for a number of products means that many manufacturers need to know what the standard will be years in advance. For example, the costs to the manufacturers of chipsets can be high if the DRAM standard is changed late in the process. Workstation and server manufacturers also need to know what the DRAM design will be years prior to shipping their product. (CCF 115).

2726. Coordination costs alone may completely block the switching to a new standard, irrespective of the financial switching costs. (McAfee, Tr. 11300; CCFF 2564-568).

2727. DRAM manufacturers will not switch without their customers' simultaneously willing to purchase, and the customers will not be willing to purchase unless the complementary component suppliers are also providing compatible components. (McAfee, Tr. 11301; CCFF 2547-2562).

2728. Because DRAM manufacturers will not switch without their customers' simultaneously willing to purchase, and the customers will not be willing to purchase unless the complementary component suppliers are also providing compatible components, it is incumbent to have an industry consensus in order for the industry to switch to an alternative standard, *i.e.*, significant coordination must take place. (McAfee, Tr. 11301).

2729. Such coordination is costly and includes costs that goes beyond the direct financial costs of implementing a new standard. (McAfee, Tr. 11303; CCFF 2564-568).

2730. Even if the actual direct financial switching costs are minimal, it may still be difficult or impossible for the DRAM industry to switch from an existing product standard to an alternative product standard. (McAfee, Tr. 11300).

2731. From the standpoint of assessing lock-in in this case, it is necessary to account for the aggregate switching costs of DRAM manufacturers. (Rapp, Tr. 10124). In addition, to switch successfully to an alternative DRAM technology, manufacturers of other complementary products would also have to make costly changes. (Rapp, Tr. 10124-25). Therefore, for the DRAM industry as a whole to work around Rambus's patents, coordination among DRAM manufacturers and manufacturers of other products such as makers of microprocessors and chipsets would have to take place. (Rapp, Tr. 10125).

2732. Depending on the alternative technology chosen, makers of hard drive storage, sockets, modems, memory modules, graphics cards, graphics subsystems, and CDROM/DVD drives might have to change their products to accommodate a new DRAM standard. (Rapp, Tr. 10141-42).

2733. The aggregate costs to non-DRAM makers of working around Rambus's patents could actually be higher than the aggregate costs to DRAM makers. (Rapp, Tr. 10136).

2734. In order to avoid Rambus's patents, the DRAM manufacturers would have to make changes to each of the densities of SDRAM or DDR that they had in production. (Rapp, Tr. 10144).

(B) Costs of Changing Standards Are High.

2735. It is difficult and time consuming for the DRAM industry to reach agreements over changing the DRAM standards. (McAfee, Tr. 7410-11; 2564-568; 2576-584).

2736. Because it is difficult and time consuming for the DRAM industry to reach agreements over changing the DRAM standards there is a high risk of hold-up from patents on DRAM standards. (McAfee, Tr. 7411).

2737. There is a substantial volume of switching costs in the DRAM industry, where switching costs refers to the costs of changing standards. (McAfee, Tr. 7408-409; CCF 2576-584).

2738. The costs of changing the standards today to avoid the Rambus patents includes the cost to: (1) develop new technology standards (McAfee, Tr. 7440); (2) reach consensus after the first standard had been adopted (McAfee, Tr. 7447-52; *see* DX0225); and (3) design, test, and qualify DRAM components and the necessary complements to those DRAM components. (McAfee, Tr. 7453-54). Additional switching costs are the opportunity costs of using resources to change the standard and the cost that delaying the standard can have on the industry. (*See* DX-0223; CCF 2537).

2739. From an economic perspective, coordination problems are rightly considered to be an element of overall switching costs. (Teece, Tr. 10828-29)

2740. Time is a relevant factor in considering lock-in. (Rapp, Tr. 10147).

2741. One of the most important switching costs in the DRAM industry is the cost of delay in the standard to the DRAM industry. (McAfee, Tr. 7440-41; CCF 123-124)

2742. Recent standards have taken at least two years to develop and at least another three years before full volume production. (CCF 2565-568); McAfee, Tr. 7441-42; *see* DX0224). Because the changes that take place between generations of DRAM standards are minimized by JEDEC's need for evolutionary change, that experience is at least suggestive of the amount of time it would take to develop and deploy standards that would avoid Rambus's patents. (McAfee, Tr. 7441-42; *see* DX224; CCF 127-128, 2569-573).

2743. It is important to consider the time it would take to ramp up production of the new technology as well as the time it takes to develop the standards because firms cannot avoid paying the royalty to Rambus until they are actually producing the new DRAM that does not infringe the patents in volume. (McAfee, Tr. 7443-44; 7446).

2744. It should be more difficult to reach a consensus to change the standard now than it

was to reach consensus on the original standard because the interests of the members of JEDEC are not as well aligned now as they were *ex ante*. (McAfee, Tr. 7447-48; CCF 2745-750).

2745. One reason the interests of the JEDEC members are not as well aligned now is because some members of JEDEC have licenses from Rambus and others do not. (CCFF 1999, 2004-11, 2014; McAfee, Tr. 7448).

2746. Because some JEDEC members have licenses from Rambus they have an incentive to maintain the current standard rather than changing it. (McAfee, Tr. 7449-50; CCF 1999, 2004-11, 2014).

2747. A second reason the interests of the JEDEC members are not as well aligned now as they were *ex ante*, is that firms have made different types of investments based on the standards that may make them have a different willingness to agree to particular changes. (McAfee, Tr. 7450-51).

2748. One example of the effect of differing investments on the willingness of firms to adopt a particular technology is the willingness of AMD to adopt a DRAM standard with a fixed burst length of four. (McAfee, Tr. 7451; CCF 2580-581).

2749. Had the industry adopted a fixed burst length of four for the original SDRAM standard, then AMD would have used that burst length. However, since the standard allowed the use of burst lengths of eight, the company optimized their processors to work with a burst length of eight and would now be harmed by a move to a burst length of four. (McAfee, Tr. 7451; CCF 2580-581).

2750. The investments that AMD made to exploit a burst length of 8 are specific investments in the programmable burst length features of SDRAM and DDR SDRAM. (McAfee, Tr. 7451-52).

2751. Opportunity costs refers to the opportunities that have been forgone because of an activity. (McAfee, Tr. 7455). The opportunity costs of creating a new standard to avoid the Rambus IP is the fact that the engineering talent, the resources, the testing facilities and all of the resources used are not available to other projects. (CCFF 2537; McAfee, Tr. 7456).

2752. In the DRAM industry, the opportunity costs of developing products to a new standard includes the costs of diverting teams from potentially profitable projects. In that case, the opportunity costs would exceed the wages of the engineers. (McAfee, Tr. 11294-295; CCF 2537).

2753. Opportunity costs would be incurred if DRAM manufacturers and other component makers were to seek to work around Rambus patents. (Rapp, Tr. 10154-55).

2754. The desire on the part of buyers to have multiple suppliers tends to encourage a single product to become a dominant standard. (McAfee, Tr. 7225-26).

(C) Intellectual Property Is an Important Concern in the Industry.

2755. Intellectual property is important from an economic standpoint in the DRAM industry. (McAfee, Tr. 7409-410).

2756. Industry members have been concerned for years about the potential for the presence of patents or other IP relating to the standards. (CCFF 300-304).

B. The Relevant Product Markets Are Technology Markets.

1. Market Definition Methodology.

2757. The normal starting point for any antitrust analysis is to define the relevant antitrust markets. (McAfee, Tr. 7310). Market definition sets the scope of competitive activity, *i.e.*, identifies the technologies, products, and firms that are relevant to the analysis. Market definition defines the context for performing competitive analysis. (McAfee, Tr. 7309).

2758. Defining a relevant antitrust product market requires identifying products or collections of products that do not have price-constraining alternatives. (McAfee, Tr. 7314).

2759. There is a well accepted methodology adhered to by economists for defining relevant markets in antitrust cases. (McAfee, Tr. 7312). The accepted methodology for defining markets is embodied in the approach taken by the Federal Trade Commission and Department of Justice Horizontal Merger Guidelines. (McAfee, Tr. 7314). The FTC-DOJ Horizontal Merger Guidelines use what is called the SSNIP test. (McAfee, Tr. 7331). SSNIP stands for a small but significant non-transitory increase in price. (McAfee, Tr. 7331). The SSNIP test is performed by analyzing the willingness of buyers to shift purchases to a competing product in response to a small but significant price increase. (McAfee, Tr. 7331-32).

2760. The approach of the Horizontal Merger Guidelines is to assume that a hypothetical monopolist controls sales of potentially competing products, and ask whether that monopolist can profitably increase price by a small but significant amount and sustain that price increase. (McAfee, Tr. 7314, 7317, 7331-32; see DX0173).

2761. If it is determined that the hypothetical monopolist cannot profitably sustain a small but significant non-transitory increase in price, then the market definition process requires that one keep adding additional potential substitutes to the provisional product market until the collection of products is such that the hypothetical monopolist can sustain a small but significant

price increase profitably. (McAfee, Tr. 7317-18).

2762. If historical price and quantity data are available, an economist can analyze buyer substitution by looking at what buyers have actually done in response to changes in relative prices. (McAfee, Tr. 7320-21). When historical pricing data relating to actual sales or transactions is unavailable, the general economic approach is nonetheless to try to understand buyer substitution. (McAfee, Tr. 7321). One approach to understanding buyer substitution in the absence of historical pricing data is to interview relevant purchasers in the marketplace. (McAfee, Tr. 7322).

2. Individual Technology Markets.

2763. Technology markets are markets for ideas or inventions where technology itself is a product. (McAfee, Tr. 7324; *see* DX0174). The demand for DRAM technology is derived from the demand for DRAMs, and the demand for DRAMs is derived from the final products in which DRAM is used. Ultimately the demand for the technology traces back to the demand for the final good. (McAfee, Tr. 7182, 7198-99; *see* DX-0132).

2764. In this case the appropriate starting point in the market definition exercise is to assume preliminarily that the challenged technologies comprise a relevant product market. (McAfee, Tr. 7313-14). The next step is to consider the next closest substitutes - that is, the technologies which are the most price-constraining to the challenged technologies. (McAfee, Tr. 7316-19; *see* DX0173).

2765. One begins by collecting alternative technically feasible technologies, *i.e.*, those technologies that can perform the same tasks as the challenged technologies in this case. (McAfee, Tr. 7327). The technical feasibility of a technology must be determined by engineering experts in the field. (McAfee, Tr. 7327-29).

2766. The next step is to ask which of those technically feasible technologies are price-constraining. (McAfee, Tr. 7330). Another way of characterizing that question is to ask which of the technologies are “commercially viable,” ones that, in the event of a price increase associated with the technology in question, informed buyers would have adopted or preferred over the technology with the price increase. (McAfee, Tr. 7330, 7333) This approach is parallel to the SSNIP test, except that no historical price data are available for the analysis. (McAfee, Tr. 7331-7333; *see* DX0176).

2767. Often in technology markets, as is true in this case, frequent trades have historically not taken place. Therefore there is little historical price and quantity data. (McAfee, Tr. 7321).

2768. In lieu of data pertaining to actual trades, serious consideration of a technology by

JEDEC participants suggests that informed buyers of the technology view those technologies as significant substitutes and hence price-constraining substitutes. (McAfee, Tr. 7333-34). Thus, in connection with defining relevant product markets in this case, it is useful to account for the JEDEC standardization and selection process. (McAfee, Tr. 7335).

2769. The relevant purchasers or buyers in this case are the decision-makers at JEDEC, *i.e.*, the participants who choose technology to be incorporated into JEDEC standards (McAfee, Tr. 7323-24). These buyers include DRAM manufacturers. (McAfee, Tr. 7323-24).

2770. JEDEC members include chipset manufacturers, microprocessor manufacturers, integrated circuit packaging companies, memory module manufacturers, motherboard manufacturers, DRAM manufacturers, PC-OEMs, printer manufacturers, networking companies and cell phone manufacturers. (CCFF 210-213).

2771. Here, in particular, DRAM manufacturers are the relevant consumers in the relevant technology markets and are the relevant consumers to consider in evaluating the competitive effects of Rambus's conduct. (Rapp, Tr. 9969-72).

2772. Factors that enter into JEDEC's decision-making process are relevant to the evaluation of commercially viable alternatives. (McAfee, Tr. 7335). For example, if "time to market" is a factor that influences JEDEC's decision-making process, that factor can affect an assessment of commercial viability. (McAfee, Tr. 7335-336).

2773. If "time to market" is an important factor, then economics teaches that decision-makers may not be willing to spend the amount of time necessary to find the perfect solution to the problem. (McAfee, Tr. 7336). Instead, decision-makers may "satisfice" – that is to say, evaluate technologies as equal when the benefit of finding the best solution is outweighed by the cost of the time it would take to find that solution. (McAfee, Tr. 7335-336).

2774. In situations before a standard issues, if there exists a range of roughly equivalent alternative technologies, simply picking one and standardizing on it facilitates coordination and avoids fragmentation. In such situations, the chosen alternative may be only slightly superior *ex ante* to other feasible alternatives, and the SSO could just have easily have chosen another alternative. (Teece, Tr. 10484).

2775. Completing standards in a timely manner is important to JEDEC.(CCFF 123)

2776. Individual JEDEC members differed with respect to the features they wanted to see in the standards. (CCFF 248-249, 251-254, 505-506)

2777. JEDEC members were willing to make compromises in order to have the standards pass more quickly. (CCFF 124)

2778. Another factor would be if JEDEC has a preference not to adopt technologies to which intellectual property attaches. If so, such a technology would be less likely to be selected and less likely to be considered commercially viable. (McAfee, Tr. 7337).

2779. There was a strong preference at JEDEC to avoid standards that included intellectual property. (CCFF 300-304).

2780. In addition, the evaluation of commercial viability should account for the cost of manufacturing and implementing a prospective technology relative to its expected performance, although differences in the positions of the firms in JEDEC might influence what each sees as the best cost/performance solution. (McAfee, Tr. 7337-39; CCFF 125)

2781. Also, in the DRAM marketplace, the technically superior technology may not always win the standards competition, if, for example, the technology's performance improvements are ahead of their time from the standpoint of what customers are demanding at a given point in time. (Rapp, Tr. 10065).

2782. For example, a form of dual-edged clocking called "high-speed toggle mode" was presented at JEDEC a number of times in the early 1990s, but was not adopted until the DDR SDRAM standard. (CCFF 129, 508-510, 515-526).

2783. At the time it was first proposed, one issue that the 42.3 committee had with the high speed toggle mode proposal was that it provided performance that was not needed at the time. (CCFF 129, 525-526).

2784. In assessing "commercial viability," it is also significant that, at the time that the technologies are selected for incorporation into a standard, not all of the facts are known. There may be substantial uncertainty as to all of the implementation costs and problems to be solved. (McAfee, Tr. 7340). The presence of uncertainty tends to blur the distinctions between the technologies, and thus make it more likely that a technology is commercially viable, *i.e.*, increase the likelihood that more technologies would be considered to be commercially viable. (McAfee, Tr. 7341; CCFF 130-131).

2785. "Commercially viable" alternatives include alternatives not chosen, *i.e.*, alternatives to which customers could shift even though they are not first on the hierarchy of choices and therefore are not initially chosen. (Rapp, Tr. 10231-32).

2786. The relevant time frame for defining product markets in this case is the time prior to the issuing of a standard. (McAfee, Tr. 7351).

2787. Based on the above-described analytical framework for defining the product markets relevant to analyzing the competitive issues in this case, there are four relevant

technology markets. (McAfee, Tr. 7163, 7390). These relevant technology markets are the latency technology market (McAfee, Tr. 7364; *see* DX0187), the burst length technology market (McAfee, Tr. 7373; *see* DX0194), the data acceleration technology market (McAfee, Tr. 7380; *see* DX0200), and the clock synchronization technology market (McAfee, Tr. 7385-86; *see* DX0207).

2788. Dr. Rapp did not conduct any market definition analysis in this case. (Rapp, Tr. 10032).

2789. Dr. Rapp does not have any disagreements with the Professor McAfee's market definitions that merit engagement. (Rapp, Tr. 10044).

2790. The relevant time frame for defining the latency and burst length technology markets was roughly 1992. (McAfee, Tr. 7351-52; CCF 527-544).

2791. Technically feasible alternatives for programmable CAS latency include: fixed CAS latency, pin strapping (setting CAS latency with a dedicated pin), programming CAS latency in the read command, and setting CAS latency by fuses. (CCFF 2130-227; *see* DX-0182).

2792. Fixed CAS latency, pin strapping (setting CAS latency with a dedicated pin), programming CAS latency in the read command, and setting CAS latency by fuses were all seriously considered by engineers at JEDEC. (CCFF 2131).

2793. Prior to the standardization of programmable CAS latency, fixed CAS latency was a commercially viable alternative to programmable CAS latency. (McAfee, Tr. 7354; *see* DX-0183).

2794. Prior to the standardization of programmable CAS latency, pin strapping, or the use of one or more dedicated pins to set CAS latency, was a commercially viable alternative to programmable CAS latency. (McAfee, Tr. 7357, 7359; *see* DX-0184).

2795. Prior to the standardization of programmable CAS latency, setting CAS latency in the read command was a commercially viable substitute for programmable CAS latency. (McAfee, Tr. 7359; *see* DX-0185).

2796. Prior to the standardization of programmable CAS latency, setting CAS latency by fuses was a commercially viable substitute for programmable CAS latency. (McAfee, Tr. 7361; *see* DX-0186).

2797. Because these technologies were commercially viable prior to standardization, they constrained the price of programmable CAS latency in the latency technology market.

(McAfee, Tr. 7363-64; CCF 2766; *see* DX0187).

2798. Insufficient evidence is available to determine whether scaling CAS latency with a clock frequency was a commercially viable alternative to programmable CAS latency. (McAfee, Tr. 7363).

2799. Technically feasible alternatives for programmable burst length include: fixed burst length, pin strapping (setting burst length with a dedicated pin), programming burst length in the read command, and using a burst interrupt command. (CCFF 2234-260, 2270-2318; *see* DX-0189).

2800. Fixed burst length, pin strapping (setting burst length with a dedicated pin), programming burst length in the read command, and using a burst interrupt command were all seriously considered by engineers at JEDEC. (CCFF 2235).

2801. Prior to the standardization of programmable burst length, fixed burst length was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7367; *see* DX-0190).

2802. Prior to the standardization of programmable burst length, setting burst length with one or more dedicated pins was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7368; *see* DX-0191).

2803. Prior to the standardization of programmable burst length, setting burst length in the read command was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7369; *see* DX-0192).

2804. Prior to the standardization of programmable burst length, use of a burst interrupt command to set burst length was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7370; *see* DX-0193).

2805. Because these technologies were commercially viable prior to standardization, they constrained the price of programmable burst length in the burst length technology market. (McAfee, Tr. 7373; CCF 2766; *see* DX-0194).

2806. Insufficient evidence is available to determine whether using fuses to set burst length was a commercially viable alternative to programmable burst length. (McAfee, Tr. 7372).

2807. The relevant time frame for defining the data acceleration technology and the clock synchronization technology markets is roughly 1995. (McAfee, Tr. 7376-77; CCF 2232-234, 2366-367).

2808. Technically feasible alternatives for dual-edge clocking include: interleaving banks on the module, doubling the clock frequency, and toggle mode. (CCFF 2322-365; *see* DX0196).

2809. Interleaving banks on the module, doubling the clock frequency, and toggle mode were all seriously considered by engineers at JEDEC. (CCFF 2323-24).

2810. Prior to the standardization of dual-edge clocking, interleaving banks on the module was a commercially viable alternative to dual-edged clocking. (McAfee, Tr. 7377; *see* DX-0197).

2811. Prior to the standardization of dual-edge clocking, doubling the clock frequency was a commercially viable alternative to dual-edged clocking. (McAfee, Tr. 7379; *see* DX-0199).

2812. Prior to the standardization of dual-edge clocking, toggle mode was a commercially viable alternative to dual-edged clocking. (McAfee, Tr. 7380; *see* DX-0214).

2813. Because these technologies were commercially viable prior to standardization, they constrained the price of dual-edged clocking in the data acceleration technology market. (McAfee, Tr. 7380, 7402; CCFF 2766; *see* DX-0213).

2814. Professor McAfee did not consider increasing the number of pins per module as a commercially viable alternative to dual-edged clocking. (McAfee, Tr. 7378; *see* DX0198)

2815. Technically feasible alternatives for on-chip PLL/DLL include: putting DLL on the memory controller, putting the DLL on the module, using a Vernier technique, and using no DLL at all . (CCFF 2366-2414; *see* DX0202).

2816. Putting DLL on the memory controller, putting the DLL on the module, using a Vernier technique, and using no DLL at all were all seriously considered by engineers at JEDEC. (CCFF 2367).

2817. Prior to the standardization of on-chip PLL/DLL, putting DLL on the memory controller was a commercially viable alternative to on-chip PLL/DLL. (McAfee, Tr. 7382; *see* DX0203).

2818. Putting the DLL on the module was a commercially viable alternative to on-chip PLL/DLL. (McAfee, Tr. 7383; *see* DX0204).

2819. Using a Vernier technique was a commercially viable alternative to on-chip PLL/DLL. (McAfee, Tr. 7383; *see* DX0205).

2820. Using no DLL at all was a commercially viable alternative to on-chip PLL/DLL. (McAfee, Tr. 7384; *see* DX0206).

2821. Because these technologies were commercially viable prior to standardization, they constrained the price of on-chip PLL/DLL in the clock synchronization technology market. (McAfee, Tr. 7385-86; CCF 2766; *see* DX-0207).

2822. Dr. Rapp agrees that potentially one of the lost competitive advantages to Rambus of disclosing patent-related information to JEDEC is that this could induce work-around efforts. (Rapp, Tr. 10171).

2823. In Dr. Rapp's view, the fact that a Rambus disclosure to JEDEC could induce work-around efforts is a reason why it would not have been in Rambus's interest to disclose additional patent-related information to JEDEC. (Rapp, Tr. 10171).

2824. Dr. Rapp agrees that it is possible that the effect of Rambus disclosing patent application-related information to JEDEC might have been that it would have caused JEDEC participants to commence efforts to try to work around what they understood the patent applications to cover. (Rapp, Tr. 10175).

2825. In his analysis of whether it would have been economically rational for JEDEC or JEDEC participants to switch to alternatives rather than include the Rambus-claimed technologies, Dr. Rapp assumed that JEDEC would choose the best cost-performance options. (Rapp, Tr. 10196-197).

2826. Dr. Rapp did not make any assumptions about the way that the JEDEC process or the JEDEC rules work. (Rapp, Tr. 10197).

2827. Dr. Rapp just assumed that a rational standards organization and rational members of such an organization would choose the best cost-performance options. (Rapp, Tr. 10197).

2828. All of the cost information that Dr. Rapp used in his analysis came from Mr. Geilhufe's testimony. (Rapp, Tr. 10201).

2829. In conducting the analysis summarized in his report, Dr. Rapp did not seek to obtain cost information on any alternatives from JEDEC or JEDEC participants or JEDEC-related documents that might cost information. (Rapp, Tr. 10201).

2830. Dr. Rapp did not review JEDEC-related materials to see if he could corroborate the cost information that he obtained from Mr. Geilhufe. (Rapp, Tr. 10201).

2831. Dr. Rapp understands that Mr. Geilhufe did not testify as to what cost information JEDEC or JEDEC participants had in this ex ante time period. (Rapp, Tr. 10203).

2832. Dr. Rapp agrees that if in the relevant time period, JEDEC participants had information about the costs of the alternatives that Dr. Rapp considered that was different from Mr. Geilhufe's cost information, that might undermine the economic conclusions that Dr. Rapp made about what decisions would be rational for JEDEC or JEDEC participants to make in the but-for world. (Rapp, Tr. 10203-204 (“It could, but it would depend greatly on the nature of that cost information and whether it was appropriate to solving the problem that we are solving by the cost analysis, Mr. Geilhufe's and subsequently mine.”)).

2833. Dr. Rapp agrees that if it were the case that JEDEC or JEDEC participants had different information about the costs of the alternatives that Dr. Rapp considered, that might suggest that JEDEC participants could have reached different conclusions than the conclusions that he reached and still have been acting in an economically rational manner. (Rapp, Tr. 10204 (“I will admit to the possibility that it would suggest that, but nothing more. In other words, it would not indicate that. It would raise the possibility of it.”)).

2834. Dr. Rapp agrees that the information JEDEC participants had in the relevant time period about the alternatives that Dr. Rapp considered as part of his analysis could have impacted what choices would have been economically rational for such JEDEC participants to make. (Rapp, Tr. 10204-205).

2835. Dr. Rapp agrees that he does not know what information any individual JEDEC participant in fact did have relating to any specific alternative that he considered. (Rapp, Tr. 10205).

2836. Because Dr. Rapp agrees that he does not know what information any individual JEDEC participant had relating to any specific alternative that Dr. Rapp considered, he also agrees that he cannot say as a matter of economic analysis what decision would have been economically rational for any JEDEC participant during the relevant time period based on information that was at the disposal of such JEDEC participants. (Rapp, Tr. 10205 (“But it is in the nature of the kind of analysis that economists normally do to use available data to make inferences about what individual decision makers would do at a particular time in a particular economic choice even though the data that was -- that were available, even though it's not known that that -- that those data were on the desktop of the individual in question. There's nothing unusual about that situation.”)).

2837. Dr. Rapp cannot rule out the possibility that for some of the companies that were participants of JEDEC in the relevant time, based on the information that they possessed, the economically rational thing would have been to support the use of various alternatives over the use of Rambus' technologies. (Rapp, Tr. 10205-206).

2838. Dr. Rapp agrees that JEDEC and/or specific JEDEC participants would not have known specifically what royalties Rambus would seek in connection with the technologies that Rambus has claimed in the event that those technologies were adopted as part of JEDEC's standards. (Rapp, Tr. 10206-207).

2839. Dr. Rapp agrees that it is possible that in the but-for world JEDEC participants might have been required to make judgments and choices between Rambus' technologies and alternative technologies without knowing what royalties Rambus ultimately might charge for the use of its technologies if they were used in the JEDEC standards. (Rapp, Tr. 10207-208 (“Without knowing with precision but with a certain capacity for anticipation if they had the disclosure at their disposal and if they knew about what the alternatives were.”)).

2840. Dr. Rapp agrees that, to the extent that JEDEC participants were uncertain about what royalty would apply, there could be varying projections from JEDEC participant to JEDEC participant regarding what royalty rates would apply to the Rambus technologies and those projections could differ from the royalty rates that he assumed in material ways. (Rapp, Tr. 10209 (“And I think the best single estimate of what the outcome of the variety of different possible forecasts is is the royalty rate that came in fact to be Rambus' royalty rate, the Rambus license royalty rate.”)).

2841. Dr. Rapp agrees that to the extent that prices are relevant to the analysis of what JEDEC would have done if Rambus had disclosed, the relevant price figures, if this information were available, would be the prices that individual JEDEC participants would have used in making their own calculations about the potential cost of Rambus royalties. (Rapp, Tr. 10211 (“If you'll allow me to say that the anticipations of price that they would have used, then the answer is yes.”)).

2842. Dr. Rapp agrees that the reason why anticipated prices are important to his analysis is that prices relating to products in his analysis would not have been for sale at the time the JEDEC members made their decisions. (Rapp, Tr. 10211-212).

2843. Dr. Rapp agrees that from the standpoint of the JEDEC participant in 1993 seeking to assess the cost of the Rambus royalties, if they were to do that in anything approaching an accurate sense, they would have to be making projections about the cost of not-yet-standardized devices in the marketplace extending out many years into the future. (Rapp, Tr. 10212).

2844. Dr. Rapp is aware that in the real world there have been instances in which JEDEC participants have disclosed patent-related information to JEDEC. (Rapp, Tr.10214).

2845. Dr. Rapp has not looked at the factual record in this case to determine whether in instances in which JEDEC participants have disclosed patent-related information to JEDEC,

JEDEC participants in deciding what actions to take have applied the same type of analysis or methodology that he applied. (Rapp, Tr. 10214).

2846. Dr. Rapp relied on only Dr. Soderman for his opinions about whether various alternatives identified by complaint counsel's experts would be subject to Rambus patents. (Rapp, Tr. 10215).

2847. Dr. Rapp understands that Dr. Soderman is not a patent lawyer. (Rapp, Tr. 10215).

2848. Dr. Rapp is aware that Dr. Soderman has never done design work on synchronous DRAMs. (Rapp, Tr. 10216).

2849. Dr. Rapp relied on the work of Mr. Geilhufe to find that there would be a number of different fixed CAS latencies in the event that alternative were chosen to work around the Rambus claims on programmable CAS latency. (Rapp, Tr. 10223).

2850. Before completing his expert report, Dr. Rapp did not look at the evidence relating to the process through which JEDEC made the decisions that it made in developing the relevant standards. (Rapp, Tr. 10111).

2851. Dr. Rapp developed his opinions about the commercial viability of various alternatives without having any understanding as to why JEDEC in fact chose the four Rambus technologies over any alternatives that it may have considered. (Rapp, Tr. 10111 (“And that is because the commercial viability and substitution qualities of those alternatives are independent of what got said in JEDEC.”)).

2852. Dr. Rapp wrote that “[k]nowing the reasons behind JEDEC's selection of SDRAM as the standard is important for evaluating the economic soundness of the assumption that the members would have switched to an alternative technology if Rambus' potential future royalty demands were disclosed at the time the SDRAM standard was being set.” (Rapp, Tr. 10112-113). That was a statement that Dr. Rapp made in the context of criticizing the work or conclusions of another economist in Rambus’s case against Micron. (Rapp, Tr. 10113).

2853. Dr. Rapp’s analysis of the alternatives to the disputed technologies is flawed. (McAfee, Tr.11208-209; *see* DX0359).

2854. Dr. Rapp’s analysis of the alternatives relies on a flawed methodology, (CCFF 2856-870) and is not robust to apparently reasonable changes in assumptions. (CCFF 2871-2884).

2855. Because of the flaws in Dr. Rapp’s analysis, it did not change Professor McAfee’s

opinions regarding the existence of competing alternative technologies *ex ante*. (McAfee, Tr.11279 (“I find his methodology to be flawed and, as a result, I find his criticism of my conclusion that there are commercially viable alternatives to be unfounded and, as a result, I am not inclined to change my conclusion.”)).

2856. Dr. Rapp’s analysis of alternatives fails to replicate actual JEDEC decision-making behavior. (McAfee, Tr. 11233-34; *see* DX0362).

2857. Simply analyzing what a “rational” DRAM manufacturer or a “rational” standard setting organization would select among alternative technologies cannot lead to an appropriate analysis of how the marketplace decides unless that methodology accounts for how the decisions are made. (McAfee, Tr. 11234-235 (“If you want to actually understand how the marketplace decides, you have to understand how the decisions are made. That is, you have to understand the process by which decisions are actually made, and that is not accounted for in Dr. Rapp’s approach.”)).

2858. An appropriate methodology to determine how JEDEC would select among technologies must take into account the time to market needs of the organization and the resulting satisficing behavior. (McAfee, Tr. 11234-235; *see* DX0362; CCF 122-124, 2650-658, 2772-777).

2859. Failing to take into account the time to market needs of JEDEC makes Dr. Rapp’s analysis unreliable. (McAfee, Tr. 11244; *see* DX0362).

2860. An appropriate methodology to determine how JEDEC would select among technologies must take into account the differences between royalties and manufacturing costs. (McAfee, Tr. 11241-242; *see* DX0362 (“A rational manufacturer would not be indifferent between a manufacturing cost and a royalty that were the exact same percentage of their costs generally.”); CCF 107-111).

2861. One difference between royalties and manufacturing costs is that manufacturing costs are subject to productivity gains that are to some extent under the control of the agent experiencing the costs. (McAfee, Tr. 11242-243; *see* DX0362 (“with manufacturing costs I can seek ways to minimize -- to minimize those costs. That is, I can find ways to actually reduce my costs overall. And that’s going to be not possible with a straight percentage royalty.”)).

2862. Another difference between royalties based on patents and manufacturing costs is that royalties, unlike manufacturing costs are subject to hold-up, which means that the costs might be increased on renegotiation. (McAfee, Tr. 11243; *see* DX0362 (“Royalties, on the other hand, are subject to hold-up in the sense that if, for example, the contract, the license under which royalties are paid, expires prior to the time that the patents that underlie those royalties expire, you’re going to have to renegotiate at some point, and at that point the royalties can be

renegotiated upward; that is, the lock-in can be exploited.”)).

2863. Failing to distinguish the differing effects of manufacturing costs and royalties on the decision making of firms at JEDEC has the effect of biasing Dr. Rapp’s analysis by understating the importance of royalties compared to manufacturing costs. (McAfee, Tr. 11244).

2864. An appropriate methodology to determine how JEDEC would select among technologies must take into account the potential impact of IP disclosures on evolution of DRAM technologies in but-for world. (McAfee, Tr. 11245; *see* DX0363).

2865. Changes in the world can change incentives, which can change the choices that economic actors make. (McAfee, Tr. 11246 (“how changes in the world affect choices that are made is actually a normal economic analysis point, and that changing, for example, the price of some technology, what will that do to demand for technology is right within the core of economic analysis.”)).

2866. Attempting to recreate the actual world using alternative technologies fails to take into account the fact that, had an alternative technology been selected, the world would have evolved in a different way in that technology would have developed differently. (McAfee, Tr. 11245; *see* DX0363).

2867. By failing to take into account the effect of changes in the world on the evolution of DRAM technologies, Dr. Rapp in making his cost estimates, for example, makes the mistake of assuming that JEDEC would have made the same choices regarding the number of CAS latencies and burst lengths using the fixed CAS latency and fixed burst length alternative that JEDEC made when using the programmable CAS latency and programmable burst length alternative that JEDEC chose in the actual world. (McAfee, Tr. 11246-247).

2868. An appropriate assumption regarding the evolution of the world had Rambus disclosed would take into account the effect of changes in the world on the incentives of the firms making the decisions. For example, given the fact that when fixed alternatives were presented at JEDEC they generally included only one or two alternatives, it would be highly unlikely that JEDEC would have chosen a large number of CAS latencies and burst lengths had JEDEC chosen the fixed CAS latency and fixed burst length alternatives. (McAfee, Tr. 11247 (“Given my understanding of the DRAM marketplace and in particular the dominance of a single standard that we've referred to, I would be highly surprised if the outcome of the marketplace was for all twelve of those possibilities to actually be offered in fact. Now, I wouldn't go as far as to say that only one of the twelve would be offered, although that's a possibility, and it's a possibility that was suggested to me by Desi Rhoden, but instead that not all twelve would be offered.”); CCF 2138, 2142-143, 2150-153, 2243-244, 2248-250).

2869. One effect of Dr. Rapp’s assumption that technology would have evolved the

same way it did even if Rambus had disclosed its patents is to overstate the costs of some of the alternatives. (McAfee, Tr. 11248 (“Well, in the choice of -- to be specific, in the choice of fixed CAS latency and fixed burst length, Dr. Rapp has assumed that all twelve of the theoretical combinations would be offered. If instead only two of those combinations were actually offered by the marketplace, then in fact he's overstated the costs by a factor of six.”)).

2870. Another effect of Dr. Rapp's assumption, that technology would have evolved the same way it did even if Rambus had disclosed its patents, is that assumption apparently led Dr. Rapp to erroneously ignore asynchronous alternatives entirely. Dr. Rapp apparently dismissed asynchronous alternatives entirely as not having sufficient potential for growth. However had an asynchronous alternative been chosen by JEDEC after Rambus disclosed there would have been an incentive on firms to invest in the further development of that technology. (McAfee, Tr. 11248-249 (“And my understanding of JEDEC behavior is that the burst EDO is actually a serious contender to SDRAM as an alternative and burst EDO is an asynchronous alternative. Had burst EDO been selected by the marketplace over SDRAM, the likely outcome from an economic perspective is that there would have been further investment in the asynchronous alternatives and that the marketplace might never have gone to synchronous DRAMs at all.”); CCF 568-569, 2233).

2871. Dr. Rapp's analysis is not robust to relatively small changes in the assumptions and changing his assumptions can overturn his conclusion regarding commercial viability. (McAfee, Tr. 11230; *see* DX0364).

2872. Because he failed to analyze alternatives that Dr. Soderman claimed infringes a Rambus patent, Dr. Rapp excluded what he would have calculated to be the least costly alternative to programmable CAS latency. (McAfee, Tr. 11252; *see* DX0365).

2873. Because he failed to analyze alternatives that Dr. Soderman claimed infringes a Rambus patent, Dr. Rapp excluded what he would have calculated to be the second least costly alternative to programmable burst length. (McAfee, Tr. 11254; *see* DX0365).

2874. As a consequence of his failure to analyze technologies that Dr. Soderman claimed to infringe Rambus patents, Dr. Rapp failed to identify two combinations of alternatives that his methodology indicates JEDEC would have preferred to the current SDRAM standard with the current Rambus royalties. (McAfee, Tr. 11256-258 (“So this slide has substituted the programming in read command, which is an allegedly infringing technology, for programmable CAS latency. That was the least expensive technology according to ... Mr. Geilhufe.... And that comes out as a total cost of .21 percent, which is substantially less than ... the alleged ... SDRAM royalty that Dr. Rapp used in his testimony. As a result, the consequence is that the conclusion that Dr. Rapp had found is in fact overturned.”); *see* DX0366).

2875. Because he failed to analyze an alternative that Dr. Soderman at one point

claimed infringes a Rambus patent, Dr. Rapp excluded what he would have calculated to be the least costly alternative to dual-edged clocking. (McAfee, Tr. 11259-260; *see* DX0365).

2876. As a consequence of his failure to analyze technologies that Dr. Soderman at one point claimed to infringe Rambus patents, Dr. Rapp failed to identify a combination of alternatives that his methodology indicates JEDEC would have preferred to the current DDR SDRAM standard with the current Rambus royalties. (McAfee, Tr. 11263-264 (“so with this change in assumptions but otherwise following exactly Dr. Rapp’s logic, the conclusion is the reverse of his conclusion, which is to say a rational manufacturer would prefer the alternatives rather than the Rambus license.”)); *see* DX0367).

2877. The effect of Dr. Rapp failing to consider asynchronous alternatives for the technologies in the JEDEC standard also led Dr. Rapp to exclude “toggle mode” which he would have calculated to be a low cost alternative to dual-edged clocking. (McAfee, Tr. 11265-266).

2878. As a consequence of his failure to analyze toggle mode, Dr. Rapp failed to identify a combination of alternatives that his methodology indicates JEDEC would have preferred to the current DDR SDRAM standard with the current Rambus royalties. (McAfee, Tr. 11266 (“The toggle mode as an alternative for dual-edged clocking is sufficiently inexpensive at 12 cents that it would still leave the overall cost less than the assumed DDR royalty.”)).

2879. Productivity gains and its effect on the cost of the technologies does not appear to have been considered by either Mr. Geilhufe in arriving at his estimates or Dr. Rapp in making his calculations. (McAfee, Tr. 11267-268; *see* DX0368).

2880. Even granting his methodology and his other assumptions as being correct, if Dr. Rapp is incorrect in his assumption of no productivity gains, the existence of productivity gains can change Dr. Rapp’s analysis, depending on the extent of productivity gains. (McAfee, Tr. 11271-272).

2881. Substituting alternative cost figures that account for productivity gains reverses the outcome of Dr. Rapp’s analysis to both SDRAM and DDR SDRAM. (McAfee, Tr. 11272; *see* DX0368).

2882. If the assumption is made that productivity gains are thirty percent per year then both the least costly and most costly combinations of alternatives described by Dr. Rapp become less costly than the current JEDEC SDRAM standard with the Rambus royalty. (McAfee, Tr. 11272-273 (“what I’ve done is replicate his analysis but with a 30 percent productivity increase, annual 30 percent productivity increase, to examine what that would do to ... his results for SDRAM. And as you can see,... even the most costly alternative with a 30 percent annual productivity increase winds up being cheaper than the Rambus alleged royalty.”)); *see* DX0369).

2883. If the assumption is made that productivity gains are thirty percent per year then both the least costly and most costly combinations of alternatives described by Dr. Rapp become less costly than the current JEDEC DDR SDRAM standard with the Rambus royalty. (McAfee, Tr. 11276-277; *see* DX0370; CCF 95-98).

2884. Dr. Rapp relies on the cost estimates of Mr. Geilhufe to the exclusion of lower cost estimates made by industry participants. If Dr. Rapp instead relied on the cost estimates of industry participants, then his conclusions would be reversed. (McAfee, Tr. 11278 (“The accuracy of Dr. Rapp's conclusions is only as good as the underlying assumptions. And in particular, if the cost assumptions are changed, are lowered, then his conclusions would be reversed.”)). For example, Mr. Geilhufe thought that an on-chip PLL would cost \$3.80, but there was testimony that such PLLs only cost one dollar. (CCFF 2343).

3. Cluster Market.

2885. In addition, it is analytically useful, as a matter of convenience, to consider a “cluster” market. (McAfee, Tr. 7390-92; *see* DX0210-11). A “cluster” market, in this case, would consider each of the four relevant product markets as a collection, based on the logic that the products are used in the same products, though strictly speaking they are not substitutes for one another. (McAfee, Tr. 7390-92).

2886. Here, the “cluster” market is defined as the synchronous DRAM technology market. (McAfee, Tr. 7390-91 *see* DX0210).

2887. In addition, asynchronous designs were relevant alternatives through 1995 and probably thereafter as an alternative in the cluster market defined as synchronous DRAM technology. (McAfee, Tr.7386; *see* DX0209).

2888. Asynchronous DRAM designs were price constraining alternatives to DRAM designs. (McAfee, Tr. 7387-89).

2889. Asynchronous designs would have been more successful if engineering effort had not been diverted away from them by the choice of JEDEC to standardize SDRAM. (McAfee, Tr. 7388; CCF 568-569, 2233).

C. The Relevant Geographic Market Is the World.

2890. The relevant geographic market for each relevant product market is the world. (McAfee, Tr. 7393; *see* DX0212).

2891. The relevant geographic market for each relevant product market is the world because buyers of technology typically do not care about the geographic source of technology.

(McAfee, Tr. 7393-95; *see* DX0212).

2892. The relevant geographic market for each relevant product market is the world because technologies tend to be licensed worldwide. (McAfee, Tr. 7393-95; *see* DX0212).

2893. The relevant geographic market for each relevant product market is the world because technologies tend to flow across national borders. (McAfee, Tr. 7393-95; *see* DX0212).

2894. The relevant geographic market for each relevant product market is the world because the downstream products are produced and used world-wide. (McAfee, Tr. 7393-95; *see* DX0212; CCF 3189-198).

2895. The relevant geographic market for each relevant product market is the world because the transportation costs of both technology and DRAMs are negligible. (McAfee, Tr. 7393-95; *see* DX0212).

2896. Technology markets tend to be worldwide markets. (McAfee, Tr. 7393-94).

2897. Because transportation costs are low, DRAM is also a world-wide market. (McAfee, Tr. 7394; CCF 3193-194, 3198).

D. Rambus Has Monopoly Power in the Relevant Markets.

2898. Monopoly power is the durable power of a company to maintain prices substantially above competitive levels and is a strong form of market power. (McAfee, Tr. 7419-20; *see* DX0216). By durable, economists mean that market power may be exercised for a significant period of time. It is long lasting. (McAfee, Tr. 7420).

2899. Rambus possesses monopoly power in each of the four relevant technology markets, and it also possesses monopoly power in the cluster market. (McAfee, Tr. 7420-21).

2900. It is Dr. Rapp's view that Rambus today possesses market power in each of the relevant markets defined by Professor McAfee. (Rapp, Tr. 10046).

2901. The source of Rambus's monopoly power derives from the fact that the relevant technologies have been incorporated into the JEDEC DRAM standards. (McAfee, Tr. 7432; *see* DX0218).

2902. Incorporation of the technologies in the JEDEC standards conferred monopoly power onto Rambus, because the JEDEC standards dominate the DRAM industry. (McAfee, Tr. 7428).

2903. If the JEDEC standards have dominated the DRAM industry for most of the last ten years that would indicate that owning patents over the JEDEC standard was likely to confer monopoly power. (McAfee, Tr. 7427-28).

2904. Market share statistics show that the JEDEC standards have dominated the DRAM industry for at least the last ten years. (McAfee, Tr. 7428; *see* DX0141; CCFF 267).

1. Indirect Evidence of Monopoly Power.

(A) Rambus Market Share.

2905. Programmable CAS latency using the mode register is a mandatory element of both the SDRAM and DDR SDRAM standards. (CCFF 562-563, 657).

2906. Programmable burst length using the mode register is a mandatory element of both the SDRAM and DDR SDRAM standards.(CCFF 562-563, 657).

2907. Dual-edged clocking of data is a mandatory element of the DDR SDRAM standard. (CCFF 656).

2908. PLL/DLL on the DRAM is a mandatory element of the DDR SDRAM standard. (CCFF 655).

2909. Rambus claims that its patents cover each of these features. (CCFF 1950-974).

2910. Rambus has made it clear in negotiations with DRAM manufacturers and the manufacturers of other compatible components that it believes that its patents cover the SDRAM and DDR SDRAM standards. (CCFF 1963-974).

2911. Rambus's internal communications indicate that it believes that its patents cover the SDRAM and DDR SDRAM standards. (CCFF 1951-1952; 2039-2042).

2912. The JEDEC SDRAM and DDR SDRAM standards determined what features were required to be present in JEDEC-compliant DRAMs. (CCFF 2905-906)

2913. The percentage of total DRAM production in the world today that is subject to Rambus's patent claims is in the upper nineties. (McAfee, Tr. 7430; *see* DX0219, DX0141; CCFF 2039-2042).

(B) The Industry is Locked In to the JEDEC SDRAM and DDR SDRAM Standards.

2914. The DRAM standards lead to monopoly power in the relevant technology markets. (McAfee, Tr. 11205).

2915. Technologies that were viable in each of the relevant markets before the standards were set are no longer commercially viable because of the incorporation of the technologies into the dominant JEDEC standards. (CCFF 2542, 2546, 2918-922; McAfee, Tr. 7421).

2916. The DRAM industry is no longer capable of switching from the technologies in the SDRAM standard to alternatives because it is locked in to the current standard. (CCFF 2501-505).

2917. The DRAM industry is no longer capable of switching from the technologies in the DDR SDRAM standard to alternatives because it is locked in to the current standard. (CCFF 2506-526).

2918. Technologies that were viable substitutes for programmable CAS latency in the *ex ante* period are no longer viable because the industry is locked in to the JEDEC standards. (McAfee, Tr. 7459-61; *see* DX0187; CCFF 2543).

2919. Technologies that were viable substitutes for programmable burst length in the *ex ante* period are no longer viable because the industry is locked in to the JEDEC standards. (McAfee, Tr. 7461-63; *see* DX0194; CCFF 2543).

2920. Technologies that were viable substitutes for dual-edged clocking in the *ex ante* period are no longer viable because the industry is locked in to the JEDEC standard. (McAfee, Tr. 7463-64; *see* DX0200; CCFF 2544).

2921. Technologies that were viable substitutes for on-chip PLL/DLL in the *ex ante* period are no longer viable because the industry is locked in to the JEDEC standard. (McAfee, Tr. 7464-65; *see* DX0207; CCFF 2545).

2922. If there were commercially viable alternatives available, the industry would substitute to those rather than pay royalties to Rambus. The fact that such substitution has not taken place demonstrates the absence of commercially viable alternatives today. (McAfee, Tr. 7630, *in camera*).

2923. Dr. Rapp has not calculated the switching costs that would be associated with changes to any other products other than DRAM products in the event that there were an effort to work around the Rambus patents through alternative JEDEC standards. (Rapp, Tr. 10127).

2924. Dr. Rapp has not considered what the costs of changing standards might be to chipset manufacturers, microprocessor manufacturers, socket manufacturers or anyone else.

(Rapp, Tr. 10127 (“I have considered that coordination efforts and changes in an industry as dynamic as the computer industry take place all the time, and I infer from that that costs to these other makers of complementary goods would for the most part be accomplished within the framework of continually changing your products.”)).

2925. Dr. Rapp’s basis to speak to the relative magnitude of the costs that would be borne by non-DRAM manufacturers if there was an attempt to develop alternative standards to work around Rambus’ patents is “the understanding that circuitry is subject to continual change in the computer industry and that switching costs are, generally speaking, relatively low when there is -- when change is routine, in the same way as in the DRAM industry.” (Rapp, Tr.10128).

2926. Dr. Rapp has not quantified the costs that the manufacturers of products other than DRAMs would experience if the JEDEC standards were changed to work around Rambus’ technologies.(Rapp, Tr.10128-129).

2927. Dr. Rapp is aware that Andy Bechtelsheim testified in this case, but did not read the testimony. (Rapp, Tr.10129).

2928. In assessing the lock-in question, Dr. Rapp has, with one exception, not considered the specific type of change that would have to be made to go to any given alternative that’s been raised as a possibility in the case. (Rapp, Tr. 10140-141 (“I -- the -- I haven’t considered, with the exception of the example that I gave, anything other than the general fact that it would be circuitry design changes.”)).

2929. In considering how long it would take either the DRAM industry as a whole, or multiple participants in the DRAM industry, to agree upon a single or uniform approach for working around Rambus’ patents if that were to be attempted, Dr. Rapp assumed that would take no more time than normal redesign efforts take. (Rapp, Tr. 10148 (“As I’ve said before, this is an industry, both the DRAM industry and the larger components industry, where technical change happens with high frequency and redesigns occur with high frequency, and I took for my assumption the fact that the changes that would be necessary to create and implement new designs involving the substitution of these alternatives could be done in a time frame of normal redesigns.”)).

2930. When Dr. Rapp refers to normal redesigns in the DRAM industry, he is referring either to process changes, redesigns in connection with die shrinks, or other sorts of changes. (Rapp, Tr. 10148).

2931. In evaluating how long it would take either the DRAM industry as a whole, or multiple participants in the DRAM industry, to agree upon a single or uniform approach for working around Rambus’ patents, Dr. Rapp did not consider separately the time it would take

multiple DRAM participants to agree upon a uniform approach for working around Rambus' patents, if they were to seek to do that. (Rapp, Tr. 10148-149).

2932. Dr. Rapp does not know how long it took JEDEC to agree upon the SDRAM specification from the start of the process to the end of the process. (Rapp, Tr. 10149).

2933. Dr. Rapp believes that it took JEDEC something on the order of about three years to agree upon the DDR specification from the start of the process to the end of the process. (Rapp, Tr. 10149).

2934. Dr. Rapp does not have any specific knowledge as to what features other than dual-edged clocking and on-chip PLL/DLL were added when JEDEC moved from SDRAM to the DDR SDRAM standard. (Rapp, Tr. 10152).

2935. Dr. Rapp did not, as part of his lock-in analysis seek to separately quantify any costs associated with the period of time it would take to either agree upon an approach for working around Rambus' patents or to implement such approach. (Rapp, Tr. 10154).

2936. Dr. Rapp agrees that the opportunity costs that might arise in the course of DRAM manufacturers or other component suppliers seeking to work around Rambus' patents is the opportunity cost of engineers and devotion of their activities to working around the Rambus patents. (Rapp, Tr. 10154-155).

2937. In assessing lock-in Dr. Rapp did not take into account any testimony that was given by DRAM industry participants during the trial relating to the subject of opportunity costs associated with engineers. (Rapp, Tr. 10155).

(C) Barriers to Entry

2938. Barriers to entry are a requirement to a finding of monopoly power. (McAfee, Tr. 7421-422). Barriers to entry allow a firm to increase prices without prompting entry of other firms into the market, which would force the prices back down. (McAfee, Tr. 7421-22, 7465).

2939. If, when a firm increases prices, other firms enter that firm's market in a way that forces prices back down, then the firm does not have monopoly power. (McAfee, Tr. 7420). Exploitation of a temporary circumstance is not generally considered to be monopoly power, the power to raise prices must be durable to be considered monopoly power. (McAfee, Tr. 7420).

2940. There are significant barriers to entry facing proponents of alternative technologies to the Rambus technologies. (McAfee, Tr. 7467-468).

2941. Those barriers to entry are the effects on entry of: scale, user switching costs,

strong learning curve, sunk costs, and patents. (McAfee, Tr. 7468; *see* DX0226).

(1) Economies of Scale.

2942. Economies of scale relates to the effect where per unit costs fall as more of a product is manufactured. (McAfee, Tr. 7189).

2943. The DRAM industry is an example of an industry with significant economies of scale, part of which flow out of large capital requirements. (McAfee, Tr. 7189; CCF 104).

2944. As a result of economies of scale, the costs of the DRAM product that has the largest share of demand tends to have its costs fall faster than products with lesser shares. This fact encourages a single product to become the dominant product and to become the industry standard. (McAfee, Tr. 7223, 7225).

2945. There are two types of economies of scale relevant to the DRAM industry: first, the fact that the minimum efficient scale of a fab is very large; and, second, the fact that as the industry gets larger, the average costs of related components falls. (McAfee, Tr. 7609-10).

2946. The first type of economies of scale is where a firm experiences reductions in cost as it increases its output because of large capital requirements. (McAfee, Tr. 7189). One example of the capital requirements that is relevant to economies of scale are the costs of doing a “die shrink” to reduce the costs of a DRAM. (McAfee, Tr. 7217 (“And so the effect of this is, from an economic perspective, if you’ve got two products that you might apply a die shrink to, you’re going to apply it to the product that you’re producing the most of. That is to say, the product... that you’re producing the most of will be the product you shrink first and the product you shrink most.”); CCF 105-106).

2947. Another example of the capital requirements that is relevant to economies of scale is the cost of design testing and qualification of new DRAM chips. (McAfee, Tr. 7222-23 (“[W]hen design, testing and qualification costs are large, you want to try to use a single or not too many different flavors or varieties of DRAM so that I don’t have to go through the whole design, testing and qualification process over and over and over again.”)).

2948. The second type of economies of scale is also called “network externality.” (McAfee, Tr. 7610-11). This relates to the effect that as the volume of a DRAM increases, the costs to produce compatible components will fall as well. (McAfee, Tr. 7472-73 (“[T]he larger the volume that is produced of a chip, the lower the cost per unit not just of the chip itself but also of the complementary goods. That is, the large investments made to produce complementary goods gets amortized over a larger volume of product, which lowers their per unit costs, which makes it even more attractive to the marketplace.”), 7611).

2949. This effect is one of the main reasons there tends to be one dominant DRAM standard, and it makes it difficult to displace an existing standard. (McAfee, Tr. 7473; CCF 2605-630).

2950. Network effects occur when systems compatibility is required to give value to the product. (Rapp, Tr. 9792-93). Compatibility of DRAM parts is an important issue from the standpoint of DRAM manufacturers. (Rapp, Tr. 10093). When compatibility requirements are substantial, the market or formal standard-setting will allow only one dominant standard to prevail. (Rapp, Tr. 9791).

2951. In circumstances where compatibility requirements are high, it is more likely that there will be only one dominant standard. (Rapp, Tr. 10096-97)

(2) Switching Costs.

2952. Another entry barrier is user switching costs. User switching costs refers to the costs of switching from the current standard. (McAfee, Tr. 7408, 7468).

2953. One type of switching cost is the “opportunity cost” of switching to a new standard. (McAfee, Tr. 7456 (“And so the opportunity cost of creating a new standard and getting out from under the Rambus IP is that the engineering talent,... and all of the resources used are not available to other projects which may be profitable.”); CCF 2537).

2954. A substantial volume of cost in the industry are switching costs. (McAfee, Tr. 7409). In addition, switching costs grow over time as the industry becomes progressively more locked in to the standard. (McAfee, Tr. 7435-37; *see* DX0221).

2955. Professor Teece agrees that if switching costs are high, the resultant royalty rate will be higher than if switching costs are low. (Teece, Tr. 10707-08).

2956. Standardization is a factor contributing to barriers to entry because the proponent of an alternative standard or an alternative technology must induce the rest of the industry to switch to the new standards. (CCF 2547-549). So standardization creates a barrier to entry. (McAfee, Tr. 7458-59, 7470).

2957. One type of switching cost are sunk costs, also known as specific investments. (McAfee, Tr. 7469). These costs are non-recoverable costs, and they have the effect of discouraging entry because an entrant faces a risk of the loss of these costs in the event of failure. (McAfee, Tr. 7469).

2958. The industry is characterized by such specific investments, particularly because of investments made by firms making complementary parts. (McAfee, Tr. 7296-297; *see* DX0164;

CCFF 35-77; 2501-526).

(3) Other Barriers to Entry.

2959. Another entry barrier is the strong learning curve characteristic of the DRAM industry. (McAfee, Tr. 7468) This barrier arises because an incumbent firm that has already gone down the learning curve has an advantage over a firm who has not. (McAfee, Tr. 7468).

2960. The presence of patents is also a contributor to an analysis of barriers to entry. (McAfee, Tr. 7469) Patents create a legal barrier to entry. (McAfee, Tr. 7470).

2961. Patents nearly always confer market power when they protect the right of a technology that is selected as the standard technology either by a standard-setting organization or *de facto* by the marketplace. (Rapp, Tr. 9964).

2. Direct Evidence of Monopoly Power.

2962. Because of Rambus's conduct, it is able to receive substantially higher and discriminatory prices in the relevant technology markets. (McAfee, Tr. 7633, *in camera*).

(A) Pricing above Competitive Levels.

2963. One major indicator of Rambus's monopoly power is that *ex post* pricing of Rambus's technologies substantially exceeds their *ex ante* value. That is, the technologies are priced at a level that is significantly above the *ex ante* value of the technology. (McAfee, Tr. 7422, 7622, *in camera*).

2964. Pricing at a level that is significantly above the *ex ante* value of the technologies suggests the exercise of monopoly power, which suggests the existence of monopoly power. (McAfee, Tr. 7422).

2965. The *ex ante* value of a technology is the amount that the industry participants would have been willing to pay to use a technology over its next best alternative prior to the incorporation of the technology into a standard. (McAfee, Tr. 7307-08). *Ex post*, the value of a standardized technology is the *ex ante* value of that technology plus the entire specific investment that has been made in the standardized technology. (McAfee, Tr. 7308).

2966. Because of the existence of alternatives to the Rambus-claimed technologies *ex ante*, the *ex ante* value of those technologies is limited by the incentive for the firms in JEDEC to engage in *ex ante* negotiations. (McAfee, Tr. 7494-95; 7625, *in camera*).

2967. The royalties that Rambus would likely to have been able to receive *ex ante*

would have been small or zero because of the existence of alternatives. (McAfee, Tr. 7625, *in camera*).

2968. The RDRAM royalty rate reflects another measure *ex ante* value of all the Rambus technologies. (McAfee, Tr. 7623, *in camera*).

2969. Rambus was charging _____, depending on volume, for RDRAM. (McAfee, Tr. 7623, *in camera*; CCF 1612-613).

2970. The base level royalty rate for DDR, _____, significantly exceeds _____. The higher rate is being charged to _____ among others. (McAfee, Tr. 7623, *in camera*; CCF 2004-11).

2971. In addition, _____ agreed to pay a rate of _____. (McAfee, Tr. 7623, *in camera*; CCF 1999, 2000).

2972. These facts about royalty rates indicate that the minimum rate that is being charged on DDR substantially exceeds the rate that was being charged for the manufacture of RDRAM. (McAfee, Tr. 7624, *in camera*).

2973. This, in turn, suggests that *ex post* pricing exceeds the *ex ante* value of the technologies, even where the *ex ante* value is approximated by the charges for the production of RDRAM. (McAfee, Tr. 7624, *in camera*). Therefore, the rates on DDR are indicia of Rambus's ability to exercise market power. (McAfee, Tr. 7627, *in camera*).

2974. If there were commercially viable alternatives available, the industry would substitute to those rather than pay royalties to Rambus. The fact that such substitution has not taken place demonstrates the absence of commercially viable alternatives today. (McAfee, Tr. 7630, *in camera*).

2975. On economic grounds, the DDR royalties reflect monopoly pricing. (McAfee, Tr. 7629, *in camera*).

(B) Price Discrimination.

2976. The power to price discriminate also reflects the exercise of market power. (McAfee, Tr. 7636, *in camera*).

2977. Price discrimination refers to charging buyers their willingness to pay rather than the cost of dealing with them. (McAfee, Tr. 7636, *in camera*). The ability to charge customers their willingness to pay reflects the absence of competition and so is direct evidence of the ability to raise prices above the competitive level. (McAfee, Tr. 7636-37, *in camera*).

2978. The fact that [redacted] is paying a higher royalty rate than [redacted] means that price discrimination is taking place. (McAfee, Tr. 7635, *in camera*).

2979. Even if the rates that [redacted] agreed to pay were competitive, the fact that [redacted] agreed to pay a higher royalty rate than [redacted] suggests that there are no longer any commercially viable alternative technologies available to DRAM users. Otherwise [redacted] would have switched to one of the alternatives to get the lower competitive rate. (McAfee, Tr. 7627, *in camera*).

2980. Rambus had a strategy of demanding higher royalty rates from those firms that litigate against Rambus. Rambus also had a strategy that it might not license at all to those companies that litigate against Rambus and lose. (CCFF 1990-994).

2981. A refusal by Rambus to license a company that litigated against it and lost would be discriminatory from an economic standpoint. (Teece, Tr. 10565-69, *in camera*).

2982. The [redacted] pays for the use of the Rambus technologies in SDRAM and DDR are not necessarily justified by costs related to the Rambus/Hitachi litigation. (Teece, Tr. 10556-57, *in camera*).

2983. The mere fact that an *ex post* royalty may have resulted from an arm's length negotiation does not mean that that royalty would be reasonable from the standpoint of what might have been negotiated *ex ante*. (Teece, Tr. 10513).

2984. Payment caps in license agreements have the effect of altering the effective royalty rate paid under the license. (Teece, Tr. 10616).

2985. License rates charged by companies that are not pure play technology companies are not entirely comparable to license rates charged by pure play technology companies such as Rambus. (Teece, Tr. 10622-23).

E. The Rambus Conduct was Anticompetitive.

2986. Exclusionary conduct is behavior or conduct that would exclude an equal or superior competitor from the marketplace. (McAfee, Tr. 7142, 7476). Such conduct harms consumers by reducing their choices and eliminating competition in the marketplace. (McAfee, Tr. 7476).

2987. Exclusionary conduct that eliminates equal or superior competitors will harm consumers by reducing their choices and eliminating competition in the marketplace. (McAfee, Tr. 7476).

2988. Exclusionary conduct has no valid efficiency rationale. (McAfee, Tr. 7477).

1. Providing False or Misleading Information.

2989. From an economic perspective, providing false or misleading information to economic decision-makers can have the effect of being exclusionary. (McAfee, Tr. 7167-68).

2990. The reason that such conduct can be exclusionary is because it causes the decision-makers to evaluate various alternative product choices that they face incorrectly, and thus when decision-makers try to choose the best product they may fail. (McAfee, Tr. 7168). The decision-makers may choose an inferior rather than a superior product because they have incorrect information about the alternatives. (McAfee, Tr. 7168).

2991. Misleading information tends to prevent competition on the merits by distorting consumer choice away from their optimal choices. (McAfee, Tr. 7482). The effect is to benefit inferior products and harm equal or superior products. (McAfee, Tr. 7483). For this reason, the provision of distorted information is often exclusionary. (McAfee, Tr. 7483; *see* DX0232).

2992. Rambus's conduct is exclusionary, because it was false and misleading, if the following assumptions are true: (1) at the time Rambus was at JEDEC, it possessed IP relevant to JEDEC standards / work; (2) Rambus failed to disclose relevant IP as required by JEDEC rules / process; (3) Rambus engaged in other, related misrepresentations while a member of JEDEC; (4) after leaving JEDEC, Rambus continued to conceal its IP; and (5) before during and after JEDEC participation, Rambus planned to enforce JEDEC-related IP. (McAfee, Tr. 7477-79; *see* DX0230).

2993. If the first two assumptions, are true, the third assumption is not necessary to find that Rambus engaged in exclusionary conduct. (McAfee, Tr. 7478).

2994. The fourth assumption is also not necessary to a finding that Rambus's conduct was exclusionary if the first two are true, but the fourth assumption relates to the magnitude of the effect of Rambus's conduct. (McAfee, Tr. 7478-79).

2995. The fifth assumption relates to whether Rambus's conduct was intentional rather than inadvertent. (McAfee, Tr. 7479).

2996. If the above assumptions are true, then on economic grounds Rambus's challenged conduct is exclusionary. (McAfee, Tr. 7481-82).

2997. At the time Rambus was at JEDEC, it possessed IP relevant to the work JEDEC was undertaking and the JEDEC standards. (CCFF 867-1237).

2998. Rambus failed to disclose relevant IP as required by JEDEC rules / process. (CCFF 1238-1357).

2999. Rambus engaged in other, related misrepresentations while a member of JEDEC. (CCFF 902-909, 968-976, 1062-1068, 1109-114).

3000. After leaving JEDEC, Rambus continued to conceal its IP. (CCFF 1259, 1676-1700).

3001. Before, during and after JEDEC participation, Rambus planned to enforce JEDEC-related IP. (CCFF 800-821, 1714-17, 1919-24, 1870-71).

3002. Rambus's challenged conduct would be exclusionary because Rambus's provision of misleading or incorrect information to JEDEC decision-makers excluded equal or superior competitors. In this case, the competitors were alternative DRAM technologies. (McAfee, Tr. 7168).

3003. The nature of the exclusionary conduct is the distortion of JEDEC's standardization process. (McAfee, Tr. 7173).

3004. The conduct would be exclusionary because it distorted the JEDEC standard-setting process. (McAfee, Tr. 7481). In so doing, it caused JEDEC to make mistakes that it would not have made if JEDEC had accurate information. (McAfee, Tr. 7481-82).

3005. According to Dr. Rapp, a failure on the part of Rambus to disclose to JEDEC information about pending or future patent applications that it was required to disclose would be "exclusionary" from the standpoint of antitrust economics, if there were no independent business justification for the failure to disclose. (Rapp, Tr. 9921).

2. Conscious Choice by Rambus to Jeopardize Its Own Rights.

3006. If Rambus was aware of legal risks associated with the assumed conduct, then that provides an additional basis for finding that Rambus's conduct was exclusionary. (McAfee, Tr. 7479-80; *see* DX0230). That basis is that if the assumption is true, then Rambus's conduct entailed a conscious choice to jeopardize the enforceability of patented intellectual property. (McAfee, Tr. 7501; *see* DX0231).

3007. An intentional decision to jeopardize the enforceability of patented intellectual property is potentially exclusionary behavior because it implies that the firm is expecting a substantial compensating benefit. (McAfee, Tr. 7502). The potential expected gain would be the ability to monopolize the relevant markets. (McAfee, Tr. 7502-503).

3008. Like predatory pricing, this conduct is irrational absent the expected benefits that would be obtained by excluding competition. (McAfee, Tr. 7502; *see* DX0238).

3009. If Rambus knowingly incurred a legal risk associated with its conduct, the implication from an economic perspective is that there must have been an expected compensating benefit. (McAfee, Tr. 7502).

3010. Rambus incurred a legal risk associated with its conduct. (CCFF 820-821).

3011. On economic grounds, the prospect of creating a monopoly on the JEDEC standards can be considered to be a compensating gain for undertaking a large risk of jeopardizing the enforceability of patented intellectual property. (McAfee, Tr. 7170-71).

F. Rambus's Anticompetitive Conduct Led to its Monopoly Power.

3012. The incorporation of Rambus technology in the SDRAM and DDR SDRAM standards contributes to Rambus' monopoly power in the relevant markets. (McAfee, Tr.7427-28).

3013. The distortion of the information available to JEDEC decision-makers is the basis on which Rambus's monopoly power has been obtained. (McAfee, Tr. 7173).

3014. One reason for this is the change in the bargaining positions between Rambus and other JEDEC participants that occurred going from the *ex ante* world to the *ex post* world. (McAfee, Tr. 7634, *in camera*).

3015. At the time before the relevant standards were set, consumers of the technology had a variety of options, and thus Rambus's bargaining power was limited, *i.e.*, the bargaining power was weighted more heavily toward DRAM manufacturers than it was toward Rambus. (McAfee, Tr. 7634, *in camera*).

3016. By contrast, in the *ex post* world, once the industry has been locked into the Rambus technologies, the bargaining power of DRAM manufacturers became limited, and Rambus was in a much stronger bargaining position. (McAfee, Tr. 7634, *in camera*).

3017. A standard economic methodology for assessing the effects of exclusionary conduct is known as a "but-for world" analysis. (McAfee, Tr. 7485).

3018. The but-for world analysis is to suppose, as a hypothesis, that Rambus had not engaged in the conduct at issue, and then ask what would have happened under those circumstances. (McAfee, Tr. 7485).

3019. In this case, the appropriate but-for hypothesis is that Rambus had not engaged in the challenged exclusionary conduct. (McAfee, Tr. 7485). In defining the but-for world, the appropriate thing is to change nothing except the conduct that is challenged. (Teece, Tr. 10735).

3020. Rambus's business strategy in the but-for world should mimic its business strategy in the actual world. (McAfee, Tr. 11311)

3021. The most likely outcome in the but-for world would be that JEDEC would avoid Rambus IP or would have licensed Rambus IP at lower royalty rates. (McAfee, Tr. 11304)

3022. In the but-for world where Rambus has disclosed relevant intellectual property to JEDEC in a timely fashion, it is first necessary to ask whether or not Rambus would have issued a RAND letter. (McAfee, Tr. 7486).

3023. It is not consistent with JEDEC behavior that in response to a disclosure of intellectual property by Rambus, it would not have requested a RAND letter. (McAfee, Tr. 11308; *see* DX0377; CCF 347-348).

3024. There is reason to doubt that Rambus would have issued a RAND letter. (McAfee, Tr. 11311; CCF 1091, 2419-2432). First, it appears that it was contrary to Rambus's business model for it to have issued a RAND letter because Rambus wanted flexibility to charge different royalty rates. (McAfee, Tr. 7489). Based on their business plan it was more likely than not that Rambus would have refused to issue a RAND letter. (McAfee, Tr. 11311; *see* DX0377)

3025. Another reason to doubt that Rambus would have issued a RAND letter is that refusing to issue a RAND letter might help RDRAM succeed in the marketplace by delaying the passage of the JEDEC standard. (CCF 1616). Not issuing a RAND letter might have stalled the JEDEC standard because of the requirement that JEDEC not include intellectual property in the standard without such a RAND letter. (McAfee, Tr. 7489-90).

3026. In the case where Rambus had not issued a RAND letter, assuming that JEDEC was prohibited by its own rules from including technologies covered by patent rights in a standard, the JEDEC standard would not have incorporated Rambus's intellectual property. (McAfee, Tr. 7487).

3027. JEDEC would not have included a technology for standardization if they understood in advance that the technology would not be offered to everyone on a non-discriminatory basis. (CCF 347-348)

3028. Under the assumption that Rambus would have refused to issue a RAND letter,

Rambus's failure to disclose its intellectual property in a timely fashion caused the inclusion of the Rambus technology into the JEDEC standard. (McAfee, Tr. 7488). In that case, the misrepresentations matters. (McAfee, Tr. 7487-88 ("In that event, the standard does not incorporate Rambus IP, and as a result, we can conclude that in this branch of the tree Rambus' failure to disclose actually caused the inclusion of the Rambus technology in the JEDEC standard."); McAfee, Tr.11312; *see* DX0377).

3029. If Rambus would have issued a RAND letter, JEDEC most likely would not have included Rambus's intellectual property in its standards. (McAfee, Tr. 7491; 7496-500; *see* DX0236-37). The reason for this conclusion is that other commercially viable technologies were available to JEDEC. (McAfee, Tr. 7491; CCF 2433-440).

3030. In fact, given the existence of alternatives, there is no real probability that JEDEC would have adopted the existing standards had Rambus disclosed its intellectual property, even if it issued a RAND letter. (McAfee, Tr. 11315-316; *see* DX0377).

3031. JEDEC members were opposed to the use of royalty bearing technologies in the JEDEC standards. (CCFF 300-304)

3032. Given JEDEC's incentive to avoid royalties because of the price sensitivity of DRAM customers, it would have been difficult to arrive at a consensus to include Rambus's intellectual property into a standard when other commercially viable alternatives existed. (McAfee, Tr. 7492).

3033. One reason why JEDEC would have a preference to avoid including patented technologies in their standards is that the incorporation of proprietary technologies when commercially viable alternatives exist can expose the industry to the threat of hold-up. (McAfee, Tr. 7495-96 ("The incorporation of proprietary technology when commercially viable alternatives exist generally exposes the industry to the threat of hold-up.")).

3034. Since a RAND letter does not specify royalty rate, firms have an incentive for *ex ante* negotiation. (McAfee, Tr. 7492-93 ("And since a RAND letter doesn't specify a royalty rate, firms are at risk when they've incorporated patented technology that the royalty rates may turn out to be very large. The RAND letter does specify "reasonable," but to a great extent "reasonable" is in the eye of the beholder. [T]he firms have an incentive for *ex ante* negotiation; that is to say, the firms that intend to practice the JEDEC standard have an incentive to say, 'Hey, what's this going to cost me'? That is to say, to investigate what does the word 'reasonable' mean in the RAND letter.")).

3035. In addition, the fact that Rambus was not a manufacturer, but instead a "pure play" technology company would have given JEDEC members additional incentive to attempt to negotiate royalty rates with Rambus *ex ante* rather than *ex post*. As a pure play technology

company, Rambus would not have been subject to the restrictions on royalty rates because of cross licenses that limit the royalties of other firms. (McAfee, Tr. 7493-94)

3036. *Ex ante* negotiation places a limit on the exercise of monopoly power, because, *ex ante*, the users of the technology have alternatives available. (McAfee, Tr. 7494-95). Hence, the technology users will be in a stronger bargaining position than they would be after they become locked into a technology. The effect would be to change the price that is charged for the technologies. (McAfee, Tr. 7495, 11313-314; *see* DX0377).

3037. When Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he was not familiar with the details of the process that JEDEC went through in the real world in selecting the Rambus-claimed technologies. (Rapp, Tr. 10106-109).

3038. When Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he did not know whether, prior to their ultimate adoption, there was any opposition within JEDEC to the use of any of those technologies. (Rapp, Tr. 10109).

3039. When Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he did not know whether any alternatives to those technologies were discussed within JEDEC. (Rapp, Tr. 10109).

3040. When Dr. Rapp reached his conclusions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, he did not know what pros or cons may have been discussed within JEDEC relating to any given alternative. (Rapp, Tr. 10110).

3041. Before completing his expert report, Dr. Rapp did not look at the evidence relating to the process through which JEDEC made the decisions that it made in developing the relevant standards. (Rapp, Tr. 10111).

3042. In developing his opinions regarding the effect of Rambus's non-disclosures to JEDEC on whether JEDEC would have adopted the Rambus technologies anyway, Dr. Rapp did not give consideration to JEDEC's specific processes or rules for dealing with patent disclosure issues. (Rapp, Tr. 10116 ("Well, I understood in general terms what they were, but I didn't delve into them in forming that conclusion.")).

3043. When he developed his opinions as to what JEDEC would have done in a but-for world in which Rambus had made the challenged disclosures or non-disclosures, Dr. Rapp was not aware of anything in JEDEC's rules or in its procedures that might have precluded JEDEC

from using Rambus' technologies, as long as they ranked higher on a cost-performance basis than all alternative technologies. (Rapp, Tr. 10119).

3044. When he developed his opinions, Dr. Rapp was not aware of whether, in the history of JEDEC, there has ever been a situation in which a company had disclosed a patent or patent application to JEDEC and JEDEC proceeded to adopt that proprietary technology as part of its standard. (Rapp, Tr. 10119).

G. The Anticompetitive Effect of Rambus's Conduct Extends Beyond the Relevant Markets.

3045. One consequence of Rambus's monopolization of the relevant technology markets is that innovation has been misdirected. (McAfee, Tr. 7174). This effect came about because royalties create a disincentive to further innovation. That is, royalties create a dampening of incentives to innovation because part of the benefits flow to Rambus in the form of increased royalty payments. (McAfee, Tr. 7174).

3046. Rambus's monopolization has caused misdirection of efforts that otherwise would have taken place. (McAfee, Tr. 7638, *in camera*) That misdirection of efforts shows up in harm to innovation insofar as technology has not been investigated to the extent that it would otherwise have been investigated. (McAfee, Tr. 7639, *in camera*).

3047. For example, Rambus's monopolization of the relevant technology markets quite possibly distorted investments related to asynchronous technology. (McAfee, Tr. 7640-41, *in camera*; CCF 2230-233).

3048. The monopolization also distorted specific design investments, *i.e.*, because of Rambus's monopolization, firms in the industry over-invested in SDRAM and DDR SDRAM under the mistaken hypotheses that they were not going to be held-up for royalties. (McAfee, Tr. 7641-42, *in camera*).

3049. Innovation is also harmed because when a DRAM manufacturer performs a die shrink or when it increases its wafer size, it increases the number of chips it makes. As a consequence, the royalty payment it must pay to Rambus increases. In that sense, the total level of royalty payments acts like a tax on innovative activity. (McAfee, Tr. 7640, *in camera*).

3050. Another anticompetitive effect of Rambus's monopolization of the relevant technology markets is the threat of increased prices for the physical DRAM products. (McAfee, Tr. 7175). This effect arises because, in the long-run, the royalty costs can be expected to be passed on to consumers in the form of higher DRAM prices and lower DRAM output. (McAfee, Tr. 7176).

3051. Although, at present, there has not yet been an observable direct impact on DRAM supply and DRAM pricing as a result of Rambus's monopolization of the relevant technology markets, over the long-run, the increased costs due to the royalties paid by DRAM manufacturers can be expected to increase the prices of DRAM. (McAfee, Tr. 7645-46, *in camera*)

3052. Still another effect of the monopolization is that it increased the difficulty of reaching consensus within JEDEC about whether to develop a new standard and what it should be. This increased difficulty creates costly delay. (McAfee, Tr. 7644, *in camera*).

3053. Still another consequence of Rambus's monopolization of the relevant technology market is that it threatens to undermine industry confidence in open standards and the standards process. (McAfee, Tr. 7176).

3054. Rambus's hold-up of the DRAM industry threatens the standardization process because it demonstrated that the benefits of standard-setting potentially could be captured by one of the market participants. In the future, this could discourage standard-setting within JEDEC. (McAfee, Tr. 7646-47, *in camera*; CCF 2049).

3055. In addition, resources directed toward working around Rambus's patented technology and creating a subsequent standard delays the roll out of the subsequent standard. (McAfee, Tr. 7644-45, *in camera*).

3056. Another competitive effect of Rambus's monopolization of the relevant technology markets is the actual and threatened future distortions to competition in those markets. (McAfee, Tr. 7638-639, *in camera*).

3057. Another effect of Rambus's monopolization of the relevant technology markets is the incurrence of litigation costs. Litigation effort deploys resources that otherwise would have available for other purposes. (McAfee, Tr. 7642, *in camera*; CCF 1995-2032).

3058. Another effect of the monopolization of the relevant technology markets is the diversion of resources that some firms have undertaken to design around Rambus's patented technologies. (McAfee, Tr. 7643, *in camera*).

3059. Another competitive effect of Rambus's monopolization of the relevant technology markets is increased market uncertainty. (McAfee, Tr. 7643, *in camera*) From an economic standpoint, uncertainty is inherently costly because it creates difficulties to making good decisions. (McAfee, Tr. 7643, *in camera*).

3060. Rambus's monopolization of the relevant technology markets has increased the uncertainty prevailing in the marketplace with respect to what the royalties would be, how long

they would continue to be paid. The monopolization has also created uncertainty regarding the overall future of standards and their adoption. (McAfee, Tr. 7644, *in camera*; CCF 2033-2048).

3061. Paragraphs 3061 - 3099 are unused.

XIV. A Broad Remedy Is Necessary.

A. The Most Appropriate Available Remedy Is To Prohibit Rambus From Enforcing Any Patents With A Priority Date Prior to June 18, 1996 Against JEDEC-Compliant DRAMs.

3100. The harm resulting from Rambus's conduct amounts to hundreds of millions of dollars per year. (CCFF 3101-3102).

3101.

(McAfee, Tr. 7650, *in camera*; see DX0245, *in camera*).

3102. Another rough quantification of the effects of Rambus's conduct is to apply an approximate royalty rate to an approximate \$20 billion value for DRAM. Applying such a royalty rate results in a rough estimate of million a year in royalty payments. (McAfee, Tr. 7653-54, *in camera*); see also CX1391A at 32 (showing average royalty rate increasing from 1% to 5% and annual royalty income increasing from \$90 million to \$3 billion); CX0527 at 1, *in camera* (); CX1401 at 10, *in camera* ().

3103. In assessing what remedies should be to address exclusionary conduct, an economist first asks whether the world can be restored to what it would have been absent the anticompetitive conduct. (McAfee, Tr. 7510).

3104. Restoration of the world cannot be achieved because almost a decade's worth of investments in the existing technologies has already occurred. (McAfee, Tr. 7511) An installed base of SDRAM and DDR SDRAM in the devices and complementary devices to those technologies has already been developed. (McAfee, Tr. 7513) Those investments have already been made. There is no way to undo the existence of those investments today. (McAfee, Tr. 7513).

3105. In addition, investments in alternatives like asynchronous technology were not made because SDRAM was believed to be a better alternative than it proved to be, because it was believed not to carry intellectual property from Rambus. (McAfee, Tr. 7516).

3106. Because the first best remedy is unacceptable, one must look for a second best remedy, short of restoring the world to the way it would have been. (McAfee, Tr. 7517).

3107. The "but-for" world in which Rambus discloses on a timely basis and JEDEC has

the opportunity to either select alternatives or conduct ex ante negotiations between JEDEC members and Rambus, is no longer available. (McAfee, Tr. 7512).

3108. Although prohibition of enforcement of Rambus's patents against JEDEC-compliant DRAM would restore competitive pricing because they eliminate Rambus's ability to exercise monopoly power, they would not fully undo all the harmful effects. (McAfee, Tr. 7179) As a practical matter, in this case, restoration of the world to what it would have been cannot be achieved. (McAfee, Tr. 7511).

3109. On economic grounds, undoing the anticompetitive harm resulting from Rambus's conduct requires undoing the monopolization itself. (McAfee, Tr. 7177).

3110. Prohibiting enforcement of the patents against JEDEC-compliant DRAM would undo most, but not all, of the effects of the monopolization in the relevant technology markets. (McAfee, Tr. 7178-79, 7511).

3111. Based on the practical considerations of the world as it exists today, on economic grounds, Rambus should be prohibited from enforcing any intellectual property that should have been disclosed, whatever that intellectual property might be. (McAfee, Tr. 7521) In particular, the second best remedy should require that Rambus be prohibited from enforcing against JEDEC-compliant DRAMs any patents filed (or based on filings) prior to June 18, 1996. (McAfee, Tr. 7518).

3112. The remedy of prohibiting Rambus from enforcing against JEDEC-compliant DRAMs any patents filed (or based on filings) prior to June 18, 1996 will restore competitive pricing in the relevant technology markets and mitigate other anticompetitive effects. (McAfee, Tr. 7522).

B. The Remedy Should Extend To All Technologies Included in JEDEC-Compliant DRAMs.

3113. Rambus may hold patents containing claims that cover technologies used in SDRAMs and DDR SDRAMs other than programmable cas latency, programmable burst length, dual edged clocking, and on-chip DLL. (CCFF 3114-3182).

3114. Rambus has asserted that various features contained in SDRAMs and DDR SDRAMs, in addition to the four technologies identified in the complaint, are Rambus innovations. (CX1363 at 1 (listing "Multi-bank architecture" and "Doubled banks" as Rambus innovations); *id.* at 3 (list indicating that "Low voltage swing signaling" and "Source synchronous signaling" are Rambus innovations contained in DDR SDRAMs); CX1371 at 5 (informing nVidia that "Rambus innovations" include "Low voltage swing signaling" and "Source synchronous signaling"); CX1383 at 4 (informing ATI of same)).

3115.

(CX1681 at 3, *in camera*) (); CX1680 at 16, 19, 24, *in camera*) (); CX1687 at 8, 12, 28, *in camera*) ()).

3116. Rambus has stated publicly that it would seek to enforce patents that allegedly cover technologies used in SDRAMs and DDR SDRAMs that they have not yet asserted in litigation to date. (CX1888 (“In addition [to the 16 or so U.S. and European patents asserted against Infineon, Hyundai and Micron], Rambus holds newly issued U.S. and European patents covering Rambus inventions used by SDRAMs and DDR SDRAMs that have not yet been asserted in any litigation and are not impacted by the [Infineon trial court’s] decision.”); CX1382 at 29-30 (In a presentation in which Rambus identified that one way to “win” would be to collect royalties on competitive alternatives, Rambus included a chart showing that Rambus’s filed U.S. patent applications rose to approximately 200 and issued U.S. patents rose to 94 in 2000.); CX1403 at 30 (“Virginia decision involved only 4 patents; we may have others which are used by SDRAM/DDR.”)).

3117. Rambus recently has obtained additional patents that appear to cover a technology that Rambus has not yet asserted patents against. For example, on October 22, 2002 the PTO issued Rambus patent 6,470,405 (the ‘405 patent), which includes a claim relating to “initiating the precharge operation automatically after the write operation is initiated.” (CX1545 at 45).

3118. The additional technologies as to which Rambus may hold patent rights include technologies that Rambus observed presented at JEDEC while it was a JEDEC member. (CCFF 3123-3124, 3139-3140, 3153-3154, 3163, 3179).

3119. The additional technologies as to which Rambus may hold patent rights include technologies that Rambus representatives, including Richard Crisp, believed might be covered by claims in Rambus’s pending patent applications, or could be covered by claims that Rambus could file as amendments to its pending patent applications, at the time that Rambus was a JEDEC member. (CCFF 3132-3133, 3143-3146, 3156-3157, 3166-3170, 3177, 3179).

3120. At the time it was a JEDEC member, Mr. Crisp did not disclose to JEDEC that he believed Rambus had pending patent applications containing claims, or that Rambus could amend its pending patent applications to add claims, covering these additional technologies.

(CCFF 3136, 3150, 3160, 3173, 3180).

1. Low Voltage Swing Signaling.

3121. In late 1991, Mr. Crisp had consulted with Rambus concerning Rambus patent applications and the use of “low swing signals on DRAM.” (CX1932; CX3125 at 279-80 (Vincent, Dep.) (By December 1991, Rambus may have already drafted patent applications containing claims covering voltage swing levels as low as 2 volts for use with DRAMs.)).

3122. In late 1991-January 1992, Mr. Vincent continued to work with Mr. Crisp and others at Rambus as he drafted and filed patent claims. (CX1933 at 1-9; CX3125 at 279-80, 287-88 (Vincent, Dep.); Crisp, Tr. 3027-28).

3123. At the February 27, 1992, JC 42.3 meeting, the NEC, Fujitsu, Mosaid, Sun, and Intel proposed a low-voltage swing signaling interface. (JX0012 at 39, 76, 104, 111, 113; Crisp, Tr. 3045-46). At this same meeting, the JC-42.3 Committee discussed GTL technology for use with SDRAM. (JX0012 at 36, 56-58, 60, 101-02, 104, 111).

3124. On February 27, 1992, Billy Garrett attended a JC 42.3 meeting in which he witnessed SDRAM proposals to the Subcommittee, including low voltage swing signaling relating to LVTTTL and GTL technology. (JX0012 at 36-37; CX0672 at 1; Crisp, Tr. 3045-46). After attending the meeting, Mr. Garrett distributed an e-mail to Rambus staff titled, “JEDEC Meeting Notes 2/27, 2/28,” explaining that Jedec had discussed these and other technologies at the February 1992 meeting. (CX0672 at 1).

3125. In his e-mail to Rambus staff about the February 1992 Jedec meeting, Mr. Garrett recognized an opportunity for Rambus to either influence the voltage standard or “use [Rambus] patents to keep current-mode interfaces off of DRAMs.” (CX0672 at 1).

3126. A week after this meeting, Rambus’s outside patent counsel, Lester Vincent, filed a preliminary amendment to a patent application concerning low voltage swing signals. (CX0672 at 1; Crisp, Tr. 3046).

3127. On March 25, 1992, Rambus Vice President Allen Roberts and outside patent counsel Lester Vincent discussed “JEDEC” and the “need [for] preplanning before accuse others of infringement.” (CX1941; CX3125 at 296-302 (Vincent, Dep.)). Mr. Vincent’s notes from that meeting contain the reference “Jedec Committee => Standards for DRAMs” and reflect discussion of “Advising JEDEC of patent applications.” (CX1941).

3128. On March 27, 1992, Mr. Richard Crisp and Vice President Roberts met in person with Mr. Vincent. (CX3125 at 310, 311-313 (Vincent, Dep.; CX1942). Mr. Crisp or Mr. Roberts informed Mr. Vincent that “Rambus attended [a] meeting with a hundred others where

JEDEC's proposal to establish [a] standard for small swing signals for sync DRAM was discussed." (CX1942 at 1; CX3125 at 312-313 (Vincent, Dep.)).

3129. At the April 8, 1992, Special SDRAM Task Group meeting, the JC 42.3 Subcommittee considered SDRAM proposals that included low voltage swing signaling such as LVTTL and/or GTL. (CX0034 at 32 (IBM), 33 (NEC, Fujitsu), 35 (Samsung, Hitachi), 36 (Mitsubishi)).

3130. At the May 7, 1992, JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included low voltage swing signaling such as LVTTL and/or GTL. (CX0034 at 59 (NEC), 122-123 (Fujitsu)).

3131. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included low voltage swing signaling (CX0042 at 31 ("It is proposed that LVTTL be used for the I/O drivers and receivers.")).

3132. On June 18, 1993, Mr. Fred Ware of Rambus sent an e-mail stating that he had spoken with Lester Vincent and he was including a list of the current status of the additional claims that Rambus wanted to file on the original patent. Included on the list was a "DRAM using low-voltage-swing signal levels. . . This claim would be directed against GTL technology." (CX0703 at 1; Crisp, Tr. 3165-66 (testifying that CX0703 refreshed his recollection that claims on low voltage swing signaling had been filed by the date of the document, which was June 18, 1993)).

3133. On July 9, 1993, Mr. Crisp and Mr. Ware met with Mr. Vincent to discuss the status of Rambus's patent claims. (CX3126 at 447-449 (Vincent, Dep.); CX1963 at 1-4). Mr. Vincent's handwritten notes from that meeting indicate that claims on low voltage swing signaling had already been filed. (CX1963 at 4; see also CX3126 at 449-52 (Vincent, Dep.) (Mr. Vincent recalled discussing low voltage swing signaling claims prior July 1993 and may have already filed some low voltage swing signaling claims by then)).

3134. On May 24, 1995, after being asked by Mr. Kelley to inform the JC-42.3 Subcommittee as to whether Rambus had patents relating to the SyncLink presentation at JEDEC, Mr. Crisp stated to Rambus executives and others (but not to the JC-42.3 Subcommittee), "As far as intellectual property issues go here are a few ideas: . . . 2. DRAM with low swing signaling [sic]." (CX0711 at 68, 73; Crisp, Tr. 3268-71).

3135. Jedec included low swing signaling technologies in SDRAM and DDR SDRAM standards. (CX0234 at 116, 189-95)

3136. Mr. Crisp never informed Jedec that Rambus believed it could obtain patent coverage over low voltage swings as they were being discussed at JEDEC. (Crisp, Tr. 3455; *see*

DX0028).

3137. Rambus may intend to assert patents relating to low voltage swing signaling against manufacturers or users of DDR SDRAMs. (CX1363 at 3 (list indicating that “Low voltage swing signaling” is a Rambus innovation contained in DDR SDRAMs); CX1371 at 5 (informing nVidia that “Rambus innovations” include “Low voltage swing signaling”); CX1383 at 4 (informing ATI of same)).

2. Dual Bank Design.

3138. Mr. Crisp testified that “DRAM with multiple open rows” describes a technology that is related to but broader than the two bank feature discussed within JEDEC. (CX0686; Crisp, Tr. 3122).

3139. At the February 1992 JC 42.3 meeting that Billy Garrett attended, the Subcommittee addressed the topic of “multiple [active] subarrays” in two presentations (JX0012 at 34, 37) and multibank or dual bank design in other presentations (*See, e.g., id.* at 60). At the February 27, 1992, JC 42.3 meeting, the Subcommittee considered proposals for multibank, or dual bank, design from NEC, Mitsubishi, Fujitsu, and Sun. (JX0012 at 39, 60, 76, 110; CX0672 at 1 (Mr. Garrett’s notes from this meeting indicate that JEDEC had reached a “general agreement on two banks.”)).

3140. At the May 7, 1992, JC 42.3 meeting, the Subcommittee considered SDRAM proposals that included both dual bank design and low voltage swing signaling such as LVTTL and/or GTL. (CX0034 at 59 (NEC), 122-123 (Fujitsu)). During that meeting, Mr. Kelley of IBM, prompted by Mr. Meyer of Siemens, asked Mr. Crisp whether Rambus might have patent claims that related to dual bank design. (CX2089 at 130, 131, 136-137 (Meyer, Infineon Tr.)). Mr. Crisp gave no verbal response, but rather shook his head. Mr. Kelley then commented to the group that “they don’t have anything to say about that.” (*Id.*).

3141. In his email from this JEDEC meeting, Mr. Crisp continued to monitor the progress of dual bank design technology. He wrote in his email back to Rambus that “2 banks appear to still be the route the suppliers are leaning.” (CX0673 at 1).

3142. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun’s 15 meg SDRAM specification which included a dual bank design. (CX0042 at 30 (“The 4M x 4 device is organized internally as two banks.”)).

3143. On September 25, 1992, Mr. Crisp met with Mr. Vincent to discuss what claims to add to patent applications that were already on file with the Patent and Trademark Office. (CX1949 at 1; Crisp, Tr. 3096-98). The first item in Mr. Vincent’s notes, with a star next to it, referred to a DRAM with “multiple open row addresses.” (*Id.*). Under the first three items in

his notes, Mr. Vincent wrote, “So cause problems w/ synch DRAM and Ramlink.” (*Id.*) According to Mr. Crisp, multiple open row addresses describes a concept that is similar to multiple open banks or multiple banks. (Crisp, Tr. 3097).

3144. On February 9, 1993, Richard Crisp responded to a Fred Ware email, in which Ware asked Crisp to provide “a list of claims which were under consideration for addition to the original patent.” Among other things, Crisp requested that Ware see that a claim be written up to cover a “DRAM with multiple open rows”. (CX0686 at 1). This technology is related to but broader than two banks as discussed within JEDEC. (Crisp, Tr. 3120-22).

3145. On June 18, 1993, an e-mail from Fred Ware indicated that Rambus was considering claims covering “DRAM with multiple open rows” that would be “directed against SDRAMs.” CX0702 at 1). Mr. Vincent was doubtful, however, as to whether the claims could be extracted from the specification of the ‘898 application. (*Id.*).

3146. On May 5, 1994, Allen Roberts wrote a letter to Mr. Vincent in which he suggested the addition of new patent claims to existing or new divisional applications. (CX0734 at 1). Mr. Roberts, for example, suggested that Mr. Vincent add claims on the use of “[m]ultiple and independently controlled and addressed internal DRAM memory regions (banks).” (*Id.*).

3147. Allen Roberts sent a copy of a Vincent’s draft preliminary amendment for the ‘646 application that Roberts characterized as “Lester’s attempt to write the claims for the MOST/SDRAM defense” to Rick Barth, Fred Ware and John Dillon. (CX0745 at 1).

3148. Mr. Vincent’s associate, Scot Griffin, filed a Preliminary Amendment to Application 08/222,646. (Cx1466 at 19). In this application, claim 182 refers to “a plurality of independently addressable memory sections . . .” (CX1466 at 12).

3149. Both JEDEC SDRAM and DDR SDRAM standards are based on a multiple bank design. (CX0234 at 116, 145).

3150. Mr. Crisp never informed Jedec that Rambus believed it could obtain patent coverage over dual bank design as it was being discussed at Jedec. (Crisp, Tr. 3456; *see* DX0028).

3151. Rambus may intend to assert patents relating to low voltage swing signaling against manufacturers or users of SDRAMs and DDR SDRAMs. (*See* CX1363 at 1 (listing “Multi-bank architecture” and “Doubled banks” as Rambus innovations)).

3. Auto-Precharge.

3152. At a number of meetings during the course of 1992, the JC-42.3 Subcommittee discussed using the auto-precharge technology in the SDRAM standard. (February 1992: JX0012 at 37, 39 (NEC), 76 (Fujitsu), 94 (Toshiba), 108 (Sun); April 1992: CX0034 at 32 (IBM), 33 (NEC), 35 (Hitachi); May 1992: CX0034 at 6, 150).

3153. At the September 16-17, 1992, JC 42.3 meeting, the Subcommittee considered Sun's 15 meg SDRAM specification which included an "autoprecharge" option. (CX0042 at 45).

3154. On September 21, 1992, Mr. Garrett and Mr. Crisp jointly sent to all Rambus executives and staff an e-mail summarizing the September 16-17, 1992 JC 42.3 meeting that they had just attended. (CX0680 at 1). The e-mail informed Rambus representatives that the Jedec Subcommittee discussed how to implement auto-precharge during this meeting. (*Id.* at 2; Crisp, Tr. 3095-96 (testifying that CX0680 refreshed his recollection that auto-precharge had been discussed at the September 1992 JC 42.3 meeting)).

3155. JEDEC included the auto-precharge feature in the SDRAM standard. (CX0234 at 145, 151 ("[Section] 3.11.5.1.5. [] gives the logic function used to activate the AUTO-PRECHARGE function.")).

3156. On May 5, 1994, Mr. Roberts wrote a letter to Mr. Vincent that contained a list of ways to "enhance [Rambus's] claim coverage." (CX0734 at 1). One of the ideas that Mr. Roberts proposed to Mr. Vincent for enhanced claim coverage was, "Selective precharging of banks following an access to improve access time." (*Id.*).

3157. On June 16, 1994, John Dillon wrote to the Rambus e-mail "exec" group, Fred Ware, and Richard Barth that, "I believe we might be able to claim this idea." (CX0738 at 1). At that time, Rambus may have only had a narrow claim that related to auto-precharge. (*Id.*). Mr. Dillon recommended filing a broader claim that the one that was pending at the time that would cover "auto-precharge for *any* DRAM." (*Id.*). He believed that "patenting this feature would have high harassment value." (*Id.*).

3158. Allen Roberts sent a copy of Vincent's draft preliminary amendment for the '646 application that Roberts characterized as "Lester's attempt to write the claims for the MOST/SDRAM defense" to Rick Barth, Fred Ware and John Dillon. (CX0745 at 1).

3159. Mr. Vincent's associate, Scot Griffin, filed a Preliminary Amendment to Application 08/222,646. (CX1466 at 19). In this application, claim 193 refers to a "control signal specif[ying] that the plurality of sense amps are to precharge the columns of the array of memory cells immediately after the data has been transferred." (CX1466 at 15).

3160. Mr. Crisp never informed anyone at Jedec that Rambus believed it could obtain

patent coverage over auto-precharge as it was being discussed at Jedec. (Crisp, Tr. 3457; *see* DX0028).

3161. Rambus may intend to assert patents relating to auto-precharge against manufacturers or users of SDRAMs and DDR SDRAMs. (CX1539 at 964, 967 (recently filed preliminary amendment seeking to add claim 151 which refers to a “plurality of sense amplifiers [that] are automatically precharged after the data is sensed” and claim 166 which refers to “precharging the plurality of sense amplifiers [] automatically after the data has been sensed.”)).

3162. On October 22, 2002 the PTO issued Rambus patent 6,470,405 (the ‘405 patent), which includes a claim relating to “initiating the precharge operation automatically after the write operation is initiated.” (CX1545 at 45).

4. Externally Supplied Reference Voltage.

3163. At the February 27, 1992, JC 42.3 meeting, Samsung proposed an externally supplied reference voltage. (JX0012 at 58; Crisp, Tr. 3043-3044 (acknowledging that “vref” refers to externally supplied reference voltage)).

3164. Mr. Garrett recorded in his notes at this meeting that Jedec had discussed the use of an externally supplied reference voltage. (CX0672 at 1 (“As for I/O, everyone agrees that at about 100MHZ signals will have to be terminated, that it cannot be rail-to-rail, and that it cannot rely on an internal Vref (i.e., that there would be an external Vref.”)).

3165. In 1992, JEDEC had considered both GTL and CTT signaling technology. At the February 1992 JC 42.3 meeting that Billy Garrett attended and informed Rambus staff about, the Subcommittee had discussed GTL technology for use with SDRAM. (JX0012 at 36, 56-58, 60, 101-02, 104, 111 (GTL technology)). At the May 7, 1992, JC 42.3 meeting, Fujitsu gave an SDRAM presentation that outlined set-up and hold timing details for “CTT I/O” signaling technology. (CX0034 at 139, 141).

3166. On February 20, 1993, Mr. Crisp recommended to Fred Ware in an e-mail that “we get [one additional claim] on the old patents [] where the voltage reference is provided to a dynamic memory chip for setting the input receiver’s thresholds.” (CX0691 at 1; Crisp, Tr. 3123-24 (confirming that this language is “probably very similar [to], if [] not the same” as externally supplied reference voltage)). According to Mr. Crisp, “[t]his should help confound the GTL effort.” (CX0691 at 1).

3167. On June 18, 1993, Fred Ware suggested patenting the use of an externally supplied reference voltage in a way that was “directed against CTT technology ” and communicating that idea to Mr. Vincent. (CX0702 at 1; Crisp, Tr. 3164-65 (confirming that

Rambus considered adding claims to externally supplied reference voltage that were directed against CTT technology)).

3168. Mr. Vincent's notes from the July 1993 meeting also refer to "externally supplied reference voltage." (CX1963 at 4).

3169. At the May 1994 JC-42.3 Subcommittee meeting, Mr. Crisp observed various presentations regarding specific SDRAM configurations. Mr. Crisp wrote in an e-mail to Mark Johnson, an attorney for Rambus, "Note that many of the SDRAMs use an externally supplied reference voltage in the input buffers. I believe we have a claim we added to cover this configuration. We should make note of this." (CX0711 at 26, 27; Crisp, Tr. 3190-91).

3170. Later in the same May 1994 meeting, Mr. Crisp noted, "(again we need to check claims about 'DRAM with input receivers using an externally supplied reference voltage'). We may be able to slow down or stop (or at least collect from) all of the CTT, GTL and HSTL devices if this claim is allowed (Allen, I believe this was one of the claims you, Lester, Tracy and I wrote up in late '91, right?)." (CX0711 at 26, 31; Crisp, Tr. 3192-93 (confirming that CTT, GTL, and HSTL "were acronyms for signaling technologies that were just various different either standards or proposals for standards.")).

3171. On March 14, 1995, Fujitsu gave a presentation on "STBUS" signaling technology to the JC 16 Subcommittee. (CX0711 at 53, 54; *see also* CX0082 at 13). In an e-mail to Rambus executives and others, Mr. Crisp stated that Rambus had claims that anticipated Fujitsu's STBUS proposal because it was a proposal for a current source device that relied on an externally supplied reference voltage. (CX0711 at 53, 54 ("Taken along with the fact that they rely on an externally bussed reference (this should be anticipated by some of our claims), I would say that proposal may well infringe our work."); Crisp, Tr. 3241 (confirming that the reference to an externally bussed reference is a reference to an externally bussed reference voltage)).

3172. JEDEC standardized pinouts for both SDRAM and DDR SDRAM parts that provide a pin that can be used, as an option, for an externally supplied reference voltage. (*See, e.g.*, CX0234 at 84 (pin 40); 85 (pin 40); 86 (pin 49); 87 (pin 49)).

3173. Mr. Crisp never informed Jedec that Rambus believed it could obtain patent coverage over the use of an externally supplied reference voltage as it was being discussed at Jedec. (Crisp, Tr. 3456; *see* DX0028).

3174. It is unclear whether Rambus might intend to assert patents relating to externally supplied reference voltage against manufacturers or users of SDRAMs and DDR SDRAMs because, although the feature is included as an option in the JEDEC standards, the externally supplied reference voltage feature is rarely used. (Lee, Tr. 11034-35).

5. Source Synchronous Clocking.

3175. At the April 1992 JC-42.3 Special Task Group meeting, Hitachi raised the issue of source synchronous clocking. (CX1708 at 2 (“Hitachi brought up the issue of source synchronous clocking.”); Crisp, Tr. 3053-54 (recalling that a discussion on source synchronous clocking had taken place at this meeting)).

3176. In an e-mail sent to all Rambus executives, among others, Mr. Crisp indicated that he thought that source synchronous clocking was a Rambus idea. (CX1708 at 2 (“It appears that someone inside Hitachi is believing that we have some good ideas!”)).

3177. On September 25, 1992, Mr. Crisp met with Mr. Vincent to discuss claims to be added to Rambus’s pending divisional applications. Mr. Vincent’s handwritten notes reflect an instruction, “must claim source-synch clocking.” (CX1949 at 5).

3178. By March 15, 1995, Rambus may have already had patent claims that related to source synchronous clocking. (CCFF 3179).

3179. During the March 15, 1995 JC 42.3 meeting, Mr. Crisp recorded a Fujitsu representative’s suggestion that it would be necessary to use two clocks, a clock-in and clock-out, for high speed operation. (CX0711 at 58). In an e-mail sent to Rambus executives and others, Mr. Crisp stated, “It appears that they are starting to figure out that we have a very good idea with respect to source synchronous clocking. Of course they may get in to patent trouble if they do this.” (*Id.*; Crisp, Tr. 3247-48 (confirming that what he had written to Rambus executives, in March 1995, was that Fujitsu might get into patent trouble if they used source synchronous clocking)).

3180. Mr. Crisp never informed anyone at JEDEC that Rambus believed it could obtain patent coverage over source synchronous clocking as it was being discussed at JEDEC. (Crisp, Tr. 3457; *see* DX0028).

3181. JEDEC included a bidirectional data strobe, or DQS strobe, as part of the DDR SDRAM standard. (CX0234 at 164). The data strobe might be considered to be a form of source synchronous clocking. (Lee, Tr. 6682).

3182. Rambus may intend to assert patents relating to source synchronous clocking against manufacturers or users of SDRAMs and DDR SDRAMs. (CX1363 at 3 (list indicating that “Source synchronous signaling” is a Rambus innovation contained in DDR SDRAMs); CX1371 at 5 (informing nVidia that “Rambus innovations” include “Source synchronous signaling”); CX1383 at 4 (informing ATI of same)).

C. The Remedy Should Be Worldwide.

3183. The remedy should extend not only to United States patents, but to foreign patents as well. (McAfee, Tr. 7521). This follows because relevant technology markets are worldwide. (McAfee, Tr. 7521, 7178). Thus, to enforce the remedies only on U.S. patents would not fully address the problem. (McAfee, Tr. 7521). The U.S. is a net importer of DRAM, so if patent enforcement occurs outside the U.S., there would actually be harm to U.S. consumers in the long run. (McAfee, Tr. 7521-22).

3184. Rambus has numerous foreign patents that are directly based on its original U.S. patent application no. 07/510,898 (the '898 application). (CX1452 (India); CX1453 (Taiwan)). Many of these foreign patents claim priority based on the '898 application and the benefit of its April 18, 1990 U.S. filing date. (CX1485 (Israel); CX1489 (Israel); CX1496 (Israel); CX1499 (Israel); CX1514 (Korea); CX1515 (Korea); CX1527 (Germany); CX1529 (Europe); CX1533 (Europe); CX1536 (Europe)).

3185. If Rambus can enforce foreign patents, SDRAM and DDR SDRAM manufacturers will find themselves in the same position that they are in today. (McAfee, Tr. 7521; CCF 3186-3326).

3186. Rambus has sought to enforce European patents against DRAM manufacturers in court proceedings in the United Kingdom, Germany, Italy and France. (CCFF 2026-2027).

3187. Rambus has stated publicly that it would pursue enforcement of foreign patents against DRAM manufacturers and others "vigorously." (CX1888 ("While the Virginia case against Infineon involves only four Rambus U.S. patents, there are a dozen U.S. and European patents involved in other infringement cases pending against Infineon, Hyundai and Micron. Rambus intends to pursue all these cases vigorously, including a trial against Infineon in Germany")).

3188. JEDEC standards are worldwide standards. (CX3037 at 1 ("Although nominally a US body, [JEDEC] is in fact supported by companies world-wide and is the De Facto setter of standards for many matters including memory device packages, pinnings and functions."); Appleton, Tr. 6274-75 (products manufactured by Micron overseas also comply with JEDEC standards and that JEDEC standards are world standards.); Rhoden, Tr. 294 (most of the DRAM production in the world comes from JEDEC members, and that "[a]lmost all DRAM manufacturers in the world are members of JEDEC."); Tabrizi, Tr. 9141-42 ("DRAM is a commodity and it's global and there is no -- not such a thing as local standardization. Everything is done on a worldwide basis. . . .")).

3189. SDRAM and DDR SDRAM manufacturers have worldwide operations. (Tabrizi, Tr. 9141-42; Bechtelsheim, Tr. 5886; CCF 3190-3198).

3190. Synchronous DRAM is produced throughout the world by various memory

manufacturers located or doing business in the U.S. and various foreign countries. Synchronous DRAMs, and products incorporating synchronous DRAMs, are imported and exported throughout the world in large volumes. (Rambus Answer at 44, ¶ 110).

3191. Micron ships large volumes of DRAMs internationally at relatively low cost. (Appleton, Tr. 6269-70 (“You know, the fact is that these devices are very, very small, they're not much in weight, and they move around the world pretty freely and at a relatively low cost.”)).

3192. Hyundai has worldwide sales operations. (CX2107 at 14-15 (Oh, Dep.)).

3193. All DRAMs produced by Hynix that are sold to U.S. customers must pass through Korea before they are distributed to U.S. customers in the United States or elsewhere in the world. (CX2107 at 20 (Oh, Dep.)). Although Hynix manufactures DRAMs in the United States, it does not have packaging and test capability in the United States. (CX2107 at 19-20 (Oh, Dep.)). In order to manufacture and sell DRAMs in the United States, Hyundai must first ship completed wafers to Seoul, Korea, where they are tested and packaged before being shipped back to the United States. (*Id.*).

3194. Micron has worldwide DRAM design, fabrication, test/assembly, and sales facilities. (Appleton, Tr. 6266-67, 6271-72; *see* DX0111, DX0112). Micron ships parts internationally as part of manufacturing, testing and packaging, with facilities for each in different places across the world. (Appleton, Tr. at 6269). Micron ships DRAM wafers across international borders “pretty freely and at a relatively low cost.” (*Id.* at 6269-70). About half of Micron’s DRAM chips, modules, and products that containing DRAMs are sold outside of the United States. (*Id.* at 6272-73; *see* DX0113).

3195. Micron has manufacturing operations in Avezzano, Italy; Nishiwaki-City, Japan; Singapore TECH, Singapore; and Singapore AT, Singapore. (CX2735 at 15. (“Micron Around the World”). Micron has overseas design facilities in Avezzano, Italy and Bracknell, England. (*Id.*). Finally, Micron has overseas semiconductor sales units in Munich, Germany; Bracknell, England; Tokyo, Japan; Taipei, Taiwan; and Singapore. (*Id.*).

3196. Infineon has worldwide DRAM manufacturing operations. (Reczek, Tr. 4298-4300).

3197. The vast majority of PCs sold in the world today use DDR SDRAM. (Wagner, Tr. 3750-51).

3198. Products incorporating drams are shipped across borders in large volumes. (Appleton, Tr. 6273 (“[W]e ship [DRAMs or DRAM modules] to that customer, and that customer incorporates that product into an end product, and then they ship it somewhere else in

the world.”)).

3199. Patent enforcement in any country could cause substantial problems for the market. (Appleton, Tr. 6397-98 (testimony that Rambus’s German litigation against Micron could cause the company significant harm); Bechtelsheim, Tr. 5886 (testifying that he was concerned that Rambus could cause a “dislocation in the memory market depending on the country” in which it decided to sue a DRAM manufacturer)).

3200. Rambus strategically developed foreign patents as part of its overall patent plan. Rambus’s 1990 business plan discusses pursuing foreign patent registration in multiple places. (CX0535 at 1, 4 (“The base patent is being filed over the next several months in the European Patent Office, Israel, Korea, Taiwan, Japan, India, and Canada. Five additional inventions have been identified These will be filed for patents in the US by early 1991 and worldwide by late 1991.”)).

3201. The first foreign jurisdictions that Rambus chose to file the base patent in were the European Patent Office, Israel, Korea, Taiwan, Japan, India, and Canada. (CX0535 at 1, 4).

3202. During the time that Rambus was a JEDEC member, part of the work by Rambus patent counsel Lester Vincent on behalf of Rambus involved work on foreign patent filings, including counseling Rambus representatives with respect to the countries in which they should file patent applications. (Vincent, Tr. 7878-79; see CX1937 at 28). This included providing Rambus with a chart listing countries currently or in the future expected to be involved in semiconductor manufacturing, packaging and assembly and computer production, to help Rambus in making foreign patent filing decisions. (CX1972 at 1, 2).

3203. On April 16, 1991, Rambus filed an International Patent Application under the Patent Cooperation Treaty (the PCT application). (CX1451 at 1). A PCT application is a mechanism that permits an applicant to file with the World Intellectual Property Organization (“WIPO”) an application based on a United States patent application, and thereafter enter the patent registration process in various foreign countries within a specified period. (Vincent, Tr. 7883; see CX1948).

3204. Rambus also filed an application with the European Patent Office (“EPO”). The EPO is an administrative mechanism for centralized examination of patent applications for various European countries. (Vincent, Tr. 7885-86, 7894-97). Rambus pursued examination of patent applications in this fashion in the United Kingdom, France, Germany and Italy. (Vincent, Tr. 7897; RX335).

3205. Rambus attempted to conform certain independent claims in the EPO application to the amended claims being prosecuted in the United States. (Vincent, Tr. 7899).

3206. In the second half of 1994, Rambus executives focused again on ensuring that they obtained patent coverage in key foreign countries. Rambus CFO Gary Harmon wrote to Vice President Allen Roberts, with a copy to CEO Geoff Tate, urging that Rambus “should file [patent applications] in the key foreign jurisdictions.” (CX0753 at 1 (“I think we have to do everything possible to pursue and protect those patents wherever in the world it makes economic sense.”)).

3207. In a letter dated October 16, 1994, Rambus’s outside patent attorney sent Mr. Harmon, Rambus’s CFO at the time, a chart identifying current and expected “Semiconductor Manufacturing Countries” and “Packaging and Assembly Countries.” (CX1972 at 1-2). The following countries were identified as semiconductor manufacturing countries: United States, Japan, Korea, Taiwan, Germany, Holland, Italy, Malaysia, Thailand, and Ireland. (*Id.* at 2). The chart included Japan, Korea, Malaysia, PRC, Phillippines, India, Mexico, and Thailand as packaging and assembly countries. (*Id.*). Mr. Vincent believed that Mr. Harmon “might find [the chart] helpful in making foreign filing decisions.” (*Id.* at 1).

3208. As of approximately 1995, there were Rambus patent applications based on the original Rambus ‘898 patent application pending with the EPO (Vincent, Tr. 7885-86), the WIPO (Vincent, Tr. 7883), India (Vincent, Tr. 7882), Israel (Vincent, Tr. 7885), Japan (Vincent, Tr. 7886-87) and Korea (Vincent, Tr. 7887). As of that time, Rambus had also been issued a patent in Taiwan based on the specification contained in the original Rambus ‘898 patent application. (Vincent, Tr. 7883-85). (See also CX1982).

3209. After 1996, Rambus continued to work on its foreign patent strategy. (CX1804 at 5-6, 8-10, 12-13). By September 30, 2002, Rambus had thirty-two foreign patents and had seventy-three additional applications pending in Europe and Asia. (CX1782 at 8).

3210. Today, Rambus holds foreign patents that claim priority back to its U.S. patent application no. 07/510,898 in Korea, Germany, and Europe. (CCFF 1670-1674).

3211. Rambus has foreign patents that it has asserted already or believes it could assert in the future against SDRAM and DDR SDRAM manufacturers in foreign countries. (*See* following # of proposed findings).

3212. Rambus has admitted “that it is involved in patent infringement lawsuits in various foreign countries that involve foreign patents that cover some of the same inventions at issue in the U.S. litigation.” (Rambus Answer at 42, ¶ 102).

3213.

(CX2072 at 45-46 (Tate, Dep.), *in camera*).

3214. Sometime after April 19, 2000, Rambus prepared a presentation which illustrates how several claims within European patent EP 0 525 068 B1 cover different features described within a Micron 64M DDR SDRAM data sheet. (CX1269). Claims 1, 6, 7, and 8 of the European patent are represented as covering programmable cas latency. (*Id.* at 37-43, 50-51, 52-53, 54-55, respectively). Claim 2 of the European patent is represented as covering a read operation that outputs data with each positive edge of the external clock. (*Id.* at 44-45). Claims 3 and 5 are represented as covering an on-chip DLL. (*Id.* at 46-47, 48-49, respectively). The presentation then illustrates how all of the aforementioned claims with the exception of claims 3 and 5 cover features described within a Micron 64M SDRAM data sheet. (*Id.* at 58).

3215. Sometime after April 19, 2000, Rambus prepared a presentation which illustrates how several claims within European patent 0 525 968 B1 cover different features described within an Infineon 256M DDR SDRAM. (CX1268 at 3). Claims 1, 6, 7, and 8 of the European patent are represented as covering programmable cas latency. (*Id.* at 2, 15-16, 17-18, 19-29, respectively). Claim 2 of the European patent is represented as covering a read operation that outputs dat with each positive edge of the external clock. (*Id.* at 9-10). Claims 3 and 5 are represented as covering an on-chip DLL. (*Id.* at 11-12, 13-14, respectively).

3216. On August 7, 2000, Rambus sued Infineon Technologies AG in Mannheim, Germany. (CX1866 at 1). In the complaint that it filed against Infineon, Rambus identified which Infineon DDR SDRAM and SDRAM devices it alleged to infringe several of Rambus's foreign patents. (*Id.* at 30, 39, 46).

3217. On August 31, 2000, Rambus sued Micron Semiconductor (Deutschland) GmbH in Mannheim, Germany. (CX1869 at 1). In the complaint that it filed against Micron, Rambus identified which Micron DDR SDRAM and SDRAM devices it alleged to infringe several of Rambus's foreign patents. (*Id.* at 43, 49, 54).

3218. On September 14, 2000, Rambus sued Micron European Limited in the United Kingdom. (CX1871 at 1). In the complaint it filed against Micron, Rambus identified DDR SDRAM and SDRAM device that it alleged to infringe a European patent. (CX1871 at 1, 6, 7).

3219. Rambus has also sued Micron in Italy. (Appleton, Tr. 6396).

3220. Rambus has stated publicly that it intends to continue to assert its foreign patents against DRAM manufacturers and others "vigorously." (CX1888 ("Rambus intends to pursue all these cases [involving U.S. and European patents] vigorously, including a trial against Infineon in Germany . . ."))).

3221. Rambus's litigation against Micron in Germany, Italy, and the United Kingdom has put the company at risk. (Appleton, Tr. 6397; CCF 3222-3223).

3222. Rambus's litigation against Micron in Italy has threatened and still threatens to shut down a large manufacturing plant there. (Appleton, Tr. 6397). Micron's plant in Italy employs 1,500-2,000 people. (*Id.*). It produces products that are shipped across the world. (*Id.* at 6398). As Micron's CEO testified, "We've invested hundreds of millions of dollars in that operation, and to have it not operate would obviously be very detrimental to us." (*Id.*). If Micron could not operate the plant in Italy, it would not longer be able to service customers that are currently purchasing product that originated from Italy. (*Id.* at 6397-98).

3223. Micron has several very large customers in Germany that it would not be able to supply product to if Rambus were successful in its German litigation against Micron. (Appleton, Tr. 6398). Rambus's litigation against Micron in Germany also poses risks to Micron that extend beyond German borders. (*Id.*).

3224. Mr. Bechtelsheim testified that his concerns were not limited to Rambus's enforcement of U.S. patents, but also extended to the potential enforcement of Rambus's foreign patents. (Bechtelsheim, Tr. 5886). As Mr. Bechtelsheim explained, "There's an additional issue here that the memory business is of course a worldwide or international business with some manufacturers in Europe, many of them in Asia, and one remaining in the U.S., so depending on the validity of such patent claims, it could have created a dislocation in the memory market depending on the country or area these memory manufacturers were manufacturing the devices. On top of that, Cisco also manufactures their own products all over the world and there could be a secondary issue of Rambus asserting claims against Cisco at the location of manufacturing Cisco Systems' own products." (*Id.*).

3225. Rambus may have additional foreign patents that cover SDRAM and DDR SDRAM which it has not yet asserted against DRAM manufacturers. (CX1888 at 1) (Rambus May 2001 press release: "Rambus holds newly issued U.S. and European patents covering Rambus inventions used by SDRAMs and DDR SDRAMs that have not yet been asserted in any litigation and are not impacted by the [Infineon trial] Court's decision."); CX1403 at 30 (the "Virginia decision involved only 4 patents" and that Rambus has "many others which are used by SDRAM/DDR.")).

3226. In July 2001, Rambus admitted that even if it lost its efforts to enforce its U.S. patents, it could still achieve its enforcement goals because its litigation strategy only requires success in one major jurisdiction. (CX1890 at 35 (Rambus Senior Vice President of Finance and CFO Bob Eulau: "I'll take a question then which is "What is the likelihood of SDRAM licensees not paying due to the Virginia outcome? We don't think this is very likely. . . .We've said that the litigation requires success in a major jurisdiction, but not in every jurisdiction."))).

D. The Remedy Should Extend To Future Standards.

3227. The prohibition on Rambus's enforcement of any patents filed (or based on

filings) prior to June 18, 1996 against JEDEC-compliant DRAMs should extend to DDR-II SDRAM as well as SDRAM and DDR SDRAM. (McAfee, Tr. 7519). This follows because in the likely but-for world, DDR SDRAM would not contain Rambus intellectual property. Therefore, JEDEC would not be building DDR-II SDRAM in the but-for world using DDR SDRAM as the baseline. (McAfee, Tr. 7519-20)

3228. Rambus's enforcement of its patents with respect to the DDR II SDRAM standard will continue to cause harm to the industry. (CCFF 3229-3261).

3229. The technologies claimed by Rambus had already been designated as part of the DDR-2 "baseline" as early as the summer of 1998, and changing them would delay the development of the standard and harm companies who have done work based on the adoption of the standard. (CCFF 3236-3243).

3230. Development work on DDR II SDRAM began at JEDEC in April of 1998 when the first meeting of the "Future DRAM Task Group" met. (CX0376A; CX0379A; Macri, Tr. 4582-83; Lee, Tr. 6769).

3231. JEDEC members believed that it was necessary to begin work on DDR II SDRAM that early, even prior to JEDEC's final adoption of the DDR SDRAM specification, because of the time it was expected to take to finalize the standard. (CX0140 at 3; Rhoden Tr. 412-414; Macri, Tr. 4607-608 ("The design cycle was long, so we needed to do this very early so that systems could be started to be designed – DRAMs could be designed such that when the DDR1 standard,... ended its life, the DDR2 standard and its systems would be ready to take over in a seamless fashion...[W]e needed to be proactive purely because you can't build these things in a day. It takes quite a bit of time.")).

3232. In order to allow the main DRAM committee at JEDEC, the 42.3 committee, to continue work on defining DDR, JEDEC formed the Future DRAM Task Group and designated Joe Macri of ArtX (later of ATI Technologies) as its chairman. (CX0376A; Macri, Tr. 4581).

3233. The goal of the Task Group was to derive a standard that would follow DDR SDRAM. (Macri, Tr. 4608). That standard was to be no more costly on a system level basis than PC-100 SDRAM. (CX0379A at 2; Macri, Tr. 4609-10).

3234. In addition, the new standard was intended to last for at least three DRAM density generations, a period of approximately six years. (CX0379A at 2; Macri, Tr. 4610). The reason that it was important that the new standard last at least three DRAM density generations was that it was necessary to allow the various manufacturers relating to the DRAM industry to amortize the cost of changing the standard over sales for a number of years. (Macri, Tr. 4610-11).

3235. Finally, the new standard was intended to be directed at a large number of markets. (CX0380 at 6 (“Same design must support desktop PC, laptop PC, workstations/small servers, various embedded applications.”)). As a result, wide participation in the task group by a variety of different types of firms was encouraged. (Macri, Tr. 4635; CX0378 at 1; CX0387 at 1 (“I have been working hard to involve as many people as possible in the definition of DDRII.”)).

3236. One of the first tasks of the committee was to determine the “baseline” for the DDR II SDRAM standard. (CX0379A at 9). The baseline was to be used as the starting point for the new standard. (Rhoden, Tr. 409-10). At the first meeting, in April of 1998, in order to determine what was to be the baseline for the new standard, a “straw vote” was taken of the members in attendance. The candidates were DDR SDRAM, SLDRAM (also known as Synlink) and RDRAM. DDR SDRAM received twenty-two votes in favor of it becoming the baseline, SLDRAM received 12 votes and RDRAM received zero votes. (CX0379A at 9; Macri, Tr. 4612-13).

3237. By the summer of 1998, the consensus of the committee was that the new standard should be DDR-based. (CX0132 at 4; CX2745 at 7; Macri, Tr. 4614; Lee, Tr. 6774-5). By February of 1999, work on the basic DRAM device was far enough along that a “DDR-II Module Task Group” was formed to establish the standard for the modules that would be used with the new DRAMs in PC main memory. (Kellogg, Tr. 5194-5; CX0393). By March of 1999, the major functions of the new standard were described. (CX0397 at 6).

3238. At the same time that the future DRAM Task Group was developing the standard for what became DDR II SDRAM, companies that intended to manufacture the DRAM as well as companies that intended to use the DRAM in their systems were working with the proposed standard as it developed, and giving feedback to the Task Group on the standard. (Macri, Tr. 4588-89; RX2234 at 14). Companies also worked with the proposed DDR II SDRAM standard as it developed because of the long lead time necessary to develop their products to full production. (CX0140 at 3 (“[T]he difference between first DRAM device design and full production is about 4 years.”)).

3239. Design work on DDR II SDRAM at Micron began in the fall of 1999. (Shirley, Tr. 4211). That design was based on DDR II SDRAM specification generated earlier by the marketing group at Micron. (Shirley, Tr. 4211). Micron’s first DDR II SDRAM design was taped out in January of 2002. (Shirley, Tr. 4228). By the end of 2002, Micron had taped-out at least one more DDR II SDRAM chips. (Shirley, Tr. 4229). Micron currently fabricates DDR II SDRAMs. (Appleton, Tr. 6264).

3240. By May of 2002, Samsung had finalized a GDDR-2 SGRAM chip. (CX2829 at 2; Wagner, Tr. 3852). GDDR-2 SGRAM was a DDR II like DRAM designed for use with graphics processors. (Wagner, Tr. 3837-38).

3241. Infineon is currently working on three DDR II SDRAM chips: a 256-megabit, a 512-megabit and a 1-gigabit DDR II SDRAM. (Peisl, Tr. 4387-88).

3242. Graphics chip designers were among the earliest adopters of DDR II. NVidia was working on designs for a graphics chip intended for use with DRAMs based on the DDR II SDRAM standard in late 2000 to early 2001. (Wagner, Tr. 3869). The Samsung GDDR-2 SGRAM is used with NVidia workstation products currently on the market. (CX2832 at 2; Wagner, Tr. 3838-40). ATI uses both GDDR-2 and GDDR-2m in current products. (Macri, Tr. 4579). GDDR-2m, like GDDR-2 is a variant of the DDR II SDRAM standard. (Macri, Tr. 4577-78).

3243. Removal of features from the standard after firms began designing products in reliance on the existence of those features in the standard could have been disruptive. (Macri, Tr. 4600). Additions to the standard, while maintaining the earlier functionality, were not as disruptive because they would not endanger the work done to date. (Macri, Tr. 4600).

3244. DDR II SDRAM was intended to be a follow-on to DDR rather than a new stand-alone standard. (CX0140 at 3). One of the main benefits of having DDR as the baseline for the new standard was that it allowed the DDR II SDRAM to be “backward compatible” with DDR. (Macri, Tr. 4611-12 (“One of the most critical really design attributes is backwards compatibility. What we do, we don’t want to change everything such that when you would design a new system for this DDR2 SDRAM, that it would be absolutely incompatible with the past.”)).

3245. The Task Group’s goal was that the standard be backward compatible in the sense that a DRAM could be designed and fabricated that complied with both the DDR SDRAM standard as well as the follow-on standard. (Kellogg, Tr. 5193; Macri, Tr. 4627-29; CX0392 at 3 (“DDR Based. This means we stay backward compatible if at all possible with DDR. A controller should be able to support both DDR and DDR-II. Initial RAMs might support DDR and DDR-II on the same die.”)).

3246. The Task Group also intended that the standard be backward compatible in the sense that a memory controller could be fabricated that could be used in motherboards designed for DDR as well as for motherboards designed to be used with the new standard. (CX0380 at 7; CX2717 at 13; CX2767 at 5 (“In every generation so far, we have been able to maintain the possibility of allowing controllers to be designed to support either old or new memory technology.”); CX0397 at 2; Lee, Tr. 6770-73; Macri, Tr. 4625-27).

3247. For DDR II SDRAM, this sort of backward compatibility could solve what is sometimes known as the “chicken and egg” problem that faces the DRAM industry when it transitions from an old standard to a new standard. (Macri, Tr. 4625-29). The problem, which can hinder the acceptance of new DRAM standards like DDR II SDRAM, is that industry

acceptance of a new DRAM standard requires the existence of additional compatible components, including particularly memory controllers. Those same considerations dictate that sales of a memory controller depend on the existence of compatible DRAMs. In both cases, unless one is available, the firms making the other will be hesitant to produce their component. (CX2315 at 1; Macri, Tr. 4619-20) (“It is a chicken and an egg problem..... The vendors won’t line up to produce the device unless there are users.... but the users won’t consider the part unless the suppliers/infrastructure is in place.”)).

3248. The benefit of backward compatibility to DRAM manufacturers is that it solves the chicken and egg problem by allowing them to produce DRAMs compliant with the new standard, but which could be sold as DRAMs compliant with the old standard if the new standard does not get accepted as quickly as expected. (Macri, Tr. 4627-29 (The DRAM manufacturers are “doing a design believing the user community will be there ready to accept it, but they too, don’t have control of their destiny. They’re dependent on the users and other people to build the infrastructure. So, they want to make sure that the design they do still has a market, and this allows them to ... manage that transition from the previous technology to the new technology with a minimum amount of risk.”)).

3249. Backward compatibility has the same benefit for producers of memory controllers. (Macri, Tr. 4625-26 (“We mitigate the risk in moving ahead to a new technology. A new technology could be delayed, so it’s important if you’re designing a system to use that new technology, if that technology was delayed for any reason, that it would be easy to use the old technology so you could still bring it to market.”) ; Kellogg, Tr. 5191-92; *see also*, Wagner, Tr. 3874-75).

3250. As a result of the fact that DDR was chosen as the baseline for the new standard, a number of technologies from DDR were imported into that standard. (Macri, Tr. 4613 (“[W]e wanted to pick the base architecture of the device,... the DRAM we would start with, and then modify it to form the standard, the new standard, DDR-2”). Among the technologies imported into the new standard because of the choice of DDR as the baseline were programmable CAS latency, dual-edged clocking of data off of a data strobe, and the use of a DLL on the DRAM to align the clock on the DRAM with the system clock. (Macri, Tr. 4633-35).

3251. One technology that was originally slated for removal from the baseline in the new standard was programmable burst length using the mode register. The new standard was originally set to have a fixed burst length of 4. Another technology that was slated for removal was the SDRAM burst interrupt instruction. (CX0392 at 1). However, in June of 2001, after a series of presentations from Intel, AMD and the ADT group, the task group determined that there were performance benefits for some high bandwidth applications from allowing a burst length of 8 as well as 4. (Macri, Tr. 4601-602; CX0174 at 35 (“Potential Improvement of 4-10% On High-Bandwidth Applications Such As SpecFP2000”); *see* DX46 at 4). The changes between June of 2001 and September of 2001 to add programmable burst length and burst

interrupt were not disruptive to the standard because they added to the functionality of the standard and did not eliminate existing functionality. (Macri, Tr. 4600).

3252. At some point, replacement of the fixed burst length of 4 with a fixed burst length of 8 would have been disruptive. (Macri, Tr. 4600 (“[S]ome systems take a very long time to design, and it’s really important that,... we provide stability to the designers. If we were to make a change that would cause them to go back and essentially tear up their design, we would be forcing companies to incur great expense,... not only on the design period but also on their product lines.”) *see also*, 4771-72, *in camera*; Polzin, Tr. 3993-94). In 2002, for example, NVidia was planning for its next generation graphics processor to be compatible with DRAM having a burst length of 4. (Wagner, Tr. 3853). A change in the available burst lengths for DDR II SDRAM that eliminated that burst length in favor of a burst length of 8 would require nearly 2 years of design work for the graphics processor to be able to efficiently operate with that DRAM. (CX2829 at 1; Wagner, Tr. 3852-53).

3253. Other changes to the baseline were considered by the Future DRAM Task Group, including the elimination of the use of the on-chip DLL, the elimination of dual edged clocking in favor of a faster single edged clock, and the replacement of programmable CAS latency. CCF 3254, 3256; CX2758 at 2 (DDR II SDRAM presentation to JEDEC discussing the possibility of eliminating read latency from existing and future SDRAM standards); Lee, Tr. 6777-80 (discussing CX2758)).

3254. The elimination of the DLL from the DDR II SDRAM was considered early on in the standard setting process. (RX1306-001 at 8) (“HP will look at removing DLL and its impact on turnaround time.”). At the time, the Task Group considered eliminating the DLL from the DRAM as a way to simplify the DRAM. (Macri, Tr. 4623). Eliminating the DLL from the DRAM was rejected because it would have been difficult to design a controller that would be compatible with both the DDR SDRAM that had a DLL and the new standard which would not have a DLL. (Macri, Tr. 4623-24 (“[I]t was decided since we were DDR-based that we should preserve the clock system to keep the backwards compatibility...”), *see also* 4646-48 (DLL on the DRAM “was already in the DDR1 JEDEC standard. Backwards compatibility was extremely important to our products, and we would have then forced ourselves to make a fundamental change in the clocking methodology, ... it’s the thing we focus on first, because it is the most important feature of any system.”)).

3255. By 2000, removing the DLL would have led to the additional problem of requiring that firms that had been either designing DDR II SDRAMs, or designing products to be compatible with DDR II SDRAM, to redesign their systems. (Macri, Tr. 4649) (“[basically the earliest adopters would have had to go back to the design stage. Clocking is not something they can change in a trivial manner.... So, I mean, it’s not something you want to go change at that point in time. You really need a gun to your head.”)).

3256. The replacement of dual edged clocking of data was considered in September of 2000 in a proposal by Micron. (CX2769 at 13; Lee, Tr. 6795-6798). The proposal was followed by a “DDR II clocking conference call” in November of 2000 that was set up in response to the proposal by Micron. (CX0426; Lee, Tr. 6798; Macri, Tr. 4639-40). At the conference call and the following JEDEC meeting, participants decided that the faster single-edge clock was feasible, but decided they needed to retain dual-edged clocking in the DDR II SDRAM standard. (Macri, Tr. 4641-42; Lee, Tr. 6799).

3257. One concern of those opposed to change was the late date of the proposal and the potential for such a change to be disruptive in the sense that it would cause the firms that had been working on designing products compliant with the new standard to have to throw away much of the work they had done. (Kellogg, Tr. 5201 (The proposal to eliminate dual edged clocking from the DDR II SDRAM standard “was a significant change to the DDR-II data capture structure, and IBM was already moving down the path of designing our first DDR-II memory controllers at this time.”); (Macri, Tr. 4649-51); (Wagner, Tr. 3869) (“[They would have,... brought in suggestions to change the technology and we would have said, we already have a standard, we don’t really want to change, or we’re on a development cycle that cannot tolerate the schedule hit.”); Peisl, Tr. 5545-55).

3258. By September of 2000, a number of firms were already planning and designing products for use with the new DDR II SDRAM standard. (Macri, Tr. 4648-49). Consequently, a number of participants in the conference call were strongly opposed to changing the clocking of the new DRAM standard to eliminate dual edged clocking. (Kellogg, Tr. 5204 (“One [potential impact of Micron’s proposal on IBM] is our DDR-I controller or interface chip that also included DDR-II would very likely see measurable schedule delay due to the significance of the changes.”)).

3259. A second concern was that the changes proposed by Micron to allow for single data rate clocking had the potential to delay the DDR II SDRAM standard, potentially indefinitely. (Kellogg, Tr. 5204-205 (“[W]e had systems in our product plan planning to use DDR-II and our belief was that the introduction of a total new clock structure would possibly prevent our ability to use DDR-II at all because there were so many new things to consider in the committee and it would slow down DDR-II indefinitely.”).

3260. A third concern was that the replacement of the DDR-type clocking with the clocking system proposed by Micron was so different from the DDR-type that it would be very difficult to design a controller that would be able to accommodate both technologies, thus eliminating backward compatibility with the DDR standard. (Lee, Tr. 6805-806 (“It is difficult to design a controller to support the future technology and the old technology with this kind of clocking scheme because it’s so different from the old technology’s clocking scheme. It’s a very difficult design to accommodate.”); Macri, Tr. 4640, 4649-50).

3261. Finally, the use of the Micron proposal in place of the DDR-type clocking scheme was opposed by DRAM customers. (Lee, Tr. 6806) (“We had made customer visits, and they wanted to have one standard that they felt could be designed and controlled to deal with the transition strategies for DDR and DDR2 simultaneously.”); Krashinsky, Tr. 2829 (“[W]e already decided how – how DDR is going to look like, the clocking, and if we are going to change DDR-II from DDR-I, the clocking rate is going to be too dramatic to the – its going to be what we call a revolutionary change rather than evolutionary change, and that’s why, to my knowledge, the committee decided not to go ahead with it.”)).

**UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION**

In the Matter of

RAMBUS INCORPORATED,

a corporation.

Docket No. 9302

**COMPLAINT COUNSEL'S
PROPOSED CONCLUSIONS OF LAW**

1. The Commission has jurisdiction over the subject matter of this proceeding and over Respondent Rambus Incorporated (hereafter “Rambus”).

2. Rambus is a public corporation organized, existing, and doing business under and by virtue of the laws of the State of Delaware, with its office and principal place of business located at 4440 El Camino Real, Los Altos, California 94022.

3. Rambus is, and at all relevant times has been, a corporation as “corporation” is defined by Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44; and at all times relevant herein, Rambus has been, and is now, engaged in commerce as “commerce” is defined in the same provision.

4. Rambus has violated Section 5 of the Federal Trade Commission (“FTC”) Act, as amended, 15 U.S.C. § 45, by engaging in conduct constituting unfair methods of competition (*see* ¶¶ 5-12 below).

5. There are four relevant lines of commerce in which to evaluate Rambus’s conduct, each involving technologies used in the design and manufacture of synchronous dynamic random access memories (“DRAMs”); they are:

- a. Latency Technology Market. The market for technologies used to specify the length of time – or “latency” period – between the memory’s receipt of a read request and its release of data corresponding with the request, including programmable CAS latency and any alternative technologies that may be economically viable substitutes for the use of programmable CAS latency in synchronous DRAM design.

- b. Burst Length Technology Market. The market for technologies used to specify the number of times data is transmitted between the central processing unit and memory – *i.e.*, the “burst length” – associated with a single request or instruction, including programmable burst length and any alternative technologies that may be economically viable substitutes for the use of programmable burst length in synchronous DRAM design.
- c. Clock Synchronization Technology Market. The market for technologies used to synchronize the internal clock that governs operations within a memory chip and the system clock that regulates the timing of other system functions, including on-chip DLL technology and any alternative technologies that may be economically viable substitutes for the use of an on-chip DLL in synchronous DRAM design.
- d. Data Acceleration Technology Market. The market for technologies used to accelerate the rate at which data are transmitted between the CPU and memory, including dual-edge clock technology and any alternative technologies that may be economically viable substitutes for the use of a dual-edge clock in synchronous DRAM design.

6. An additional relevant line of commerce in which to evaluate Rambus’ conduct is a market comprising, collectively, all technologies falling within any one of these narrower markets (hereinafter, the “Synchronous DRAM Technology Market”).

7. Each of the technology-related product markets identified above in ¶¶ 5-6 above is worldwide in scope.

8. Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, whereby it has obtained monopoly power in the Synchronous DRAM Technology Market and narrower markets encompassed therein, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

9. Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today, with a specific intent to monopolize the Synchronous DRAM Technology Market and narrower markets encompassed therein, resulting in a dangerous probability of monopolization in each of the aforementioned markets, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

10. Rambus has willfully engaged in a pattern of anticompetitive and exclusionary acts and practices, undertaken over the course of the past decade, and continuing even today,

whereby it has unreasonably restrained trade in the Synchronous DRAM Technology Market and narrower markets encompassed therein, which acts and practices constitute unfair methods of competition in violation of Section 5 of the FTC Act.

11. The foregoing conduct by Rambus has materially caused or threatened to cause substantial harm to competition and will, in the future, materially cause or threaten to cause further substantial injury to competition and consumers, absent the issuance of appropriate relief in the manner set forth in the attached Order.

12. The threatened or actual anticompetitive effects of Rambus's conduct include the following:

- a. increased royalties (or other payments) associated with the manufacture, sale, or use of synchronous DRAM technology;
- b. increases in the price, and/or reductions in the use or output, of synchronous DRAM chips, as well as products incorporating or using synchronous DRAMs or related technology;
- c. decreased incentives, on the part of memory manufacturers, to produce memory using synchronous DRAM technology;
- d. decreased incentives, on the part of DRAM manufacturers and others, to participate in industry standard-setting organizations or activities; and
- e. decreased reliance, or willingness to rely, on standards established by industry standard-setting collaborations.

13. The Order entered hereinafter is appropriate to remedy the violations of law found to exist.

**UNITED STATES OF AMERICA
BEFORE FEDERAL TRADE COMMISSION**

In the Matter of

RAMBUS INCORPORATED,

a corporation.

Docket No. 9302

**COMPLAINT COUNSEL'S
PROPOSED ORDER**

Upon Consideration of all of the evidence on the record in this matter:

I.

IT IS HEREBY ORDERED that for purposes of this Order, the following definitions shall apply:

- A. “Respondent” or “Rambus” means Rambus Inc., a corporation organized and existing under the laws of the State of Delaware, its directors, officers, employees, agents, representatives, predecessors, successors, and assigns; its joint ventures, subsidiaries, divisions, groups and affiliates controlled by Rambus Inc., and the respective directors, officers, employees, agents, representatives, successors, and assigns of each.
- B. “JEDEC” means the JEDEC Solid State Technology Association, a non-stock corporation organized and existing under the laws of the State of Virginia, its successors and assigns, and its divisions, subsidiaries and affiliates controlled by JEDEC.
- C. “JEDEC-Compliant Products” means

(1) any Dynamic Random Access Memory (“DRAM”) that complies with the JEDEC SDRAM Standard, published as JC 21-C, Release 4, as revised, the JEDEC SDRAM standard, published as JC 21-C, Release 9, as revised, the JEDEC DDR SDRAM specification, published as JESD 79, as revised, or with any future version of the JEDEC SDRAM standard, DDR SDRAM standard or DDR SDRAM specification, including, but not limited to, the JEDEC DDR-2

SDRAM standard;

(2) any product that interfaces with any DRAM defined in Paragraph I.C.(1); and

(3) any product that contains any product defined in either Paragraph I.C.(1) or C.(2), unless the product also contains one or more DRAMs that are not defined in Paragraph I.C.(1).

- D. “Action” means any lawsuit or other action, whether legal, equitable, or administrative, as well as any arbitration, mediation, or any other form of private dispute resolution, in the United States or anywhere else in the world.
- E. “Relevant U.S. Patents” means all current or future United States patents that claim priority back to U.S. Patent Application Number 07/510,898, filed on April 18, 1990, or to any other U.S. Patent Application filed by or on behalf of Rambus Inc. before June 17, 1996.
- F. “Relevant Foreign Patents” means all current or future patents issued by a foreign government that claim a priority date before June 17, 1996.
- G. “License Agreement” means any contract, agreement, arrangement or other understanding between Respondent and any other party or parties that requires, calls for, or otherwise contemplates, payment of fees, royalties or other monies, in cash or in kind, associated with the manufacture, sale or use of any product defined in Paragraph I.C.
- H. “Compliance Officer” means the officer, director, or full-time employee of Respondent employed pursuant to Paragraph VII. of this Order.
- I. “Standard-Setting Organization” means any group, organization, association, membership or stock corporation, government body, or other entity that, through voluntary participation of interested or affected parties, is engaged in the development, promulgation, promotion or monitoring of product or process standards for the electronics industry, or any segment thereof, anywhere in the world.

II.

IT IS FURTHER ORDERED that Respondent shall cease and desist any and all efforts it has undertaken by any means, either directly or indirectly, in or affecting commerce as “commerce” is defined in Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44, including, without limitation, the threat or prosecution of, or assertion of any affirmative defense in, any Action, pursuant to which Respondent has asserted that any person or entity, by

manufacturing, selling, or otherwise using any JEDEC-Compliant Product, infringes any of Respondent's Relevant U.S. Patents. Respondent shall dismiss or cause to be dismissed, with prejudice, all such prosecutions and all such affirmative defenses within thirty (30) days from the date this Order becomes final.

III.

IT IS FURTHER ORDERED that Respondent shall not undertake any new efforts by any means, either directly or indirectly, in or affecting commerce as "commerce" is defined in Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44, including, without limitation, the threat or prosecution of, or assertion of any affirmative defense in, any Action, pursuant to which Respondent asserts that any person or entity, by manufacturing, selling, or otherwise using any JEDEC-Compliant Product, infringes any of Respondent's Relevant U.S. Patents.

IV.

IT IS FURTHER ORDERED that Respondent shall cease and desist all efforts it has undertaken by any means, either directly or indirectly, in or affecting commerce as "commerce" is defined in Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44, including, without limitation, the threat or prosecution of, or assertion of an affirmative defense in, any Action, pursuant to which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using any JEDEC-Compliant Product for import or export to or from the United States, infringes any of Respondent's Relevant Foreign Patents.

V.

IT IS FURTHER ORDERED that Respondent shall not undertake any new efforts by any means, either directly or indirectly, in or affecting commerce as "commerce" is defined in Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44, including without limitation the threat or prosecution of, or assertion of any affirmative defense in, any Action, pursuant to which Respondent has asserted that any person or entity, by manufacturing, selling, or otherwise using any JEDEC-Compliant Product for import or export to or from the United States, infringes any of Respondent's Relevant Foreign Patents.

VI.

IT IS FURTHER ORDERED that Respondent shall cease any and all efforts by any means, either directly or indirectly, in or affecting commerce as "commerce" is defined in Section 4 of the Federal Trade Commission Act, 15 U.S.C. § 44, to collect any fees, royalties or

other payments, in cash or in kind, relating to the manufacture, sale or use of any JEDEC-Compliant Product pursuant to any existing License Agreement.

VII.

IT IS FURTHER ORDERED that,

- A. Within thirty (30) days from the date this Order becomes final, Respondent shall employ, at Respondent's cost, a Compliance Officer who will be the sole representative of Respondent for the purpose of communicating Respondent's patent rights related to any standard under consideration by any Standard-Setting Organization of which Respondent is a member.
1. The employee serving as the Compliance Officer shall be employed subject to the approval of the Commission, which approval Respondent shall seek pursuant to § 2.41(f) of the Commission's Rules of Practice, 16 C.F.R. § 2.41(f).
 2. Respondent shall provide the Compliance Officer with full and complete access to Respondent's books, records, documents, personnel, facilities and technical information relating to compliance with this Order, or to any other relevant information, as the Compliance Officer may reasonably request; and Respondent shall assure that the Compliance Officer has all information necessary to represent Respondent for the purpose of communicating Respondent's patent rights related to any Standard under consideration by any Standard-Setting Organization of which Respondent is a member. Respondents shall cooperate with any reasonable request of the Compliance Officer, including, but not limited to, the development or compilation of data and information for the Compliance Officer's use. Respondent shall take no action to interfere with or impede the Compliance Officer's ability to represent Respondent for the purpose of communicating Respondent's patent rights related to any Standard under consideration by any Standard-Setting Organization of which Respondent is a member.
 3. If at any time the Commission determines that the Compliance Officer has ceased to act or failed to act diligently, or is unwilling or unable to continue to serve, the Commission may require Respondent to employ a substitute to serve as Compliance Officer in the same manner as provided by this Order.

VIII.

IT IS FURTHER ORDERED that:

- A. Within thirty (30) days after the date this Order becomes final, Respondent shall distribute a copy of this Order and the complaint in this matter to JEDEC, to those members of JEDEC that Respondent contacted regarding possible infringement of any of its patents by JEDEC-compliant SDRAM and DDR SDRAM products, and to any other person or entity that Respondent contacted regarding possible infringement of any of its patents by JEDEC-compliant SDRAM and DDR SDRAM products.
- B. Within ten (10) days after the date this Order becomes final, Respondent shall distribute a copy of this Order and the complaint in this matter to every officer and director of Respondent, to every employee or agent of Respondent whose responsibilities include acting as Respondent's designated representative to any Standard-Setting Organization, and to every employee or agent having managerial responsibility for any of Respondent's obligations under this Order.
- C. For a period of five (5) years after the date this Order becomes final, Respondent shall furnish a copy of this Order and the complaint in this matter to each new officer and director of Respondent and to every new employee or agent of Respondent whose responsibilities will include acting as Respondent's designated representative to any Standard-Setting Organization or who will have managerial responsibility for any of Respondent's obligations under the Order. Such copies must be furnished within thirty (30) days after any such persons assume their position as an officer, director or employee. For purposes of this paragraph VIII.C., "new employee" shall include without limitation any of Respondent's employees whose duties change during their employment to include acting as respondent's designated representative to any Standard-Setting Organization, group or similar body of which respondent is a member.
- D. For a period of ten (10) years after the date this Order becomes final, Respondent shall furnish each Standard-Setting Organization of which it is a member and which it joins a copy of this Order and Respondent shall identify to each such organization the name of the person who will serve as Respondent's designated representative to the Standard-Setting Organization.

IX.

IT IS FURTHER ORDERED that:

- A. Respondent shall file a verified written report with the Commission setting forth in detail

the manner and form in which it intends to comply, is complying, and has complied with this Order: (i) within sixty (60) days after the date this Order becomes final; and (ii) annually for five years on the anniversary of the date this Order becomes final.

- B. Respondents shall include in its reports, among other things required by the Commission, a full description of the efforts being made to comply with the this Order, a description of all substantive contacts or negotiations relating to Respondent's participation in any Standard-Setting Organization of which Respondent is a member, the identity of all parties contacted, copies of all written communications to and from such parties, internal documents and communications, and all reports and recommendations concerning Respondent's participation in any Standard-Setting Organization of which Respondent is a member.
- C. For a period of ten (10) years after the date this Order becomes final, Respondent shall maintain records adequate to describe in detail any action taken in connection with the activities covered by Paragraphs II through VIII of this Order.

X.

IT IS FURTHER ORDERED that, for the purpose of determining or securing compliance with this Order, and subject to any legally recognized privilege, and upon written request with reasonable notice, Respondent shall permit any duly authorized representative of the Commission:

- A. Access, during office hours and in the presence of counsel, to all facilities and access to inspect and copy all books, ledgers, accounts, correspondence, memoranda and other records and documents in the possession or under the control of Respondent relating to any matter contained in this Order; and
- B. Upon five days' notice to Respondents and without restraint or interference from them, to interview the Compliance Officer and any other of Respondent's officers, directors, or employees, who may have counsel present, regarding any such matters.

XI.

IT IS FURTHER ORDERED that Respondent shall notify the Commission at least thirty (30) days prior to any proposed change in the corporate Respondent such as dissolution, assignment, sale resulting in the emergence of a successor corporation, or the creation or dissolution of subsidiaries or any other change in the corporation that may affect compliance obligations arising out of this Order.

XII.

IT IS FURTHER ORDERED that, this Order shall terminate twenty (20) years from the date this Order becomes final.

By the Commission.

Donald S. Clark, Secretary

SEAL

Issued: _____, 2003